# Modeling Techniques for Strained CMOS Technology

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Downscaling of MOSFETs as institutionalized by Moore's law is successfully continuing because of innovative changes in the technological processes and the introduction of new materials. The 32nm MOSFET process technology recently developed by Intel [1] involves new hafnium-based high-k dielectric/metal gates and represents a major change in the technological process since the invention of MOSFETs. Although alternative channel materials with a mobility higher than in Si were already investigated, it is commonly believed that strained Si will be the main channel material even for MOSFETs beyond the 32nm technology node. With scaling apparently approaching its fundamental limits, the semiconductor industry is facing critical challenges. New engineering solutions and innovative techniques are required to improve CMOS device performance.

Strain techniques are powerful to enhance performance of modern MOSFETs. Being relatively inexpensive and quite simple to incorporate in the modern technological process strain allows boosting the drive current in both p- and n-MOSFETs, which is used by the semiconductor industry already, since the 90nm technology node was introduced. Mobility and current enhancement is caused by a profound strain-induced modification of the silicon band structure. The valence band of silicon is standardly described by the six-band k.p Hamiltonian [2] including strain. With this approach the mobility enhancement in p-MOSFETs is well understood for both biaxial and uniaxial stress [3]. Compressive uniaxial [110] stress used by industry lowers the wings of the subband dispersion relation with the favorable transport mass in the transport direction. This effect combined with the stress-induced decrease on the density-of-states and scattering guarantees substantial mobility enhancement in p-MOSFETs [3].

The role of uniaxial [110] strain on mobility enhancement in n-MOSFETs was surprisingly less understood until recently. The reason is that the conduction band of silicon was usually approximated by six equivalent valleys, with each valley dispersion described by a parabolic approximation [4]. The effective masses were assumed to be constant and independent of strain. Thus, stress was considered only to lift the degeneracy between the six valleys of the conduction band. Engineering stress in such a way that the valleys with favorable transport effective masses shift down in energy and become more populated guarantees the electron mobility enhancement. Although this description is correct for biaxially and also uniaxially in [001] direction stressed silicon, there was a growing amount of indications that the model is not completely correct for [110] stressed silicon. The reason for doubts was an observed mobility enhancement in strained ultra-thin (001) silicon films [5], where the primed subbands are already depopulated due to the strong quantization. Additional application of strain should not improve the situation. Thus, the only reason for the mobility to be enhanced by [110] uniaxial tensile stress is the dependence of the transport effective mass on strain [5].

First experimental evidence that the effective masses of the [001] valleys depend linearly on [110] stress was reported long ago [6]. The reason for this dependence is the shear strain component generated by [110] stress. This component introduces an additional coupling between the two lowest conduction bands, which is quantitatively described by the two-band k.p Hamiltonian [6]. It was demonstrated that this form of the k.p Hamiltonian is the only one compatible with the symmetry properties of the Brillouin zone at the X-point [7]. Using the two-band k.p Hamiltonian shear strain dependences of the effective masses, the valley shifts and the band non-parabolicity parameter are obtained [8]. These parameters were used for the mobility enhancement calculations in the bulk [8].

Strain-induced mobility enhancement is the most attractive solution to increase the device speed and will certainly take a key position among other technological changes for the next technology generations. In addition, new device architectures based on multi-gate structures with better electrostatic channel control and reduced short channel effects will be developed. Confining carriers within thin Si films reduces the channel dimension in transversal direction, which further improves gate channel control. However, an accurate evaluation of the electron subband parameters based on the two-band k.p Hamiltonian in ultra-thin silicon films is still missing. This evaluation is critical for an accurate transport calculation in ultra-scaled thin body multi-gate MOSFETs. A multi-gate MOSFET architecture is expected to be introduced for the 22nm technology node. Combined with a high-k dielectric/metal gate technology and strain engineering, a multi-gate MOSFET appears to be the ultimate device for high-speed operation with excellent channel control, reduced leakage currents, nearly ballistic transport, and low power budget.

We compute the subband effective masses and demonstrate their strong dependence on shear strain and the film thickness. We also show that shear strain induces an additional splitting between the unprimed subbands with the same quantum number [9]. Furthermore, we demonstrate that this splitting is the key for the drive current enhancement in ballistic MOSFETs with (001) ultra-thin silicon body. The drive current increase combined with the improved channel control makes multi-gate MOSFETs based on thin films or silicon fins likely the best candidates for the 22nm technology node and beyond.

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