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# The Effect of Microstructure on Electromigration-Induced Failure Development

R. L. de Orio, H. Ceric, J. Cervenka, and S. Selberherr

Institute for Microelectronics, TU Wien, Gußhausstr. 27–29/E360, A-1040 Wien, Austria

The effect of the microstructure on the electromigration failure development is analyzed. We investigate the influence of the statistical distribution of copper grain sizes on the electromigration time to failure distribution. Also, the effect of the microstructure on the formation and development of an electromigration-induced void is studied by simulation and the results are compared with experiments. It is shown that the lognormal distribution of the grain sizes resulted in lognormal distributions of the electromigration lifetimes. A close investigation has shown that the network of grain boundaries has a decisive impact in the determination of void nucleation sites and main features of void development.

## Introduction

According to The International Technology Roadmap for Semiconductors (ITRS) 2008 Update (1) the copper dual-damascene technology process will continue to be applied for the fabrication of on-chip interconnects for the next technological nodes. The metal wiring pitch in microprocessors units will reach as down as 64 nm for the 32 nm node, and 44 nm for the 22 nm node. At the same time, the expected operating current densities can reach 2.11 MA/cm$^2$ and 2.80 MA/cm$^2$, respectively. Under such conditions, electromigration will continue to be a major reliability concern.

Electromigration data have been described by lognormal distributions (2). Although the origin of the lognormal distribution of electromigration lifetimes is not entirely clear, it has been argued that the diffusion process in connection with the effect of microstructure on electromigration provides the basis for the lognormal distribution (3). In copper dual-damascene interconnects the main diffusivity path is along the copper/capping layer interface. This interfacial diffusion is affected by the orientation of the grains. As the copper grain sizes seem to follow lognormal distributions in typical dual-damascene process technology (3) and due to the influence of microstructure on the electromigration process, the lognormal distribution has been considered the underlying statistics for electromigration lifetimes. However, it has been discussed whether this choice is the most appropriate (4, 5).

Grain boundaries affect electromigration in different ways. First, they are natural locations of atomic flux divergence. Second, they act as fast diffusivity paths for vacancy diffusion (6) and, third, grain boundaries act as sites of annihilation and production of vacancies (7).

The main challenge in electromigration modeling and simulation is the diversity of physical phenomena which have to be taken into account for an adequate description of the problem. Electromigration transport is also accompanied by material transport driven

by the gradients of material concentration, mechanical stress, and temperature. Furthermore, taking into account the effects of interfaces and grain boundaries as fast diffusivity paths imposes new challenges for electromigration modeling.

In this work we analyze the effect of the microstructure on the electromigration failure development. We investigate the influence of the statistical distribution of copper grain sizes on the electromigration time to failure distribution. Moreover, the effect of the microstructure on the formation and development of an electromigration-induced void is studied by simulation and the results are compared with experiments.

## Electromigration Modeling

Several driving forces are responsible for the vacancy transport in a conductor line under electromigration. The combination of these driving forces leads to the total vacancy flux given by

$$\vec{J}_v = -D_v\left(\nabla C_v + \frac{\left|Z^* e\right|}{k_B T} C_v \nabla\varphi - \frac{Q^*}{k_B T^2} C_v \nabla T + \frac{f\Omega}{k_B T} C_v \nabla\sigma\right), \qquad [1]$$

where $D_v$ is the vacancy diffusion coefficient of the dominant transport path, $C_v$ is the vacancy concentration, $Z^*e$ is the effective charge, $Q^*$ is the heat of transport, $f$ is the vacancy relaxation ratio, $\Omega$ is the atomic volume, $\sigma$ is the hydrostatic stress, $k_B$ is Boltzmann's constant, and $T$ is the temperature.

Vacancies accumulate or vanish in sites of flux divergence, and this dynamics is described by the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G(C_v), \qquad [2]$$

where $G(C_v)$ is the source function which models vacancy generation and annihilation processes (8). The source term $G(C_v)$ plays a major role for the mechanical stress build-up and is taken into account only at interfaces and grain boundaries. It comprises three processes, namely, the exchange of point defects between adjacent grains, exchange of point defects between grains and grain boundaries, and the formation/annihilation of point defects at grain boundaries.

In our model, the grain boundary is treated as a separate region which can trap or release vacancies, as shown in Figure 1. We denote the vacancy concentration from both sides of the grain boundary as $C_v^1$ and $C_v^2$, respectively, and the concentration of immobile vacancies which are trapped inside the grain boundary as $C_v^{im}$.

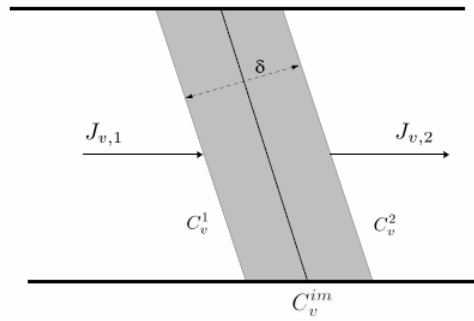



Figure 1. Grain boundary model.

The trapping rate of vacancies at the grain boundary, which corresponds to the generation/recombination rate, is controlled by the atomic fluxes $J_v^1$ and $J_v^2$, yielding (9)

$$\frac{\partial C_v^{im}}{\partial t} = G = \frac{1}{\tau}\left( C_v^{eq} - C_v^{im}\left( 1 + \frac{2\omega_R}{\omega_T\left(C_v^1 + C_v^2\right)}\right)\right), \qquad [3]$$

where $\omega_T$ is the trapping rate of vacancies from the both neighboring grains, $\omega_R$ is the release rate, and $C_v^{eq}$ is the equilibrium vacancy concentration inside the grain boundary, given by

$$C_v^{eq} = C_v^0 \exp\left(\frac{\sigma_{nn}\Omega}{k_B T}\right), \qquad [4]$$

where $C_v^0$ is the equilibrium vacancy concentration in the absence of stress and $\sigma_{nn}$ is the stress component normal to the grain boundary. Eq. [3] shows that grain boundaries act as source/sinks of vacancies provided that the concentration of trapped vacancies deviates from the equilibrium one. τ represents the vacancy relaxation time and it characterizes the efficiency of the grain boundary as vacancy sink/source (9)

$$\frac{1}{\tau} = \frac{\omega_T\left(C_v^1 + C_v^2\right)}{\delta}. \qquad [5]$$

The strain growth from both sides of the grain boundary is proportional to the growth rate of immobile vacancies (10)

$$\frac{\partial \varepsilon_{kk}}{\partial t} = \Omega\left[ (1-f)\nabla \cdot \vec{J}_v + f\,\frac{\partial C_v^{im}}{\partial t}\right], \qquad [6]$$

where $\varepsilon_{kk}$ is the trace of the strain vector.

Gleixner *et al.* (11) showed that void nucleation due to vacancy condensation is not expected to occur. They suggest that flaws at the metal/capping layer interface may provide a mechanism having low energy barrier for void formation. It is shown that the

stress threshold ($\sigma_{th}$) required for void nucleation at some weak adhesion point is given by (11)

$$\sigma_{th} = \frac{2\gamma_s \sin\theta_c}{R_p}, \qquad [7]$$

where $R_p$ is the radius of the adhesion-free patch, $\theta_c$ is the contact angle between the void and the surface, and $\gamma_s$ is the surface energy. If we assume the adhesion free patch with a radius of 10 nm (about 20 atoms) and $\theta_c = \pi/2$, we obtain $\sigma_{th} \sim 344$ MPa (9).

As a void is nucleated in the interconnect line, a new phase of failure development starts, the void evolution phase. An evolving void surface is shaped by two dynamic forces, namely the chemical potential gradient and the electron wind. Including both contributions, the total surface vacancy flux is (12)

$$\vec{J}_s = J_s\vec{t} = -D_s\left(\left|eZ^*\right|\vec{E}_s + \Omega\nabla_s\left(\frac{\sigma:\varepsilon}{2} - \gamma_s\kappa\right)\right), \qquad [8]$$

where $\vec{t}$ is the unit vector tangential to the void surface, $\vec{E}_s = E_s\vec{t}$ is the local component of the electric field tangential to the void surface, $\nabla_s$ is the surface gradient operator, $1/2(\sigma:\varepsilon)$ is the strain energy density of the material adjacent to the void surface, and $\kappa$ is the curvature of the void surface. $D_s$ is given by an Arrhenius law

$$D_s = \frac{D_0\delta_s}{k_B T\Omega}\exp\left(-\frac{Q_s}{k_B T}\right), \qquad [9]$$

where $\delta_s$ is the thickness of the diffusion layer, $Q_s$ is the activation energy for the surface diffusion, and $D_0$ is the pre-exponential coefficient for mass diffusion.

## Numerical and Simulation Approach

Equations [1]-[7] are solved using the finite element method (FEM) until the stress threshold for void nucleation is reached at some weak adhesion point. We consider the intersection of grain boundaries with the copper/capping layer interface as natural places of weak adhesion (13). As grain boundaries and interfaces act as fast diffusivity paths, the diffusion coefficient in eq. [1] has to be adapted for these regions. We have used $D_v^{gb} = 10^4 D_v^{bulk}$ for grain boundaries and $D_v^{Cu\text{-}cap} = 10^5 D_v^{bulk}$ for the copper/capping layer interface (14). It should be pointed out that all model parameters are equal for all grains and all simulated structures. Grain boundaries, and generally, all interfaces of the problem geometry have to be supplied with an appropriately fine FEM mesh. This is necessary in order to provide sufficient resolution for the local dynamics described by the proposed model.

The void evolution equations are solved using the Level Set Method (15). The evolving surface of the void is implicitly represented by a level set function $\phi$, which is governed by the Hamilton-Jacobi equation

$$\frac{\partial \phi}{\partial t} + v_n \|\nabla \phi\| = 0 , \qquad [10]$$

where $v_n = \nabla_s \cdot \vec{J}_s$ is the speed function which describes the evolution of the level set and, consequently, the void development.

In order to include the grain distribution into the numerical simulations, a microstructure generator tool has been developed. Given a specific interconnect structure and providing the tool with a median grain size and corresponding standard deviation, it generates a lognormal distribution of grain sizes. Then, following this distribution, the interconnect line is cut along its length by the planes that form the grain boundaries.

## Results and Discussion

Effect of microstructure statistics on electromigration lifetimes distribution

In order to evaluate the impact of the microstructure statistics on the electromigration lifetimes, three standard deviations for the distribution of grain sizes are considered, namely 0.1, 0.3 and 0.6. For each of them 20 dual-damascene interconnect structures were created using the microstructure generator. As the interconnect line is assumed to present a bamboo-like structure, the median grain size is equal to the line width, 0.10 µm. In these simulations, the barrier, capping, and interlayer dielectric layers are Ta, SiN, and $SiO_2$, respectively. The applied current density is 1.5 $MA/cm^2$, and the temperature is 300 °C.

Figure 2(a) shows the hydrostatic stress development for the structures with grain size standard deviation of 0.3. In Figure 2(b) the electromigration lifetime distributions for all simulated microstructures are presented. The lifetimes are fitted by lognormal distributions. The obtained standard deviations of electromigration lifetimes are about 0.0065, 0.0080 and 0.0086 for the grain size distributions with standard deviations of 0.1, 0.3 and 0.6, respectively.

The standard deviations for the electromigration lifetimes are very small compared to those frequently observed in experiments (2). Several factors can explain this behavior. First, for convenience, we have used a small value of stress threshold as failure criterion to determine the interconnect lifetime. As can be seen from Figure 2(a), the variation of the lifetimes can be more pronounced for higher stress thresholds. Second, the simulation parameters and material properties are independent of the grain distribution. This means that mechanical properties and the diffusivities are equal and constant for all grains in an interconnect line, for all simulated structures. This is clearly not the case in real experiments, as it is well known that material properties vary according to the grain orientation. It is expected that atomic diffusion along the copper/capping layer interface changes from grain to grain, inducing a flux divergence at the corresponding grain boundary. Moreover, the diffusivities are different from line to line as the grain distribution varies. Therefore, given the simplifications we have made, the small standard deviations obtained from our simulations should be expected.

When the grain size distribution presents a smaller standard deviation the corresponding interconnect lines have a more uniform distribution of the grains. As a consequence, the stress build-up presents smaller variations yielding smaller standard deviation of electromigration lifetimes. On the other hand, the lines present significant differences in the microstructure as the grain size standard deviation increases. This leads to increased variations for the stress development. Thus, a bigger standard deviation of electromigration lifetimes is expected. This behavior is presented in Figure 2(c). It shows that the increase of the standard deviation of the distribution of grains sizes increases the standard deviation of the electromigration lifetime distribution.

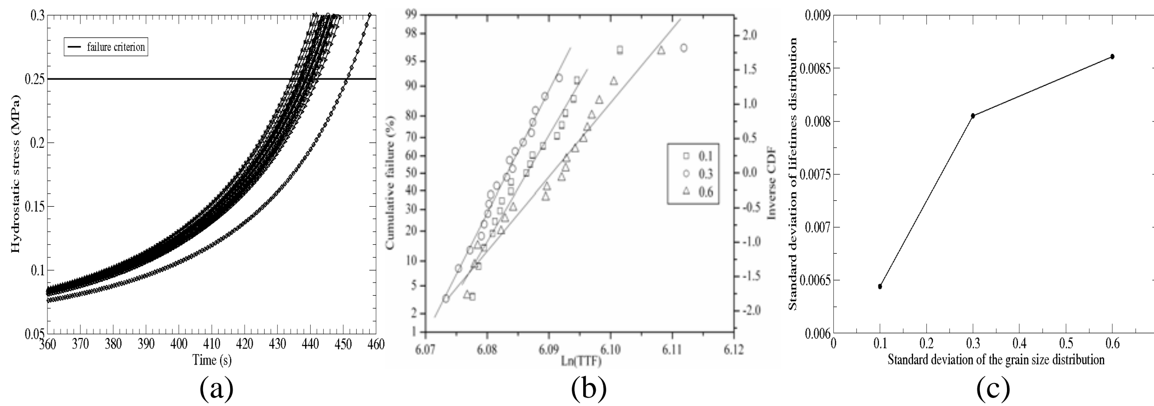



Figure 2. (a) Peak of hydrostatic stress development for the set with grain size standard deviation of 0.3. (b) Electromigration lifetime distributions. (c) Electromigration lifetime standard deviation for different standard deviations of grain size.

Effect of microstructure on the void nucleation and evolution

In this analysis all parameters for simulation are set according to experiments published in (16). The line width is 0.18 µm, the applied current density is 1.5 MA/cm$^2$, and the temperature is 300 °C. Barrier and capping layers are Ta/TaN and SiCN, respectively. SiOC is used as passivation layer. The simulated structure is shown in Figure 3(a).

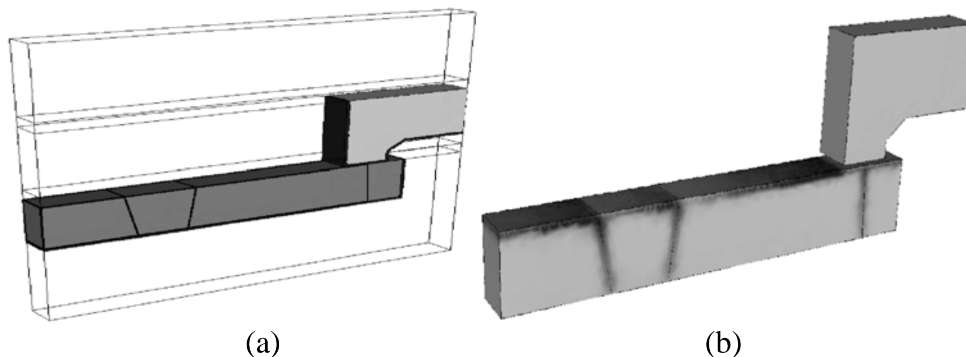
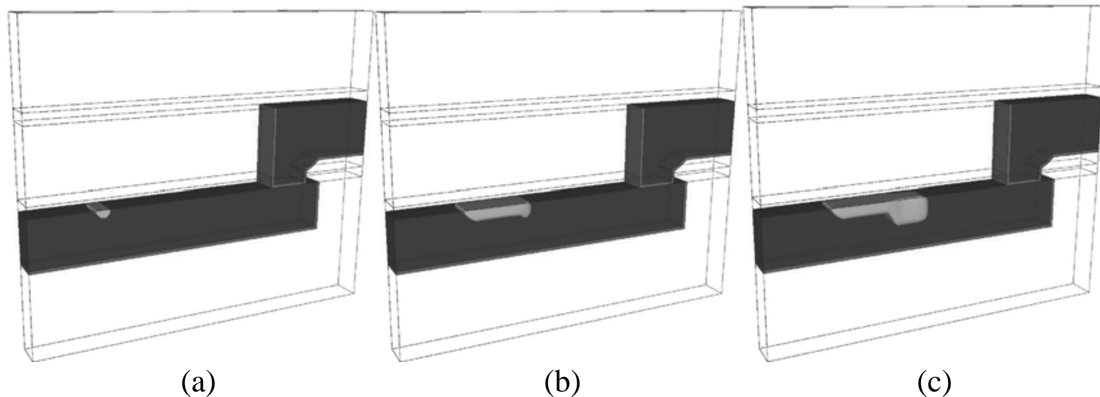



Figure 3. (a) Simulated interconnect structure. (b) Peak hydrostatic tensile stress distribution (dark areas) caused by electromigration.

Figure 3(b) shows the hydrostatic stress distribution along the interconnect line. Peaks of electromigration-induced stress develop at triple-points formed by the grain boundaries

and the copper/capping layer interface, which are natural sites of weak adhesion. Once the stress reaches the threshold $\sigma_{th}$, a small spherical void is set at the corresponding triple point location, as shown in Figure 4(a), and the Hamilton-Jacobi equation [10] is solved.

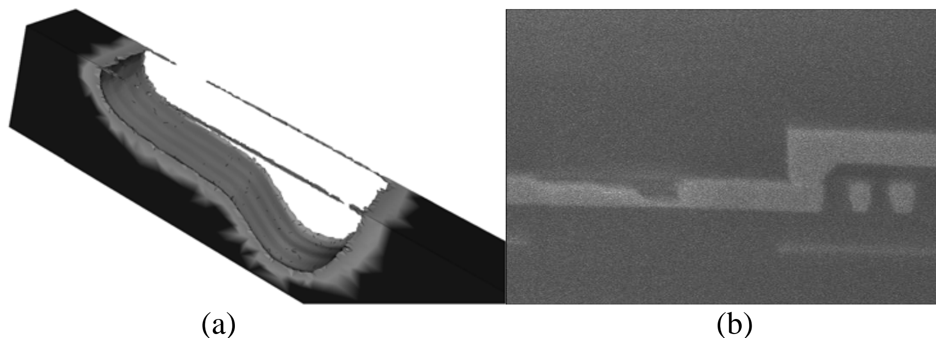


(a) (b) (c)

Figure 4. (a) Initial void placed at the nucleation site. (b) The void moves and encounters the second grain boundary. (c) Void shape changes as it drifts toward the via.

After the void is nucleated, it moves in the direction of the electric current flow. As the void encounters the second grain boundary (c. f. Figure 3(a)), it receives an additional flux of vacancies. Therefore, the void goes through a shape change process and grows through the line. As the void grows the local cross section for electric current flow decreases, which leads to a significant increase of the interconnect resistance. The void development process is shown in Figure 4(b) and (c).

The results of simulations and experiments demonstrate a decisive impact of the microstructure on the failure development (16). The void first nucleates at a triple point, then grows and changes its shape, leading to the interconnect failure. A detailed view of the fatal void is shown in Figure 5(a). For comparison, a FIB cross section of interconnect after an electromigration test is shown in Figure 5(b). The experimental result clearly shows that the applied models, together with the assumed microstructure, satisfactorily reproduce the observed void dynamics.



(a) (b)

Figure 5. (a) Detail of the final void shape. (b) FIB cross section of interconnect after an electromigration test (16) (courtesy of Dr. Lucille Arnaud).

## Conclusion

We presented a detailed analysis of the vacancy dynamics at grain boundaries and related mechanisms of stress build-up at triple points. We studied the influence of the microstructure on the electromigration-induced failure development. The simulation results indicated that the lognormal distribution of the copper grain sizes is the primary cause for the lognormal distributions of the electromigration lifetimes. A close investigation of the effect of microstructure on the void nucleation and evolution has shown that the network of grain boundaries has a decisive impact in the determination of void nucleation sites and main features of void development.

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