On the Thermal Activation of Negative Bias Temperature Instability

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ABSTRACT

The temperature dependence of negative bias temperature instability (NBTI) is investigated on 2.0nm SiO_2 devices from temperatures ranging from 300K down to 6K with a measurement window of ~12ms to 100s. Results indicate that classic NBTI degradation is observed down to ~200K and rarely observed at temperatures below 140K in the experimental window. Since experimental results show the charge trapping component contributing to NBTI is thermally activated, the results cannot be explained with the conventionally employed elastic tunneling theory. A new mechanism is observed at temperatures below 200K where device performance during stress conditions improves rather than degrades with time, which is opposite to the "classical" NBTI phenomenon.

INTRODUCTION

Upon application of a large negative bias to the gate of pMOS transistors, crucial device parameters, such as the threshold voltage, are observed to shift as a function of stress time, particularly at temperatures above 300K. Historically, both the trapping of holes in oxide defects and the creation of interface states have been suspected to be the cause of the degradation [1]. A logarithmic time dependence in the degradation of the threshold voltage is often considered the characteristic signature of a hole trapping contribution [2-4]. Conventionally, this hole trapping has been analyzed using elastic tunneling theory which predicts it to be temperature-independent [2-4]. However, recent results clearly indicate that the hole trapping component contributing to NBTI is thermally activated, which is incompatible with elastic tunneling [5]. Rather, the recorded data are consistent with hole capture according to multiphonon theory [6-8].

Further clarification to the elastic/inelastic tunneling argument can be made by examining NBTI hole trapping at cryogenic temperatures. The elastic tunneling theory predicts little change in hole trapping at low temperatures compared to the multiphonon theory. Little work on the response of NBTI on cryogenic temperatures has previously been published (e.g. [9]). This paper attempts to fill this gap by examining pMOSFET drain current response to stress and relaxation biases at temperatures ranging from 6K to 300K.

The remainder of this paper is organized as follows: First, an introduction to multiphonon theory is given with particular emphasis on its prediction on temperature dependence. Second, experimental equipment, devices, and measurement procedure is presented. Third, results demonstrating the freeze-out of the NBTI mechanism during the experimental window for temperatures less than 140K is presented along with observation of "classic" NBTI degradation and recovery for higher temperatures. In some devices, an increase in the drain current versus time during stress and a decrease in the drain current during relaxation was observed and is presented and discussed in the results section under *Non-classic NBTI observations*. Finally, a summary and future work section is present in which suggestions for further cryogenic temperature NBTI measurements are made.

THEORY

In [5], a model for the charge trapping component of NBTI based on multiphonon theory has been suggested using established features of switching traps (possibly E' centers). According to this model, the logarithmic time dependence is the result of a superposition of individual defects with widely distributed characteristic time constants charging (during stress) and discharging (during recovery) according to $\exp(-t/\tau)$. The time constants, τ, strongly depend on bias and temperature. In general, with increasing bias and temperature, the time constants become shorter, that is, charge capture and emission are accelerated by bias and temperature. The temperature activation is expected to follow an Arrhenius behavior [5, 6, 8].

As a consequence of this superposition of individual trap responses, degradation and recovery will start with the contribution of the fastest trap and end with the contribution of the slowest one. A particularly intriguing observation is that neither the fastest nor slowest trap are normally observable during stress or recovery. During stress, even with a measurement resolution of 1µs, the degradation takes place outside the measurement range [10]. Similarly, during recovery, discharging occurs earlier than the measurement window [11, 12]. We remark that reports exist claiming that the minimum time constants are in the order of 1µs [13, 14]; however, this is not in agreement with other data that show degradation and recovery are already in full flight at 1µs [10-12].

Figs. 1 and 2 show simulation results using the recently suggested two-stage model for NBTI which explains the hole trapping component by a switching trap model [5]. The model was calibrated to data obtained on devices with EOT ~1.4 nm SiON in the temperature range 298K to 473K and −0.6V to −2.0V. The behavior predicted in the much wider temperature range (100-300K) used in this simulation is speculative but consistent with the data presented below for "classic" NBTI behavior. The simulation demonstrates that the trap minimum time constant increases with reducing temperature.

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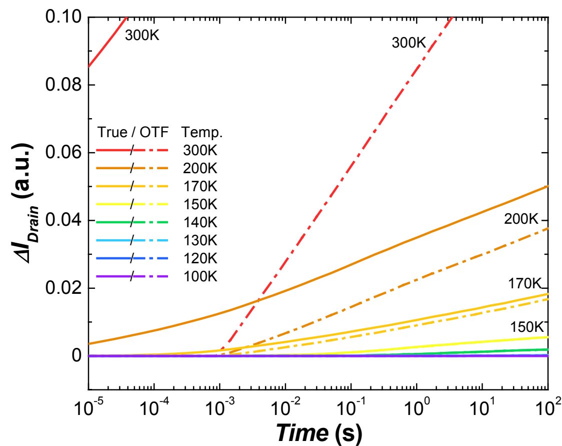

Fig. 1: Theoretical temperature dependence of the degradation monitored in an on-the-fly (OTF) measurement with V_{Gate} = -2V. The model parameters are taken from [5]. The solid lines give the simulated real degradation while the dot-dashed lines emulate the OTF measurement with a delay of 1ms. Only at temperatures below 150K is the minimum time constant within the experimental window, making the simulated real degradation agree with the OTF result. For temperatures below 140K, the minimum time constant becomes larger than 100s, resulting in no visible degradation within the experimental window.

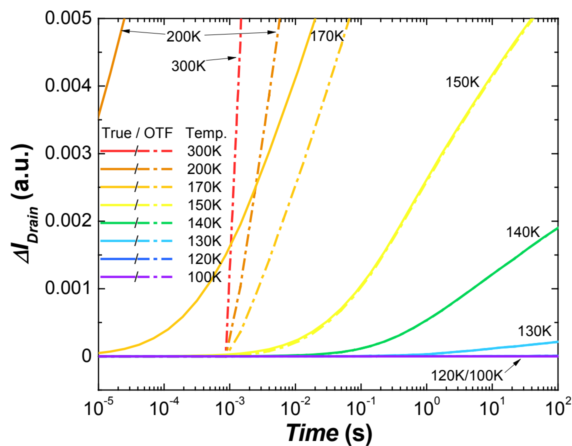

Fig. 2: Same as Fig. 1 except on a smaller vertical scale.

EXPERIMENTAL

Devices used in this study are conventional pMOSFETs with a pure SiO_2 dielectric of 2nm and a poly-Si gate electrode made in a 0.13µm process. Device sizes are wide 100µm by 0.25µm or 0.35µm pMOSFETs. Wide devices are used to increase the signal-to-noise ratio. Devices were stressed and relaxed at temperatures ranging from 6K to 300K using a Keithley 4200SCS with remote pre-amps. Temperature control was achieved using a Janis Research custom-built variable temperature probe station (5.6K to 450K) with actively cooled probes. Devices were stressed at V_{Gate} = -2V for 100s and relaxed for 1,000s at $V_{Gate} = V_{TH}$ with V_{Drain} = -100mV. The nominal minimum measurement time for stress was ~12ms with a nominal minimum measurement time for relaxation of ~7ms. Pre-stress and post-relaxation gate leakage current and threshold voltage measurements were performed with voltages between -0.4V and 0.1V.

The drain current measured during stress and relaxation was analyzed by examining trends in the relative percent change in the drain current defined as follows:

$$\%\Delta I_{Drain} = \frac{I_{Drain}(t) - I_{Drain}(t_0)}{I_{Drain}(t_0)} \times 100 \quad (1).$$

For both the stress test and the relaxation test, t_0 is the time of the first measurement point of each test. Hence, t_0 for stress is not the same as t_0 for the relaxation test. As such, $\%\Delta I_{Drain}$ references the start of the stress test or the start of the relaxation test and therefore always begins at zero. It does not reference the movement of the pre-stress threshold voltage. Due to noise in the raw data, only the 10 point adjacent average of the data and trend lines are shown for clarity.

RESULTS AND DISCUSSION

During the course of this study on 2.0nm SiO_2 gate dielectrics, two competing mechanisms were observed. The first mechanism is the "classic" NBTI mechanism, where the absolute value of the drain current *decreases* during stress and *increases* during relaxation. The second mechanism was observed when the absolute value of the drain current *increased* during stress and *decreased* during relaxation. The "classic" NBTI mechanism is discussed first.

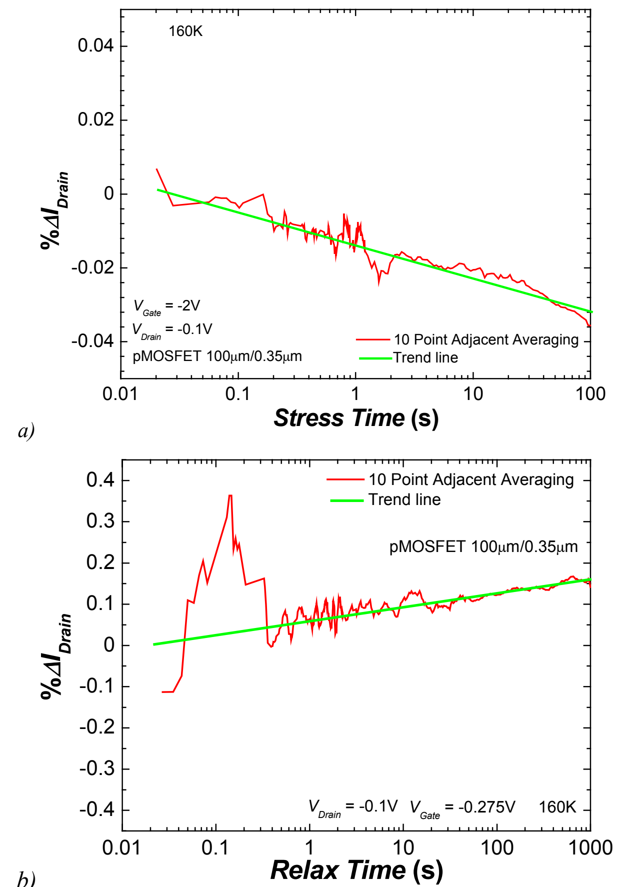

Fig. 3: Classic NBTI *a)* degradation and *b)* recovery observed at 160K. To increase clarity, the raw data have been excluded and a 10 point adjacent averaging line is plotted. Green trend lines are also plotted to aid the reader. For part *b),* excessive noise is observed during the relaxation test following the stress test until a lower current measurement range change is made to accommodate the smaller drain current measured during relaxation.

Classic NBTI Degradation and Recovery

Classic NBTI degradation (Fig. 3*a*) and recovery (Fig. 3*b*) at 160K is clearly visible. Green lines are added to highlight the trends observed during the measurement window. Stress tests at temperatures below 140K (Fig. 4*a*) resulted in non-appreciable degradation in the drain current. The absence of observable degradation (Fig. 4*a*) and recovery (Fig. 4*b*) below 140K within the measurement window shows NBTI is a thermally activated process. Note that this would not be the case for the temperature-independent elastic tunneling process. To verify stress-induced leakage current (SILC) was not a factor in the measurements, gate leakage current (I_{Gate}) measurements were performed before (I_{Gate0}) and after NBTI stress and relaxation measurements. Fig. 5 shows the SILC parameter, $(I_{Gate}-I_{Gate0})/I_{Gate0}*100$, changes very little (+/- 0.5%) due to the NBTI stress which indicates SILC degradation is not significant.

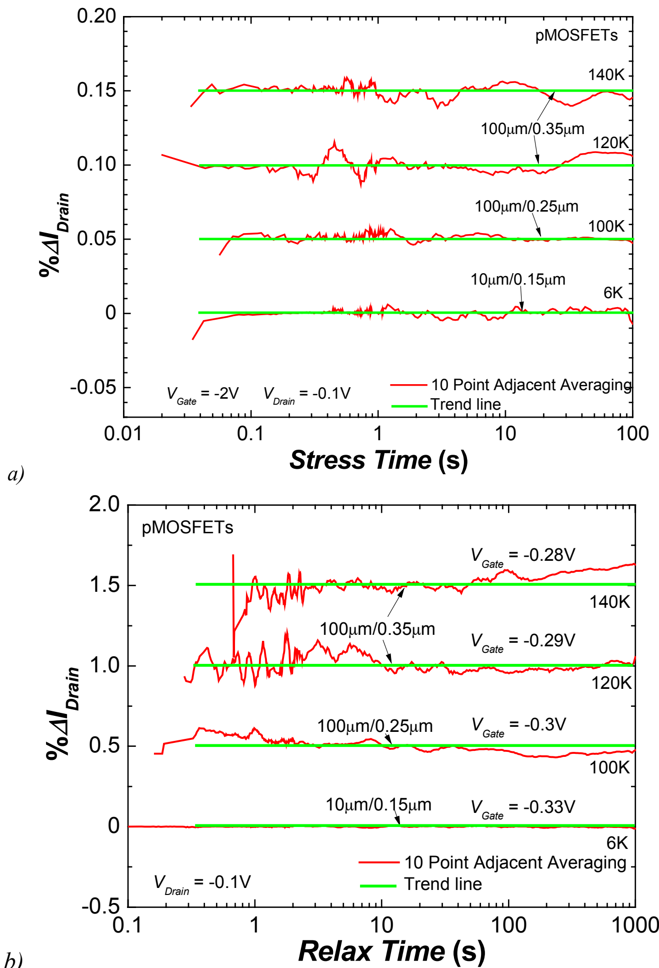

Fig. 4: Relative percent change in the drain current for devices measured at 6K, 100K, 120K, and 140K during stress (part a) and relaxation (part b). Degradation or recovery are not observed for these temperatures indicating NBTI is a thermally activated process. The 6K data were taken on a device with W/L = 10µm/0.15µm, and in order to make the noise levels comparable to the devices with W/L = 100µm/0.25µm, the signal was scaled by (10µm·0.15µm)/(100µm·0.25µm) = 0.06 (i.e., $W_1 \cdot L_1/W_2 \cdot L_2$). The data is offset to aid viewing.

NBTI data obtained at 150K (Figs. 6 & 7) show the absence of drain current degradation for the first second followed with observation of drain current degradation. Fig. 6 provides experimental evidence for the multiphonon theory yielding a time constant τ of about 1s for the fastest defect at V_{Gate} = -2V and T = 150K for this particular device. It is expected that, if the temperature was lowered, the minimum time constant value would increase and be moved outside the measurement window resulting in data resembling Fig. 4.

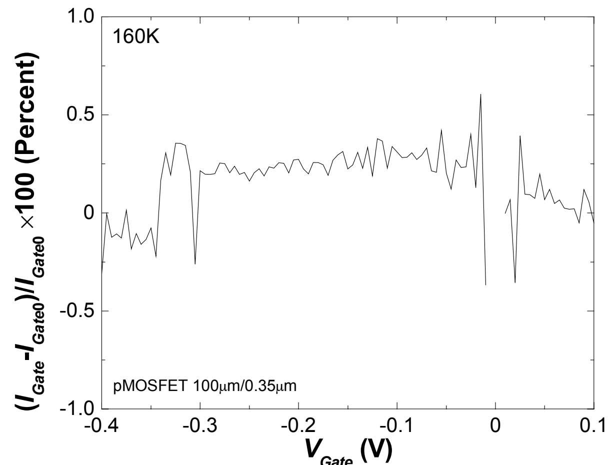

Fig. 5: Example of SILC data comparing gate leakage currents before NBTI stress to after NBTI relaxation at 160K. A very small change in the gate leakage data is observed indicating NBTI temperatures, voltages, and time scales used did not result in significant SILC. Data points about zero (where significant measurement inaccuracies occur) have been removed for clarity.

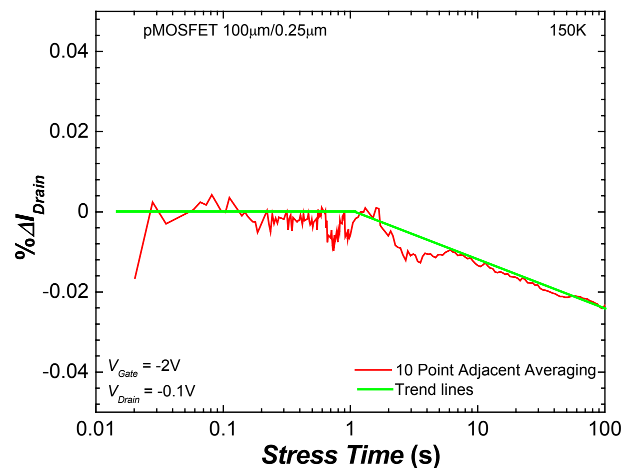

Fig. 6: NBTI stress test is shown for 150K. The red line is a 10 point adjacent average used post-measurement to reduce noise. The green straight lines are visual elements to aid in the observed trends. No degradation is observed for the first ~1s followed by classic NBTI degradation. This result is consistent with the multiphonon theory.

In a recent paper [15], it was suggested that the initial degradation of the pMOSFET is due to elastic tunneling. However in this study elastic (temperature-independent) charge trapping contributions were not detectable during either stress or recovery. Naturally, our measurement delay of 10ms does not rule out the existence of such a mechanism. However, since the time constants would be below 10ms, this mechanism has neither any bearing on our measured NBTI degradation nor can it be confused with the actual NBTI mechanism. The minimum time constant (e.g. Fig. 6) however was observed only twice. This was due to the competing mechanism discussed below.

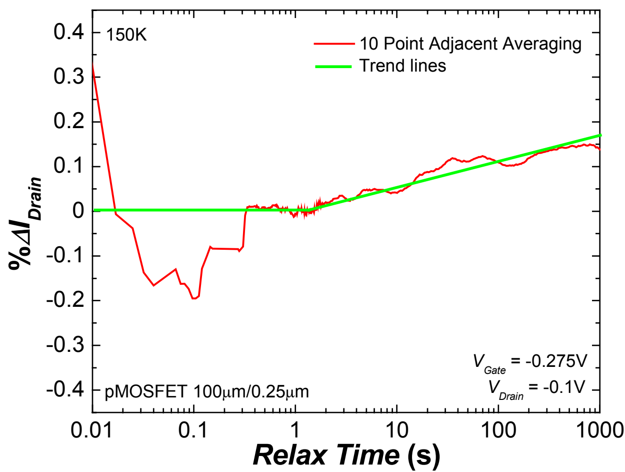

Fig. 7: NBTI relaxation test at 150K. The red line is a 10 point adjacent average used post-measurement to reduce noise. The green straight lines are visual elements to aid in the observed trends. No relaxation occurs for the first ~1s followed by classic NBTI relaxation.

Non-classic Abnormal NBTI Observations

Monitoring the drain current during stress (V_{Gate} = -2V) and relaxation ($V_{Gate} = V_{TH}$) resulted in changes to the drain current opposite to the expected NBTI behavior in some devices at temperatures below ~200K. Significant deviation from the classic NBTI behavior is seen when the measurement window of the stress test is extended to 1,000s. During stress, the absolute value of the drain current increases (Fig. 8) rather than decreases (Fig. 3*a*). During the relaxation test, the absolute value of the drain current decreases (Fig. 9) rather than increases (Fig. 3*b*).

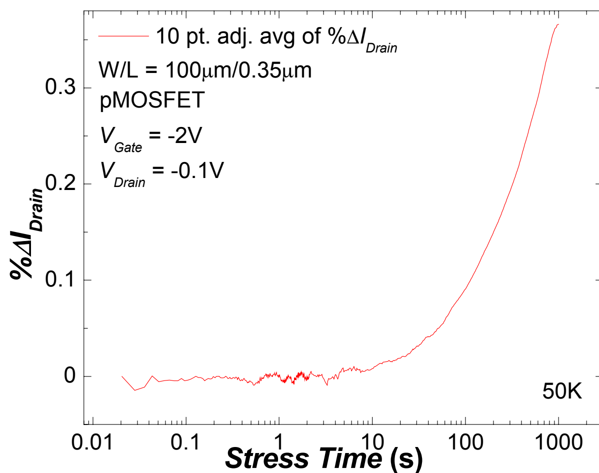

Fig. 8: Abnormal instabilities in the drain current are observed at temperatures below ~200K in some devices. Observed during stress at 50K, the drain current *increases*, which is opposite to the "classic" NBTI behavior.

Examining the sub-threshold slope (Fig. 10) before stress and after relaxation shows noticeable improvement. A reduction in the interface defect density would account for a reduction in the sub-threshold slope by increasing the surface potential movement with respect to the gate voltage. The improved sub-threshold slope results in a lower magnitude drain current at voltage near and below the threshold voltage which could account for the reduction in the drain current magnitude seen during relaxation (Fig. 8).

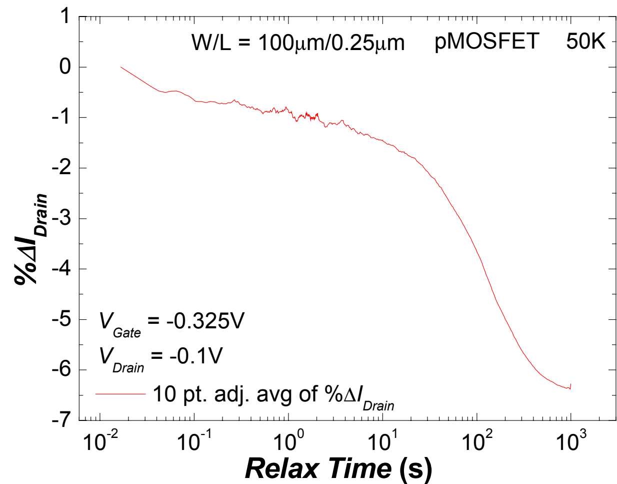

Fig. 9: Abnormal instabilities in the drain current are observed at temperatures below ~200K in some devices. Observed during relaxation at 50K, the drain current *decreases*, which is opposite to the "classic" NBTI behavior.

A reduction in the interface state defect density would also yield mobility enhancements providing higher magnitude drain currents in the strong inversion regime. Since characteristic drain current measurements were not performed at large voltages (to avoid inducing NBTI effects), it is difficult to say what may be causing the drain current increases that are observed (Fig. 8). The increases may be due to mobility improvements or a slight shift to the threshold voltage due to negative charge trapping [16]. Close inspection of the gate leakage current before stress and after relaxation (not shown) shows a slight reduction in the gate leakage current indicating passivation/reduction of defects which contribute to the gate leakage current. The reduction of the active contribution of these defects may be the same defects responsible for the increased sub-threshold slope (hypothesized to be interface state defects).

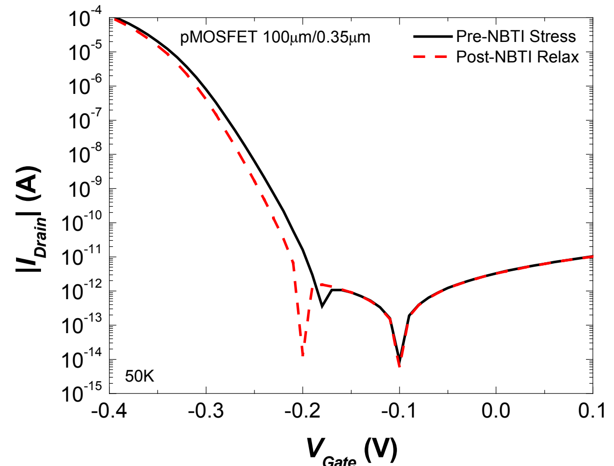

Fig. 10: In some devices tested at cryogenic temperatures, the device improves rather than degrades with time. The sub-threshold slope is observed to improve from 22.0mV/dec (before stress) to 19.4mV/dec (after relaxation) at 50K. The "hump" observed between V_{Gate} = -0.1V and -0.2V corresponds to a gate to drain leakage current dominating the drain current. The net drain current changes direction when the source to drain current dominates.

The amount of drain current increase during stress and decrease during relaxation varies from device to device with some devices showing no observable change, as in Fig. 4. It is supposed that

passivation of extrinsic defects are responsible for the device improvement during stress and relaxation. Such passivation is not observed at temperatures higher than ~200K due to classic NBTI behavior dominating the device characteristics.

At temperatures where classic NBTI degradation was observed, above ~140K (Figs. 3 & 6), the classic NBTI behavior and the abnormal behavior are observed to compete as shown in Figs. 11 & 12. In Fig. 11, classic NBTI behavior is observed during stress for the first ~1s and then abnormal NBTI behavior is observed. Notice that according to the multiphonon theory the fastest trap contributing to classic NBTI behavior has already occurred in this particular device at 150K (Fig. 11). During relaxation (Fig. 12), recovery of the drain current (classic NBTI behavior, a shift to the right in the threshold voltage) is observed for the first ~1s followed by a decreases in the drain current magnitude (abnormal behavior, an increase in the sub-threshold slope).

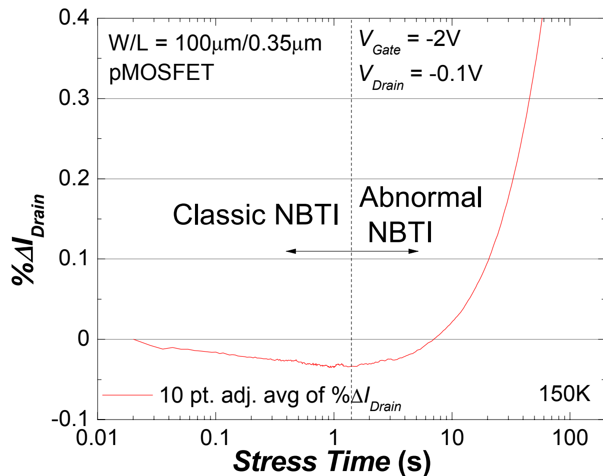

Fig. 11: NBTI stress test at 150K demonstrating the competing mechanisms of classic NBTI degradation and abnormal NBTI improvement. The vertical dashed line indicates the separation between the observed classical and abnormal NBTI behaviors.

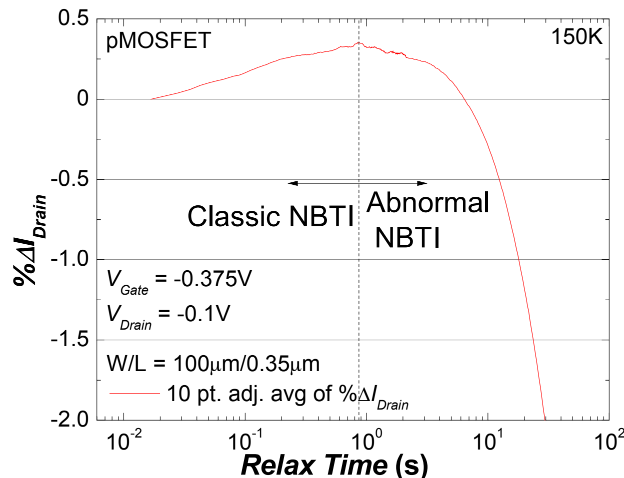

Fig. 12: NBTI relaxation test at 150K demonstrating the competing mechanisms of classic NBTI recovery and abnormal NBTI degradation. The vertical dashed line indicates the separation between the observed classical and abnormal NBTI behaviors.

As the temperature increased beyond 200K, the abnormal NBTI mechanism was not observed. Fig. 13 illustrates the temperature range of the abnormal and classic NBTI behaviors observed in this study. To better understand the mechanism of the abnormal NBTI further research is needed. As the abnormal NBTI mechanism masked the behavior of the classic NBTI mechanism, additional validation of the multiphonon theory predictions on the temperature dependence of NBTI is needed.

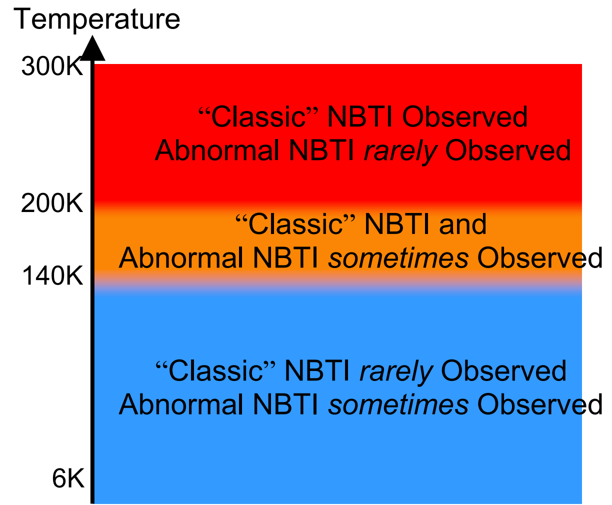

Fig. 13: Summary of temperature dependence of observed NBTI mechanisms. Drain current degradation and improvement (classic NBTI) was not observed at temperatures below ~140K. Above ~200K abnormal NBTI was not observed while classic NBTI was.

SUMMARY AND FUTURE WORK

Experimental evidence has been provided indicating that the logarithmic component contributing to NBTI degradation and recovery is thermally activated. By reducing the temperature, the minimum time constant of this charge trapping mechanism can be increased and moved into the experimental window. Finally, no evidence of an elastic tunneling process contributing to the classic NBTI mechanism could be detected within our experimental window from 10ms up to 100s, clearly confirming that the recoverable component of NBTI is due to *inelastic* hole trapping. In addition to the classic NBTI mechanism discussed in the literature, a new mechanism was observed in which the drain current magnitude increases during stress and decreases during relaxation in some devices. This mechanism was noticed at temperatures below ~200K and competed with the classic NBTI mechanism at temperatures above ~140K. The abnormal NBTI mechanism is device dependent suggesting extrinsic defects may be the cause. The increase in device performance is speculated to arise from passivation of interface/near interface traps.

Future work is required to confirm experimental evidence presented here to the theoretical predictions of the multiphonon theory. In particular, identifying devices where the abnormal NBTI mechanism is not present would be useful in understanding the underlying temperature dependence of the classic NBTI mechanism. Suggestions include investigating NBTI on nitrided oxides and high-k dielectrics. A through investigation of the abnormal NBTI mechanism observed here is also suggested where more than just the drain current response is measured.

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Questions and Answers

Q1: Some of the devices showed improvement with time during stress, could you please comment on it?

A1: In some of the devices tested at temperatures below 200K, device characteristics improved. Post NBTI stress and relaxation characterization tests in these devices show a slight decrease in the gate leakage current, improvement in the sub-threshold slope, and higher mobility. It is unclear what the mechanism is that triggers these events. Possible ideas include a reduced interface trap density (perhaps passivated by slow trapping carriers at low temperatures) or electron trapping. A more thorough study is needed to better understand and determine what the cause of device improvement with stress at low temperatures.