TUTORIALS

Chair: Drew Turner

Circuit Failure Prediction for Robust System Design in Scaled CMOS

Subhasish Mitra, Stanford University

Circuit failure prediction predicts the occurrence of a circuit failure "before" errors actually appear in system data and states. This is in contrast to classical error detection where a failure is detected after errors appear in system data and states. Circuit failure prediction is performed concurrently during system operation or during periodic on-line self-test by analyzing the data collected by special circuits called "sensors" inserted at strategic locations inside a chip. This talk demonstrated the concept of circuit failure prediction, practical implementation of the concept, and its effectiveness in overcoming major scaled-CMOS reliability challenges such as early-life failures (also called infant mortality) and aging. The concept of circuit failure prediction also provides insignts into early-life failure behaviors that may be used in developing new techniques for screening early-life failure candidates during production test.

Measurement Issues for High-k Technology including NBTI

Chadwin Young, SEMATECH

This tutorial was comprised of several parts that address various measurement methodologies required for properly characterizing high-k gate stacks. While discussing these techniques, emphasis was placed on proper instrumentation and set up, followed by proper data analysis and interpretation. Some of the key methodologies that were discussed are: Capacitance – Voltage (C-V), Pulsed Current – Voltage (I-V), and reliability evaluation techniques. The intended outcome of this tutorial was for the attendees to leave with a better understanding of high-k characterization requirements that he/she can implement in everyday measurements and have increased insight about these novel gate stacks.

JEDEC Overview

Alvin Strong, IBM

JEDEC is the leading developer of standards for the solid-state industry. However for some, there may be a mist about JEDEC that clouds the what JEDEC really is and really does. The intent of this tutorial was to clarify everyone's understanding of the mission of JEDEC, to show the breadth of JEDEC, and to give the opportunities of service. The focus was on JEDEC 14.2 since this is the JEDEC committee that is responsible for Wafer Level Reliability. Furthermore that focus was on our most recent standards and those currently on our agenda including the update to the Foundry Guidelines.

Towards Understanding Negative Bias Temperature Instability

Tibor Grasser, Technical University of Vienna

Modeling efforts of negative bias temperature instability date back to the work of Jeppson and Svensson in 1977, who proposed the basic form of the popular reaction-diffusion model. This model is still at the heart of many modeling attempts today. However, recent research indicates that even refined variants of this model, while getting some features of NBTI right, cannot capture some crucial aspects of the phenomenon, most notably its ubiquitous logarithmically-decaying recovery phase. Consequently, alternative models have been developed. Some of these models, like the extensions based on dispersive transport of the released hydrogen species, predict like the underlying reaction-diffusion model, that the overall degradation is controlled by (dispersive) diffusion of hydrogen. Alternatively, some models assume that the actual depassivation reaction is the rate limiting step. On top of the creation of interface states, some authors have argued that trapped holes form a considerable part of the overall degradation. Despite all the efforts, however, no universally accepted theory of NBTI is available today, with published models covering only some aspects of the phenomenon and giving contradictory predictions of other aspects. This tutorial attempted to give a broad review of published modeling attempts, comparing their strengths and weaknesses, and eventually listing the requirements for a more complete model of NBTI.

eFuse Design and Reliability

William Tonti, IBM

Programmable eFuse designs present an integration challenge in modern CMOS processing. The power level to program a fuse, and the programming methodologies leverage reliability mechanisms which all other elements in a design avoid. A high degree of eFuse process control and circuit design is required in order to guarantee operation. Almost all eFuse types are one time programmable and are limited to "one chance" programmable. This tutorial discussed selected eFuse technologies describing the design philosophy, electrical programming and characterization, the physics of failure, and some of the many applications an on chip programmable element provides.

Reliability for "Future" Devices

Wilfried Haensch, IBM TJ Watson Research Center

Device design has enjoyed over three decades of scaling leaving the fundamental device architecture basically unchanged. With SiO_2 gate dielectric hovering around 1 nm for the high performance space device engineers looked at different methods than scaling for performance boost. Stress enhancement of mobility is a prime example for a non scaling based performance booster. With the successful implementation of High-k dielectrics there is hope that the path to scaling is opened up again. In spite of the rapid advancement in gate dielectric scaling, most likely fully depleted devices will be needed to continue the density scaling of the past. We discussed some of the challenges and opportunities that are related to the change of device architecture and requirements to continue the trend in integration density. The presentation outlined the path down to the ultimate FET device.