Strained MOSFETs on Ordered SiGe Dots

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***Abstract*— The potential of strained DOTFET technology is demonstrated. This technology uses a SiGe island as a stressor for a Si capping layer, into which the transistor channel is integrated. The structure information is extracted from AFM measurements of fabricated samples. Strain on the upper surface of a 30 nm thick Si layer is in the range of 0.7 %, as supported by finite element calculations. The Ge content in the SiGe island is 30 % on average, showing an increase towards the top of the island. Based on realistic structure information, three-dimensional strain profiles are calculated and device simulations are performed. Up to 15 % enhancement of the NMOS saturation current is predicted.**

I. Introduction

Strain engineering as a means to enhance electronic device performance has become an integral part of contemporary CMOS technology. In addition, novel device architectures have been proposed to improve the way in which strain is induced in the device channel. Schmidt and Eberl proposed to use self-assembled SiGe islands as stressors for Si capping layers [1]. In this way higher strain values can be reached as compared to strained Si grown pseudomorphically on relaxed SiGe buffers.

In this work, the process for growing self-organized SiGe islands is briefly described, followed by an experimental and theoretical assessment of the strain in the capping layer, and a prediction of performance enhancement of n-type FETs integrated in the strained capping layer by means of three-dimensional device simulation.

II. Growth of Regular Arrays of SiGe Islands

The growth procedures are described in detail in [2] and [3]. The samples were grown the on a Si(001) substrate, on which a square pattern of pits with a period of 800 nm had been defined by e-beam lithography, and transferred by reactive ion etching to form pits with a width of 170 nm and a depth of 75 nm. A 36 nm thick Si buffer layer was deposited on the pit-patterned substrates by molecular beam epitaxy, while the substrate temperature was ramped from 450 °C to 550°C. Then the substrates were heated to a growth temperature of 720°C, at which 6 mono-layers of Ge were deposited to form one dome-shaped SiGe island per pit. A Si capping layer of 30 nm thickness was deposited after cooling the substrate to 360°C, to avoid intermixing between the SiGe island and the Si cap. The surface morphology was investigated after each growth step by atomic force microscopy (AFM). Figure 1 shows the AFM image of the final surface of the Si cap, which actually conformally replicates the surface after formation of the SiGe islands. Line scans across several pits and across a single pit are shown in Figure 2, crossing the center of the pits and buried SiGe islands.

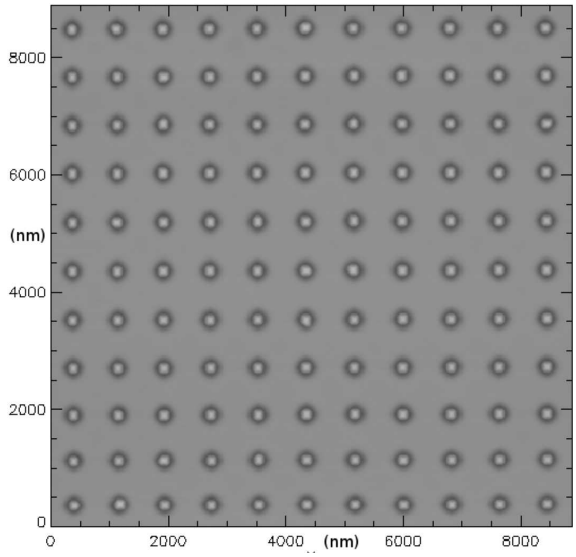

Fig. 1. AFM micrograph of the sample surface after 30 nm of Si cap has been deposited onto SiGe islands grown in pits of a prepatterned Si substrate.

III. Modeling of the Strain Field

The processes of substrate patterning and SiGe island growth have been optimized with respect to subsequent device fabrication. Excellent island ordering, as well as island shape, size, and composition uniformity have been achieved. This optimization has been supported by simulations. Three-dimensional AFM data have been directly imported into a finite element code for strain calculation. In particular, AFM data were taken both after the Si buffer growth (surface of the pit) and after Ge depositions. As compared to the ideal equilibrium shape of islands as reconstructed from facet plots[4], the procedure used here includes more details of the actual structure such as edge rounding and the trench surrounding the island. In the elastic field calculations a Ge content profile in the island has been taken into account with an average Ge content of 0.3. In an iterative procedure the elastic energy is minimized. At the top of the island a higher

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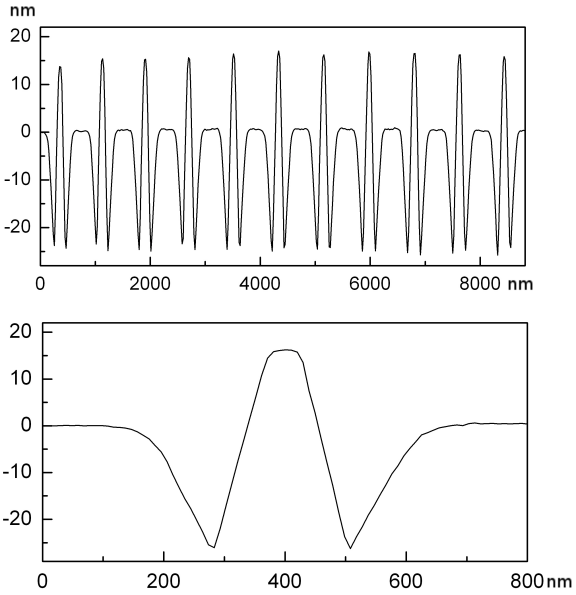

Fig. 2. AFM linescan across the islands indicates the excellent homogeneity of the island array (upper panel). The shape of the cap is shown with high resolution in the lower panel.

Ge content is found, whereas at the lower interface the Ge content is reduced by intermixing with the Si buffer layer. The Si capping layer is deposited at sufficiently low temperature to prevent any significant intermixing of the deposited Si with the SiGe island, so that Ge content profiles can be estimated prior to capping. Then in the whole structure including the capping layer the strain field is calculated using a finite-element code. The sample considered here shows at the upper surface of the 30 nm Si capping layer, where the transistor channel will be integrated, up to 0.7 % biaxial, tensile strain (Fig. 3, Fig. 4, and Fig. 4). This value has also been confirmed by high-resolution X-ray diffraction [5] and Raman spectroscopy in conjunction with simulations [6].

IV. The DOTFET Process

Removing the SiGe island at some stage of the process, a silicon on nothing (SON) device architecture can be realized. In this work, however, we consider a process in which the island is preserved. In this case the thermal budget must be kept sufficiently low to prevent intermixing of Si and Ge between the Si capping layer and the SiGe island. This can be achieved by state-of-the art low-temperature processing, including low-temperature formation of the gate stack and laser annealing of the source/drain implants. A low-complexity, dedicated n-channel MOSFET process has been developed [7].

V. Three-dimensional Device Simulation

With the AFM data of the buffer and the SiGe island surfaces, the geometrical structure has been built. The Si capping layer is treated in the simulation by a conformal deposition. The correct representation of the Si cap is very important since the simulated current is quite sensitive to the strain distribution at the surface. An unstructured mesh is used,

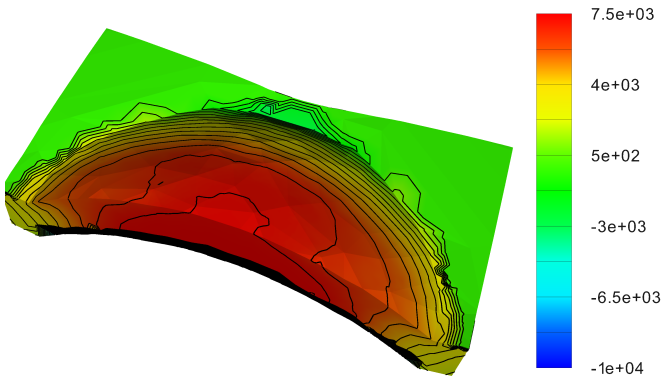

Fig. 3. Strain component e_{xx} (channel length direction) in the Si capping layer.

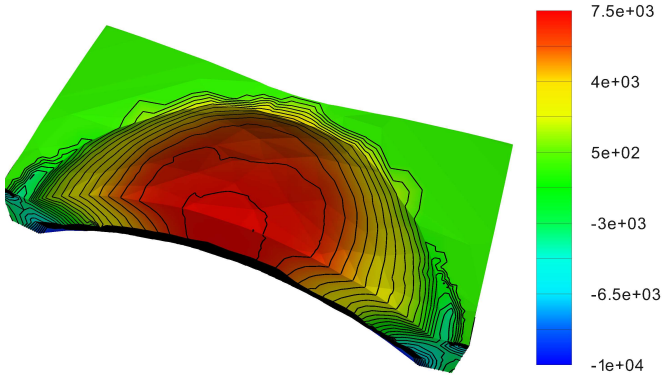

Fig. 4. Strain component e_{yy} (channel width direction) in the Si capping layer.

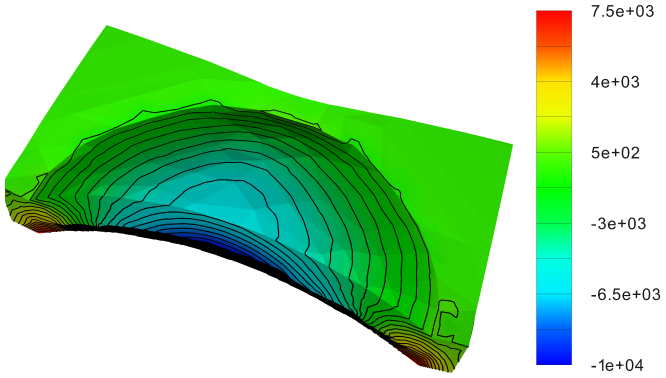

Fig. 5. Strain component e_{zz} (vertical direction) in the Si capping layer.

which has to be sufficiently dense near the surface to resolve the surface inversion layer. On the other hand, in the SiGe island and the underlying Si buffer layer, lower point densities can be used.

A. Structure definition

First the strained Si surface is defined. In a an initial step the set of measured xyz-data points has to be converted to a triangular surface mesh. Due to the high point density of the input data, a smoothing stage with proper element elimination

is applied to these surfaces. Then the three-dimensional mesh generator Netgen [8] is used, which is well suited because of its robust mesh generation technique able to handle the high aspect ratio of gate length/width to gate oxide thickness.

To achieve the desired high mesh density in the channel region a maximum tetrahedron height for the mesh elements in the oxide region is assigned. Neighboring regions will start with these small elements growing towards the outer boundaries. With this technique an appropriate resolution in the channel region is achieved.

The gate stack consists of a 1.5 nm thick oxide and a 60 nm $\times$ 60 nm polysilicon gate. A bulk contact is attached to the Si buffer layer. Source and drain regions are 60 nm wide and approximated by analytical profiles. In Figure 6 the final structure with the simulation mesh is shown. The transistor is cut along its symmetry axis and only one half of the whole structure is analyzed.

In the Si cap layer a constant boron doping of $4\times10^{18}\,\mathrm{cm}^{-3}$ is assumed. Into the access regions from source/drain to the channel an arsenic profile with a maximum doping of $5\times10^{20}\,\mathrm{cm}^{-3}$ is implanted (Figure 7). Finally, the strain profile is interpolated to the device simulation mesh.

B. Electrical Characterization

Three-dimensional device simulations are performed using MINIMOS-NT [9]. The physical models invoked include the strain-dependent low-field mobility model described in [10] and the IMLDA quantum correction model [11]. To determine the strain-induced current enhancement, comparative simulations of the same structure are performed with and without taking the strain effect on the mobility into account.

In Figure 8 the output characteristics for the unstrained and strained device are depicted. The transfer characteristics for drain voltages of 0.05 V and 1.5 V can be seen in Figure 9. Fig. 10 shows the achieved drain current enhancement as a function of the drain voltage. The current enhancement shrinks with growing gate voltage. Due to saturation of the electron velocity this value also shrinks towards higher drain voltages. At $V_{\mathrm{GS}} = 1.5\,\mathrm{V}$, $V_{\mathrm{DS}} = 1.5\,\mathrm{V}$ an enhancement of 15 % can be evaluated.

For comparison, the two-dimensional case shows a current enhancement of 16 % along the axis of the device. Due to the lowered strain values in the peripheral regions under the gate the achieved current enhancement will be reduced. However, as the strain variation under the gate is not too high this difference is marginal. Enlarging the gate width will degrade this situation.

VI. Discussion

A similar technology which utilizes local SiGe stressors has been reported by IBM in 2006 [12]. In this case strain is induced by elastic relaxation of a Si/SiGe bilayer structure. Uniaxial strain of 0.24 % in the Si channel results in a drive current improvement of 15 % [12]. In comparison, the DOTFET process induces a more uniform strain up to 0.7 % in the Si channel. The whole device is integrated in the coherently

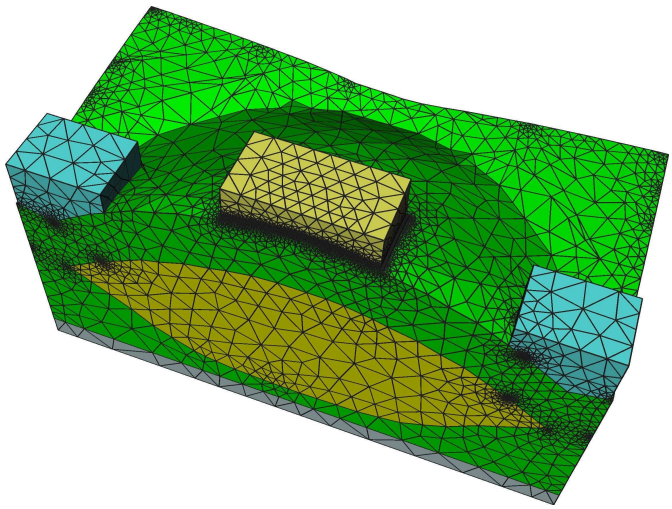

Fig. 6. The geometry of the generated transistor structure. Only one half of the transistor is simulated.

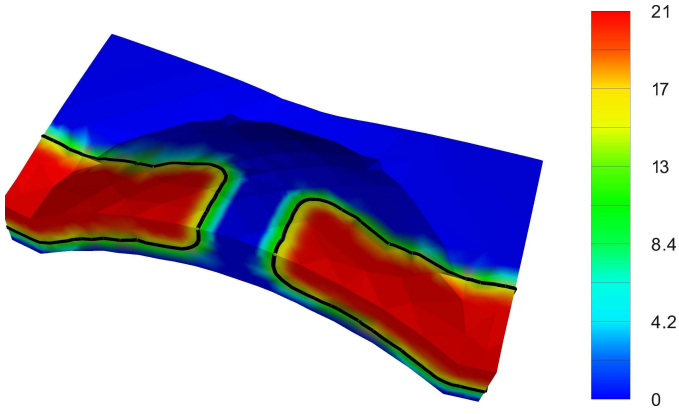

Fig. 7. The Arsenic Doping with shown pn-junction in the capping layer.

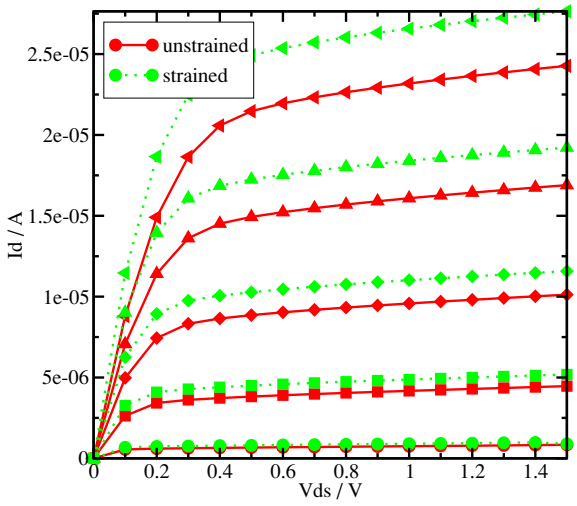

Fig. 8. The unstrained and strained output characteristics for gate voltages of 0.7 V, 0.9 V, 1.1 V, 1.3 V, and 1.5 V are shown.

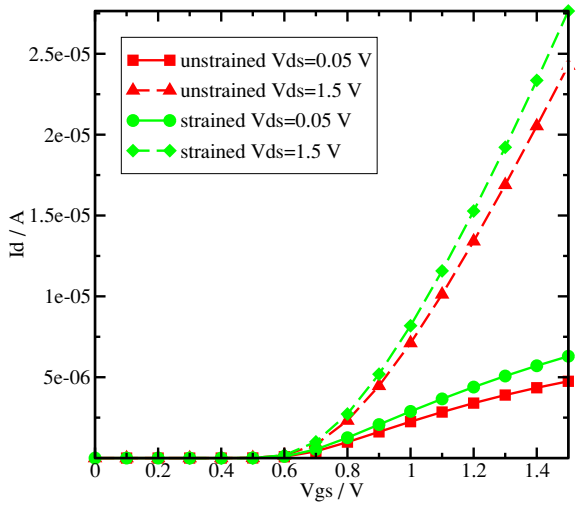

Fig. 9. The unstrained and strained transfer characteristics for drain voltages of 0.05 V and 1.5 V.

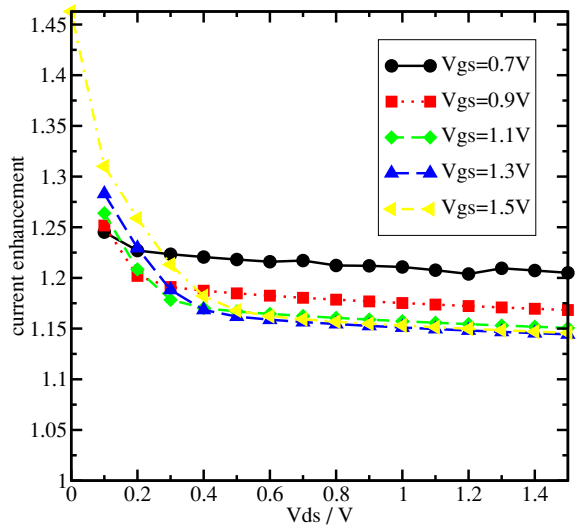

Fig. 10. The current enhancement $I_{\mathrm{D,strained}}/I_{\mathrm{D,unstrained}}$ for several gate voltages.

grown Si capping layer, wheres in the IBM process, source and drain are grown by selective epitaxy. Our simulations predict for the DOTFET the same drive current enhancement as has been reported for the IBM process, despite the strain in the latter is about three times lower (0.24 % versus 0.7 %). This can be partly attributed to different extraction methods for the current enhancement used in [12] and in our simulations. This comparison also indicates that the parameters used in our simulations give a conservative estimate of the current enhancement of the DOTFET.

VII. Conclusion

In this work the potential of the DOTFET has been studied by three-dimensional simulations. The geometry has been extracted from actually fabricated samples. The strain field is obtained by comprehensive simulations verified by strain measurements on the strained Si layer. A conservative estimate for the NMOS drive current enhancement of about 15 % is obtained.

Acknowledgment

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