Hot-carrier (HC) degradation remains one of the most critical reliability issues in MOS transistors. HC degradation is commonly associated with the build-up of traps at the Si/SiO2 interface due to Si-H bond-breakage triggered by “hot” carriers. For non-scaled devices the interface state generation is dominated by a single-particle process while for scaled devices the multiple-particle process dominates [2,3]. Thus even when the device dimensions are extremely scaled the expected halt of degradation is not observed. Therefore, the key issue in the modelling of HC degradation is the information about carrier distribution over energy. We have already presented [3] a model for HC degradation based on a carrier distribution function (DF) evaluation by means of a full-band Mote Carlo device simulator [4]. There, the interface state profiles (the concentration $N_i$ vs. the coordinate along the interface $x$) were already obtained as result of the model and used in our device simulator MINIMOS-NT [5] to simulate output characteristics of degraded devices. However, at that stage we were not yet able to compare the predicted profiles with real $N_i$ profiles obtained for instance by the charge-pumping (CP) technique [6]. This will be done in the following, thereby demonstrating the correctness of our modelling approach.

Low voltage n-MOSFETs fabricated on a standard 0.35 μm technology (Fig. 1) were stressed for $t = 10^5$ s at the gate and drain voltages of $V_{gs} = 2.0$ V and $V_{ds} = 6.75$ V. The chuck temperature was $T = 40$ °C. The experimental transfer characteristics are well reproduced by MINIMOS-NT (Fig. 1, inset).

To obtain experimental $N_i$ profiles a CP technique with a constant base level $V_g$ and varying high level $V_{gh}$ of the gate pulses has been employed [7,8]. The pulse frequency is 25 kHz. Using the approach proposed by Tsuchiya et al [9] we have extracted the dependences of the flat-band $V_b$ and threshold $V_t$ voltages on $x$ for the “fresh” device (Fig. 2, upper inset). The soundness of this approach was checked by calculating these curves with MINIMOS-NT using the widely-adopted routine [6] based on the concept of free electron/hole interface concentration for $V_{th}$ and $V_b$ evaluation. For the extraction of the $N_i$ profiles from CP data we used a standard procedure based on the effective channel length variations when gate pulses are applied [7,8]. The family of $N_i$ profiles for different stress times is depicted in Fig. 3. These profiles demonstrate a peak at the end of the gate electrode shifted respectively the maximum of the electric field (Fig. 2, lower inset).

The experimental $N_i$ profiles are reproduced by our model for interface trap generation [3], Fig. 3. The model is based on the carrier acceleration integral (AI) which is coordinate-dependent and obtained by integrating the DF weighted with the Si-H bond-breakage cross section and the density-of-states over energy. Note that the peak of $N_i$ just coincides with the peak of the AI (not depicted here). The agreement between experiment and theory may be refined by a thorough calculation of the DF with a smaller step by $x$ in the vicinity of the $N_i$ peak.

References: