Analysis of Worst-Case Hot-Carrier Conditions for High Voltage Transistors Based on Full-Band Monte-Carlo Simulations

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***Abstract* – Using a physics-based model for hot-carrier degradation we analyze the worst-case conditions for long-channel transistors of two types: a relatively low voltage n-MOSFET and a high-voltage p-LDMOS. The key issue in the hot-carrier degradation model is the information about the carrier energetical distribution function which allows us to asses the carrier acceleration integral determining the interface state build-up and which controls the interplay between the single- and multiple-carrier mechanisms of Si-H bond rupture. To analyze the worst-case conditions we generate intensity maps, i.e. dependences of some crucial quantities on source–drain $V_{\rm ds}$ and gate $V_{\rm gs}$ stress voltage. These quantities are the boundary of the high-energy tail of the energy distribution function, the interface state generation rate and the total dose of degradation. The difference between positions of severest degradation spots evaluated according different criteria is also plotted as a function of stress voltages. Using these maps we demonstrate that the worst-case conditions are realized at $0.4V_{\rm ds} < V_{\rm gs} < 0.5V_{\rm ds}$ for the n-MOSFET and at the maximal gate current for p-LDMOS. These findings correspond to experimental results published in the literature.**

I. Introduction

The shrinking of device dimensions is accompanied by a change of the worst-case conditions (WCC) for hot-carrier (HC) degradation [1-19]. The electric filed in long-channel/high voltage (HV) devices is rather high and thus severe heating of carriers in the channel occurs. As a result, already a single particle has sufficiently high energy to rupture a silicon-hydrogen bond at the interface. Further we designate this component of Si-H bond-breakage as a single-particle (SP) mechanism. To be concrete, the WCC for HV n-channel device are realized to the following interrelation between source–drain ($V_{\rm ds}$) and gate ($V_{\rm gs}$) voltages: $0.4V_{\rm ds} < V_{\rm gs} < 0.5V_{\rm ds}$. This case corresponds to the maximal substrate current or – in other words – to the largest impact ionization rate [1-4]. For HV p-MOSFETs the WCC are reached at the maximal gate current and there is no such an empirical law for this case [5-7].

At those operation/stress voltages typical for low voltage (LV) devices, a carrier unlikely can trigger the SP-process. It is worth mentioning that the process of energy interchange between carriers is statistical and therefore one may expect that a certain fraction of particles – even small – is characterized by relatively high energy. As a consequence, particles able to launch the SP-mechanism are in principle present, but their portion in the ensemble is rather small. To summarize, the change of the bond rupture mechanism for LV/scaled devices is assumed [8,9]. A Si-H bond is being broken via a consequent excitation of its vibrational modes by a series of particles. These particles have sufficiently low energies and their number impinging the interface per time unit is more critical rather than their averaged energy. Thus, the WCC for the devices of this class are realized when the carrier flux is maximal. For LV n-MOSFETs as well as for p-MOSFETs this scenario corresponds to the equality of the source–drain and gate voltages ($V_{\rm gs} = V_{\rm ds}$) [10-12,13-15].

There is a considerable number of papers published in the literature devoted to the detailed analysis of hot-carrier degradation worst-case conditions for long-channel and/or high voltage transistors as well as for scaled low voltage devices employed in logic applications [1-20]. These papers provide us with a rather detailed experimental study of this matter, but the reliable microscopic picture of the problem is still missing. Such a picture is to be developed within the framework of a HC degradation model based on information how carriers are distributed over energy and thus considering statistical information of "hot" and "colder" carriers for certain device architecture. However, the model of this kind - as far as we know - is still under development.

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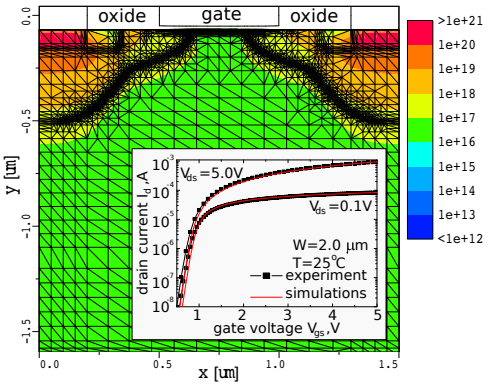

Fig. 1. The topology of n-MOS with donor profile (P) highlighted. Inset: $I_{\rm ds} - V_{\rm gs}$ experimental characteristics vs. simulated ones.

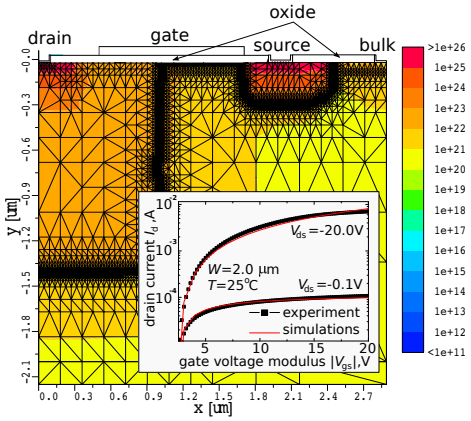

Fig. 2. The topology of HV p-LDMOS with acceptor profile (B and As) highlighted. Inset: $I_{\rm ds} - V_{\rm gs}$ experimental characteristics vs. simulated ones.

In this work we employ our HC degradation model presented in the accompanying abstract [21] to determine of the WCC conditions for devices of different types, namely for a relatively low-voltage (operation voltage of 5 V) long-channel n-MOS transistor and for a HV p-LDMOS. The model is based on precise calculations of the carrier energy distribution function (DF) using a full-band Monte-Carlo device simulator and therefore considering the "fractions" of the carriers responsible for the SP- and MP-mechanisms. This model allows us to establish a microscopic pattern of the issue.

II. Devices

For this work we used two types of devices. The first one is a (relatively) low voltage n-MOSFET fabricated on a standard 0.35 μm CMOS technology and represented in Fig. 1. The device operation voltage $V_{\rm ds}$ is 5V and the large channel length of 0.5 μm ensures that the single-particle mechanism is responsible for the HC degradation. The second device is a HV p-LDMOS with simplified geometry (flattened interface and absence of the shallow trench isolation fragment, see Fig. 2). The operation voltage of this transistor is $V_{\rm ds} = -20$ V.

For modeling the device characteristics we have employed simultaneously two device simulators, namely the device and circuit simulator MINIMOS-NT [22] used within the Global TCAD Solutions framework [23] and the full-band Monte-Carlo device simulator MONJU [24]. MONJU is primarily used for the calculation of the distribution function. We verified our simulation tools by comparing the experimental transistor transfer characteristics with the simulated ones. Insets of Fig. 1 and Fig. 2 demonstrate good agreement between the experiment and theory.

III. Hot-Carrier Acceleration Integral

Both single-particle and multiple-particle (MP) components are controlled by integrals that have the same functional structure [18,19,25]; for the SP-component this integral just represents the interface state generation rate:

$$R_{\rm SP} = \nu_{\rm SP} \int_{E_{\rm th}}^{\infty} f(E) g(E) \sigma(E) v(E) dE. \qquad (1)$$

Equation (1) has the same structure as the impact ionization rate (see [18,19]) differing only in the reaction cross section $\sigma(E)$. It includes the carrier distribution function over energy $f(E)$, the density-of-states $g(E)$ and the carrier velocity $v(E)$.

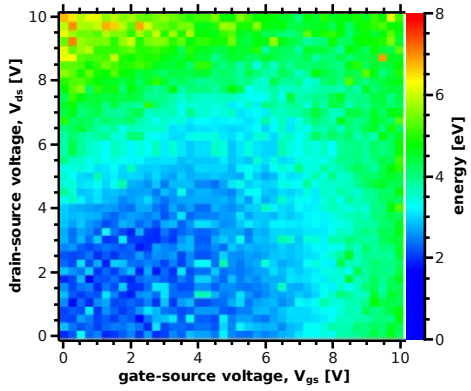

Fig. 3. The boundary of the DF high-energy tails as a function of $V_{\rm ds}$ and $V_{\rm gs}$ for n-MOS.

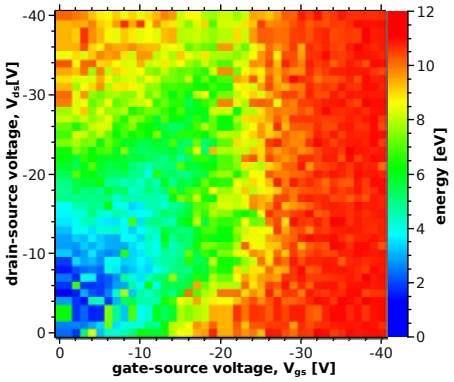

Fig. 4. The boundary of the DF high-energy tails as a function of $V_{\rm ds}$ and $V_{\rm gs}$ for p-LDMOS.

For the case of Si-H bond-breakage, the capture cross section has the same functional form as for impact ionization, i.e. $\sigma = \sigma_0(E - E_{\text{th}})^p$, but different parameter values, i.e. exponent $p = 11$, threshold energy $E_{\text{th}} = 1.5$ eV [19], and prefactor σ_0 (in this model σ_0 is a fitting parameter; actually the product of σ_0 and the attempt rate ν_{SP} acts as a generalized parameter).

Employing (1) we solve the interface trap generation equation $\mathrm{d}N/\mathrm{d}t = R_{\text{SP}}\,(N - N_0)$ and thus obtain the time dependence of trap density:

$$N(t) = N_0(1 - \exp(-R_{\text{SP}}t)), \tag{2}$$

with the initial number of passivated bonds N_0.

In this work we do not consider the MP-related contribution since for these long channel and/or HV devices the SP-process is the dominant one [18-20]. Moreover, the carrier acceleration integral in the form (1) contributes to the generation rate triggered by the MP-process in a more sophisticated manner [18-20] and the rate is not so sensitive to this factor. To summarize, the integral (1) controls the HC degradation and in the next section we will analyze its features for selected devices.

IV. Results and Discussion

Fig. 3 and 4 depict how energetically deep the DF (for minority carriers) extends for the n-MOS and the p-LDMOS, respectively. All the positions along the interface are probed for each pair of source–drain and gate voltages and the maximal energy E_{tail} is plotted vs. $\{V_{\text{ds}}, V_{\text{gs}}\}$. Note that the high energy tails are noisy due to the statistical nature of the Monte-Carlo approach and thus we assume that the DF ends if its value differs by 8 orders of magnitude from the maximal one (see Fig. 5). One may also employ another strategy when the boundary energy E_{tail} is understood as the energy at which the cumulative probability does not increase any more, i.e. when the integral $F(E) = \int_0^E F(\tilde{E})d\tilde{E}$ saturates.

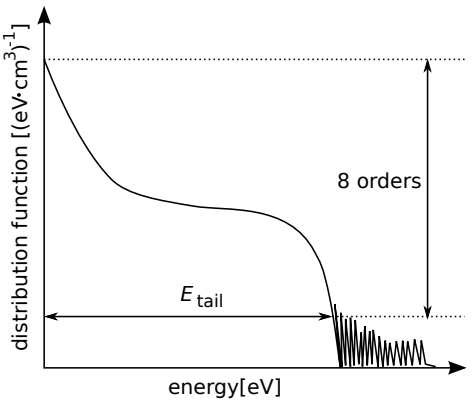

Fig. 5. The scheme representing calculations of E_{tail}.

This approach is controlled by a tolerance parameter Δ (E_{tail} corresponds to the energy when $F(E)$ reaches $1 - \Delta$) and complicates the matter especially taking into account that the results obtained using these different criteria are practically the same. Fig. 3,4 are accompanied by Fig. 6,7 providing positions in the channel of these high-energy tails for the same devices. The source position is assigned to the origin of the x-axis. One can see that the worst-case conditions are really reached at the conditions described in Introduction. Actually, for n-MOS the blue spot in Fig. 3 transforms to the green area starting at $V_{\text{ds}} \approx 8$ V and $V_{\text{gs}} \approx 4$ V. Fig. 4 demonstrate that the green spot becomes transforming to the yellow area at $V_{\text{gs}} \approx 5$ V and $V_{\text{ds}} \approx$ 20-25 V. The measurement of the gate current I_{g} vs. V_{gs} at a fixed V_{ds} of 20 V showed that I_{g} peaks at V_{gs}=5 V. Therefore, this simulated map confirms the tendency that for the case of a p-LDMOS the WCC are realized at maximal I_{g}.

The integrand in (1) includes the strongly reducing function $f(E)$ and the competently increasing combination $g(E)\sigma(E)v(E)$. At the same time the shape of the energy distribution function as a whole changes (see our accompanying abstract [21]) and thus the maximum of R_{SP} is shifted away from E_{tail}. Fig. 8-9 demonstrate diagrams $R_{\text{SP,max}}$ vs. $\{V_{\text{ds}}, V_{\text{gs}}\}$. Note that the integrals are presented in arbitrary units, i.e. accurate within the factor $\sigma_0\nu_{\text{SP}}$ (the calibration of the model according to real degradation data lies out of the scope of this work).

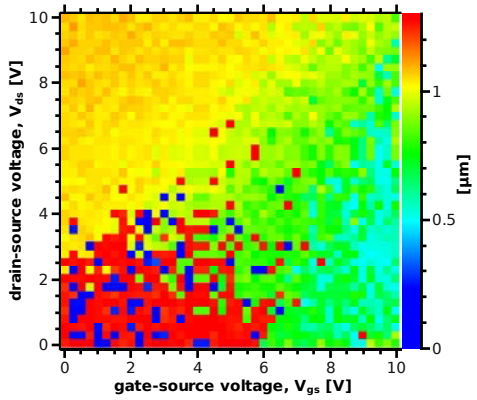

Fig. 6. Spatial position of the high-energy tails depicted in Fig. 3.

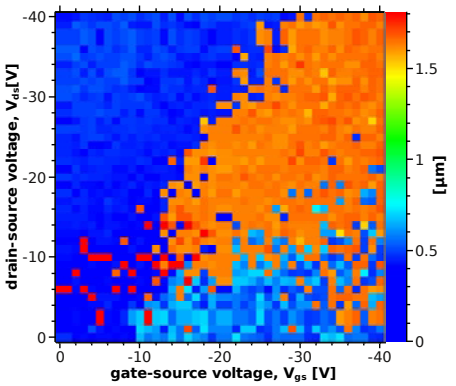

Fig. 7. Spatial position of the high-energy tails depicted in Fig. 4.

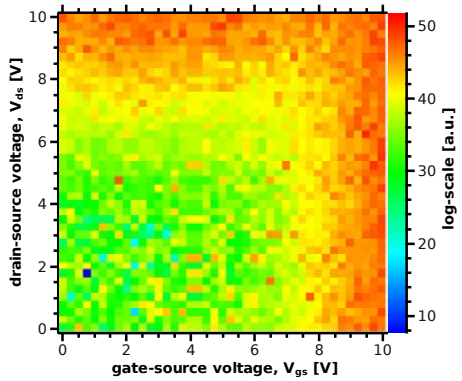

Fig. 8. Maximum of R_{SP} for n-MOS as a function of V_{ds} and V_{gs}.

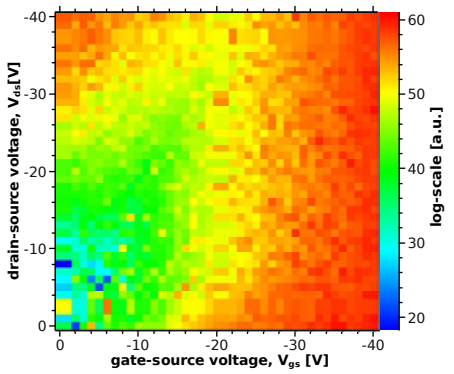

Fig. 9. Maximum of R_{SP} for p-LDMOS as a function of V_{ds} and V_{gs}.

As it was repeatedly discussed in the literature, not only the amount of interface traps generated during the stress is important but also their spatial distribution, see e.g. [26,27]. Moreover, the device life-time may be estimated using different device characteristic degradation, e.g. the threshold voltage, transconductance and linear drain current, etc. But the prevalent portion of degradation of different parameters is controlled by traps located in different position along the interface [26,27]. For this reason, it is worth plotting also $R_{\mathrm{SP,max}}$ integrated along the SiO_2/Si interface and proportional to the total amount of damage, see Fig. 10-11.

Comparing the pairs of figures $\{3,4\}$ with $\{6,7\}$ and vs. $\{10,11\}$ one concludes the same tendency, i.e. consideration of the WCC based on the total degradation dose provides us with the same results as criteria employing E_{tail} and $R_{\mathrm{SP,max}}$ It is also worth plotting the shift of the geometrical positions of the severest degradation spot evaluated according to strategies based on diverse HC parameters. Fig. 12 and 13 demonstrate the distance between those spots related to the most extended high-energy tail of the DF and that obtained finding the maximum generation rate (schematically explained in Fig.14). In the case of the p-LDMOS one can see a rather huge difference between these positions up to $\sim 1\mu$m. The reason of such a behavior is to be explained taking in mind that not only E_{tail} varies along the interface, but also the DF changes its shape. Analyzing the structure of (1) one can see that the main contribution to the acceleration integral is made at energies less than E_{tail} (due to competing tendencies $f(E)$ vs. $g(E)\sigma(E)v(E)$) and therefore such a shift becomes clear (see Fig.15). To summarize, Fig. 13 demonstrates that the estimation of the WCC employing E_{tail}-related criterion is not valid and one should deal with the acceleration integral.

V. Conclusion

We have analyzed the worst-case conditions for two types of devices, namely, for a relatively LV n-MOSFET and a HV p-LDMOS, using the hot-carrier degradation model based on calculations of the carrier distribution function by means of a full-band Monte-Carlo device simulator. Both single-particle and multiple-particle mechanisms of Si-H bond-breakage are firmly linked to the carrier acceleration integral controlled by the distribution function. The structure of the integrand herein contains a superposition of rapidly decaying high-energy tails of the distribution function and a fast increasing combination of capture cross section, carrier velocity, and the density-of-states. Therefore, the maximum of this integral is shifted with respective to the position where the DF demonstrates deepest high-energy tails.

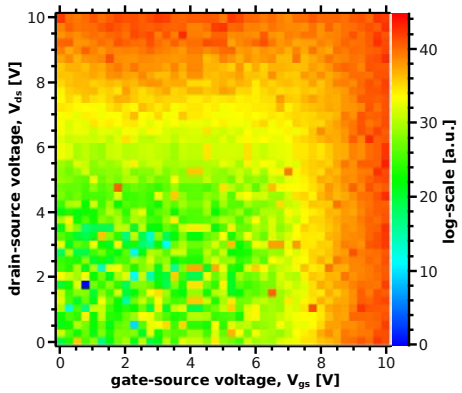

Fig. 10. Maximum of total degradation dose for n-MOS as a function of V_{ds} and V_{gs}.

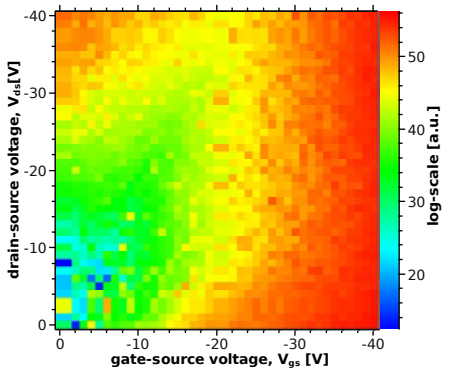

Fig. 11. Maximum of total degradation dose for p-LDMOS as a function of V_{ds} and V_{gs}.

For the analysis of the worst-case condition for HC degradation we used several criteria: the boundary energy of high-energy tail of the DF, the acceleration integral (which gives the SP-process rate) and the total dose of degradation. These quantities are mapped vs. stress source–drain and gate voltages. Analyzing these maps we concluded that for n-MOSFETs the worst-case conditions are realized if the following interrelation between voltages is satisfied: $0.4V_{\rm ds} < V_{\rm gs} < 0.5V_{\rm ds}$; in contrast for p-LDMOS the severest HC degradation corresponds to the maximal gate current. This detailed picture agrees with the empirical concept concerning the HC degradation worst-case conditions documented in literature.

Note that the severest HC degradation spots corresponding to different criteria are shifted geometrically with respective to each other and this distance in the channel is also analyzed and plotted as a function of $V_{\rm ds}$ and $V_{\rm gs}$. One can see that in the case of the p-LDMOS the WCC conditions related to criteria of the deepest high-energy tail and the maximal interface trap generation rate are separated by $\sim 1\mu$m. Such a behavior proves that the acceleration integral rather than the boundary energy should be considered.

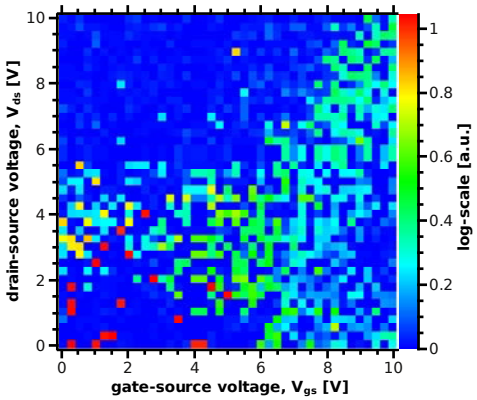

Fig. 12. Difference between positions of $E_{\rm tail}$ and $R_{\rm SP,max}$ vs. $V_{\rm ds}$ and $V_{\rm gs}$ for n-MOS.

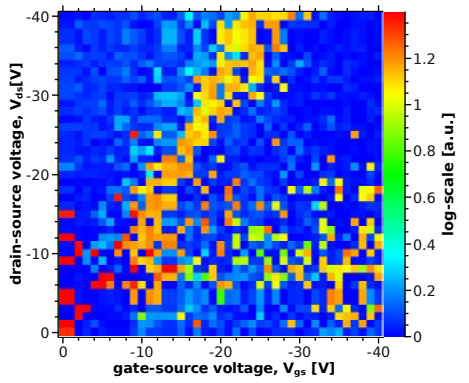

Fig. 13. Difference between positions of $E_{\rm tail}$ and $R_{\rm SP,max}$ vs. $V_{\rm ds}$ and $V_{\rm gs}$ for p-LDMOS.

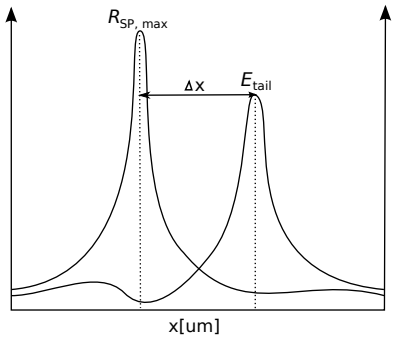

Fig. 14. Difference in positions of $R_{\rm SP,max}$ and $E_{\rm tail}$ shift Δx.

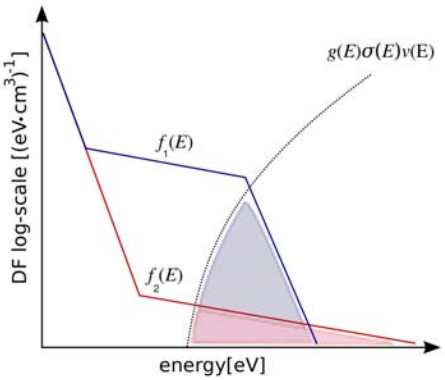

Fig. 15. Impact of the DF shape on the carrier acceleration integral.

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