On the Recoverable and Permanent Components of Hot Carrier and NBTI in Si pMOSFETs and their Implications in Si$_{0.45}$Ge$_{0.55}$ pMOSFETs

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Abstract—The introduction of SiGe channel pMOSFETs for high mobility devices is expected to enhance the impact ionization phenomenon, making it necessary to study Hot Carrier (HC) degradation also for the p-channel MOSFET reliability. The study of pure HC effects on pMOSFETs is complicated due to the mixing with Negative Bias Temperature Instability (NBTI). In the first part of this work the interaction of the two degradation mechanisms is studied thoroughly on Si devices with the extended measure-stress-measure (eMSM) technique which is capable of capturing both the charge trapping and the interface state creation components of the degradation. HC degradation is shown to enhance interface state creation, while eventually reducing the charge trapping w.r.t. standard NBTI. These experimental results are supported by MEDICI simulations. The second part of the paper focuses on the HC reliability of Si$_{0.45}$Ge$_{0.55}$ pMOSFETs. These devices show enhanced degradation w.r.t. their Si counterparts, confirming the importance of studying HC effects for the reliability of this technology. Nevertheless, the SiGe device reliability can be enhanced when reducing the thickness of the Si cap.

Keywords: Hot Carrier, Negative Bias Temperature Instability, pMOSFETs, SiON, poly-Si, high-k, metal gate, SiGe, Si cap.

I. INTRODUCTION

Hot Carrier (HC) degradation is generally considered a major reliability issue for nMOSFET [1], while the pMOSFET reliability is jeopardized by Negative Bias Temperature Instability (NBTI) [2]. Incorporation of Ge into Si substrate for high-mobility devices, which is considered as one of the most promising options to further improve CMOS performance [3], has been shown to improve NBTI reliability [4-6], while enhancing HC effects due to higher impact ionization caused by the smaller bandgap of Ge [7-9]. In this scenario, both HC and NBTI need to be considered for the pMOSFET reliability.

Furthermore, a typical HC test implies the application of high bias on both the drain and the gate terminals (Channel HC, HC) [1]: in such a case, while the oxide at the drain side of the channel experiences the effects of HC caused by the high lateral electric field ('hot hole' injection), the source side still experiences only the high oxide electric field (E$_{ox}$) due to the applied gate voltage ('cold holes' injection), resulting in a typical NBTI stress condition [2]. It is hence necessary to study the interplay of these two degradation mechanisms to properly assess the pMOS reliability.

In this work, this study is performed firstly on Si/SiON/poly-Si devices (section III). The experimental results are then validated on a more recent high-k/metal gate technology (section IV) and then further applied to the study of novel Si$_{0.45}$Ge$_{0.55}$ pMOSFETs (section V).

II. EXPERIMENTAL

Three different set of samples are used in this work. Firstly, the interaction between HC and NBTI is studied on Si pMOSFETs with a SiON dielectric (~1.65nm), a poly-Si gate, and a channel length L≈150nm. To validate the results on a more recent technology, Si high-k/metal gate devices are also used. For these samples the gate stack consists of a SiO$_2$ interfacial layer (~0.8nm) and a HfO$_2$ (~2nm) high-k layer. Channel length is L≈70nm in this case. Finally, SiGe pMOSFETs with a buried channel architecture are studied. Ge fraction in the channel is x=0.55, while the gate stack consists of a Si cap of varying thickness (0.65–2nm), a SiO$_2$ interfacial
layer (~0.8nm) and a HfO₂ (~1.8nm) high-k layer. Channel length is \( L \approx 70\)nm also in this case. More details on this process can be found in [3].

To compare the effect of NBTI and CHC on pMOS, stress experiments were performed by applying the stress voltage only to the gate for NBTI and to both the gate and the drain for CHC. Since HC effects are only weakly dependent on the temperature (T) [1], while NBTI is strongly T-activated [2], experiments were performed at 125°C (unless otherwise stated). The extended Measure-Stress-Measure technique (eMSM) [10] is used to capture both the so-called ‘recoverable’ (\( R \)) component of the threshold voltage shift \( (\Delta V_{\text{th}}) \), ascribed to the charging of pre-existing oxide defects during stress \( (\Delta N_{\text{ox}}) \), and the ‘permanent’ (\( P \)) or ‘slowly-relaxing’ one, typically associated with the creation of new interface states \( (\Delta N_{\text{it}}) \) [10,11].

A typical set of relaxation curves obtained with the eMSM technique for NBTI and CHC stress conditions on Si/SiON samples is shown in Fig. 1.

The eMSM data analysis technique developed previously for NBTI [10,11] is employed in this work also for the CHC stress conditions. Using this technique, based on the previously observed universality of NBTI relaxation, the measured \( \Delta V_{\text{th}} \) (\( t_{\text{stress,i}}, t_{\text{relax}} \)) are empirically separated into the \( R \) and \( P \) components, i.e.,

\[
\Delta V_{\text{th}} \left( t_{\text{stress,i}}, t_{\text{relax}} \right) = R \left( t_{\text{stress,i}}, t_{\text{relax}} \right) + P \left( t_{\text{stress,i}} \right) .
\] (1)

Here, \( t_{\text{stress,i}} \) represents the total stress time after the i-th stress phase, while \( t_{\text{relax}} \) stands for the time elapsed from the beginning of the last relaxation phase. According to the previous observations [10,11], all the relaxation data obtained at different stress times fall on the same curve, given by the universal relaxation function \( r(\xi) \), where \( \xi = t_{\text{relax}} / t_{\text{stress,i}} \) is the universal relaxation time. Very good fits to experimental data have been obtained in literature using the empirical relation:

\[
r(\xi) = \frac{1}{1 + B \xi^\beta} \] [11]. (2)

Therefore the relaxation of the recoverable part of the damage can be described as:

\[
R \left( t_{\text{stress,i}}, t_{\text{relax}} \right) = R \left( t_{\text{stress,i}}, t_{\text{relax}} = 0 \right) \cdot r \left( 0 \right) ,
\] (3)

where \( R \left( t_{\text{stress,i}}, t_{\text{relax}} = 0 \right) \) represents the “full” \( R \) component extrapolated to \( t_{\text{relax}} = 0 \), as if it were measured with zero delay after stress removal. Thus it is possible to estimate the total \( R \) from standard delayed measurements.

Conversely, the \( P \) component (i.e., \( P \left( t_{\text{stress,i}} \right) \) in eq. (1) ) is defined as the damage which would be ideally still measured after an infinite time from stress removal, since \( R \left( t_{\text{stress,i}}, t_{\text{relax}} = \infty \right) = 0 \) (see eqs. (2) and (3), [11]).

Interestingly, the universality of the relaxation is observed to be valid also for CHC stress on pMOSFETs, as shown in Fig. 2 for a stress voltage of, e.g., -2.2V. The same observation can be made for each of the considered stress voltages.

III. RESULTS AND DISCUSSION ON SI/SION/POLY-SI

As shown in Fig. 3, the CHC stress condition resulted in a reduced \( R \) and enhanced \( P \) w.r.t. NBTI. While the reduction of \( R \) is constant for a wide range of \( V_{\text{stress}} \) (~1.5x), the \( P \) enhancement is observed only at high \( V_{\text{stress}} \) (Fig. 4). These two experimental observations are discussed and interpreted individually in the following paragraphs.
A. Recoverable Component

The reduction of $R$ can be related to the $E_{ox}$ reduction at the drain side of the channel due to the high $|V_{D}|$, i.e. reduction of the residual NBTI effects (‘cold holes’) in that region. To support this hypothesis, the $E_{ox}$ profile along the channel was simulated with MEDICI for both the CHC and NBTI stress conditions as reported in Fig. 5a. Using the experimental dependence of $R$ on $E_{ox}$ (inset of Fig. 5a, replotted from the data in Fig. 4), the $E_{ox}$ profile can be converted into the local $\Delta V_{th}$ expected to be caused solely by the $R$ component ($\Delta V_{th,R}$) after a fixed stress time, and therefore into local trapped charge, $\Delta N_{ot}$ (Fig. 5b). While for the NBTI stress the $\Delta N_{ot}$ profile along the channel is constant, the profile for the HC case is decreasing almost linearly toward the drain. The $\Delta N_{ot}$ charge profiles are then inserted into the simulated Si/SiON/poly-Si device structures and $I_{D}V_{G}$ curves are calculated (Fig. 6). In agreement with the experimental observation, the charge trapping ($R$) component during a NBTI stress is confirmed to cause increased $\Delta V_{th}$ w.r.t. a CHC stress, with the ratio of the two shifts well matching the experimentally observed ratio of the $R$ components after NBTI and CHC (1.87x vs. 1.5x in Fig. 4). We can therefore conclude that the reduction of the charge trapping component during CHC stress can be indeed explained by the reduction of the oxide electric field along the channel caused by the application of the drain stress bias.

Figure 3. Si/SiON: CHC is observed to cause reduced $R$ w.r.t NBTI. These two observations are attributed to a reduced $E_{ox}$ at the drain side of the channel, and to an enhanced $\Delta N_{ot}$, respectively.

Figure 4. Power law pre-factors for CHC and NBTI: while the reduction of $R$ (~1.5x) is constant for a wide range of $V_{stress}$, the $P$ enhancement is observed only at high $V_{stress}$. The inset reports the extracted power law exponents.

A.4.3

Figure 5. (a) $E_{ox}$ profile along the channel from MEDICI simulations for the CHC and NBTI stress conditions ($E_{ox}$ magnitude is slightly overestimated by neglecting poly depletion and quantum mechanical effects). Using the experimental dependence of $R$ on $E_{ox}$ (inset), the $E_{ox}$ profile can be converted into (b) the local $\Delta V_{th}$ expected to be caused solely by the $R$ component ($\Delta V_{th,R}$), and therefore into the local $\Delta N_{ot}$ to be inserted into the simulated structure (see Fig. 6).

Figure 6. $I_{D}V_{G}$ curves simulated in MEDICI before and after inserting the $\Delta N_{ot}$ charge profiles from Fig. 5b: in agreement with the experimental observation, CHC stress causes reduced $\Delta V_{th}$ w.r.t. NBTI.
B. Permanent Component

The enhancement of the P component can be interpreted as enhanced $\Delta N_0$ due to pure HC effects ('hot holes'). To support this hypothesis, a substrate hot hole injection experiment [12] was performed: a diode next to the device was used to inject hot holes into the channel, while their energy was provided by applying a positive bias to the substrate of the pFET (Fig. 7). In this experiment, HC degradation is distributed uniformly over the whole channel length and, since no drain voltage is applied, $E_{ox}$ is kept constant along the channel. Results in Fig. 8 for different injection current levels confirm that pure HC stress causes only P enhancement, while R is unaffected and caused by residual NBTI due to $E_{ox}$, as seen in the previous paragraph.

The P enhancement during standard CHC stress can be attributed to increased $N_d$ creation near the drain due to the peak in the lateral electric field, shown in Fig. 9 as from MEDICI simulations. To show this, lateral $N_d$ profiling was performed with the charge pumping (CP) method of [13], where CP current ($I_{CP}$) contribution from the interface regions above the junctions is controlled by applying a reverse bias to source and drain. Results in Fig. 10 show that while NBTI stress creates $N_d$ uniformly, CHC stress enhances $N_d$ especially near the drain (higher slope of $I_{CP}$ vs. reverse junction bias).

From the results discussed above we can conclude that the residual NBTI at the source side of the channel ('cold holes') strongly contributes to the total CHC degradation on pMOSFETs, while the pure HC effects ('hot holes') are mainly responsible for the interface state creation at the drain side, as for nMOSFETs [1].
minimizing impact ionization and thanks to the high valence band offset between Si and SiO₂ [1]. This is shown in Fig. 11 also for a Si/SiO₂/high-k/metal gate (MG) device, confirming that CHC do not jeopardize the Si pMOSFET reliability, which is mainly limited by NBTI [14-16].

V. RESULTS ON Si₀.₄₅Ge₀.₅₅/Si/SiO₂/HIGH-K/MG

Higher impact ionization in novel SiGe channel pFETs [7] can change this scenario. Fig. 12a shows the same comparison between NBTI and CHC on a Si₀.₄₅Ge₀.₅₅ device. For low stress voltages, a reduction of the total ΔVₘ was still observed for the CHC case. Relying on the discussion in the previous sections, this observation can be interpreted as follows: in a regime for which R dominates over P (i.e., low stress voltages and/or short stress time), the R reduction obtained when applying also a drain stress bias directly reflects into a reduced total ΔVₘ. On the other hand, for higher stress voltages, enhanced ΔNᵢ related to pure HC effects (‘hot holes’), causes additional ΔVₘ and therefore CHC degradation matches and eventually dominates over NBTI (triangles in Fig. 12a).

A comparison between CHC stress on SiGe and on Si devices with identical high-k/MG gate stacks is also undertaken. It should be noted that due to the known Si cap penalty [3], the SiGe device shows higher capacitance equivalent thickness in inversion (T_inv) w.r.t. its Si counterpart. Moreover incorporation of Ge reduces the initial Vₜₜ₀ [3]. For a fair comparison it is therefore necessary to ‘match’ the stress conditions, artificially ‘equalizing’ the stress time, and to rescale ΔVₘ to equivalent total charge density (ΔN_eff = ΔNᵢ + ΔNᵦ = ΔVₘ/Cox/q) in order to account for different Cox. Similarly to Fig. 12a, results in Fig. 12b show that, for low stress voltages where R dominates, SiGe devices experience a reduced ΔVₘ (confirming to suffer reduced charge trapping w.r.t. Si devices, [5-6]), while for high stress voltages enhanced ΔNᵦ from pure HC effects causes higher ΔVₘ on SiGe.

We have recently shown that NBTI reliability of SiGe pFETs can be optimized by reducing the thickness of the Si cap [5-6]. It is therefore interesting to study the impact of the Si cap thickness also on the CHC reliability. It is important to highlight once again that, with the Si cap thickness affecting both the T_inv and the Vₜₜ₀ of the SiGe devices, for a fair comparison it is necessary to carefully ‘equalize’ the stress conditions as described above. Results in Fig. 13 show that a reduced Si cap thickness is also extremely beneficial against CHC degradation, remarkably reducing ΔNᵦ.

As for NBTI, a possible explanation is related to the higher Ge segregation observed with Secondary Ion Mass Spectroscopy (SIMS) at the Si cap/SiO₂ interface for thin Si cap [17,18]. As observed with Electron Spin Resonance (ESR) [19,20], a higher Ge content at the interface can lower the H-passivated Si dangling bonds density which are commonly considered as the interface state precursor defects [6]. Moreover, as one can notice in Fig. 13, a thin Si cap reduced also the ratio ΔN_eff/ΔNᵦ, revealing also a reduction of R. This reduced ΔNᵦ can be related to a favorable alignment shift of the Fermi level in the SiGe channel w.r.t. the valence band.
edge of the Si cap at the oxide interface which can reduce the carrier interaction with N_{ox} as we discussed in [6].

VI. CONCLUSIONS

The introduction of SiGe channel devices makes it necessary to study Hot Carrier (HC) degradation also for the pMOSFET reliability. A channel HC (CHC) degradation study on Si pMOSFETs was presented and compared to standard NBTI. The CHC stress condition was shown to reduce the charge trapping component of the degradation (the ‘recoverable’ component, ΔN_{dr}) due to reduced oxide electric field at the drain side of the channel (i.e., reduced ‘cold hole injection’). On the other hand, similarly to nMOSFETs, CHC is shown to enhance the interface state creation (the ‘permanent’ component, ΔN_{it}) at the drain side of the channel due to the high lateral electric field (i.e., ‘hot hole injection’).

These experimental results were well supported by MEDICI simulations. Since ΔN_{it} is the main contribution to the total degradation, and since ΔN_{dr} is significantly reduced for a CHC stress w.r.t. NBTI, these results confirm that CHC do not limit the Si pMOSFET reliability.

However, Si_{0.45}Ge_{0.55} pMOSFETs show enhanced CHC degradation w.r.t. their Si counterparts, confirming the importance of studying HC effects for the reliability of this technology. Nevertheless, the SiGe device reliability can be enhanced when reducing the thickness of the Si cap. Such optimization is shown to reduce both ΔN_{it} and ΔN_{dr}.

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