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Efficient AlGaN/GaN Linear and Digital-Switch-Mode Power Amplifiers for Operation at 2 GHz*

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SUMMARY This work addresses the enormous efficiency and linearity potential of optimized AlGaN/GaN high-electron mobility transistors (HEMT) in conventional Doherty linear base-station amplifiers at 2.7 GHz. Supported by physical device simulation, the work further elaborates on the use of AlGaN/GaN HEMTs in high-speed current-switch-mode class-D (CMCD)/class-S MMICs for data rates of up to 8 Gbit/s equivalent to 2 GHz RF-operation. The device needs for switch-mode operation are derived and verified by MMIC results in class-S and class-D operation. To the authors' knowledge, this is the first time 2 GHz-equivalent digital-switch-mode RF-operation is demonstrated with GaN HEMTs with high efficiency.

key words: *Gallium Nitride, power amplifier, switch-mode, efficiency*

1. Introduction

Energy harvesting is a key issue in the development of green information and communication technology. Energy efficiency is further a vital prerequisite in order to make use of the astounding electrical RF-power potential of group III-Nitride semiconductor devices in real communication systems [1]. III-Nitride high-electron mobility transistors (HEMTs) enable new amplifier concepts at RF-frequencies based on their increased device speed and ruggedness and the unique combination of speed and high breakdown voltage. Very high efficiency values can be achieved with conventional linearized Doherty amplifiers, as shown in this work. In addition, new III-N amplifier can be part of more advanced transceiver concepts, as depicted in Fig. 1. The aim of this work is to harvest efficiency and to reduce component usage in the chain from the digital output-I/Q of any communication system. The schematic of the transceiver chain in a base station is given in Fig. 1. The potential advantage of using switch-mode amplifiers is a more efficient organization from the I/Q-output of the digital signal processing (DSP) to the analog antenna output. The early D/A-conversion can be avoided and the digital signal is maintained up to the power amplifier potentially allowing for increased efficiency.

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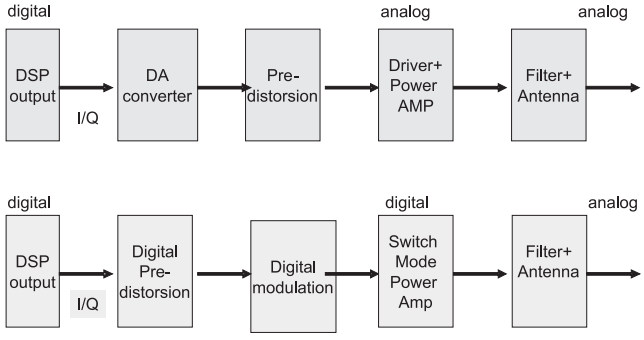

Fig. 1 Concepts of transceiver chains.

2. Device Technology and Simulation

Gallium Nitride HEMTs provide the outstanding properties of high-breakdown voltage in combination with the capability of very fast switching. Derived from an optimized analog power bar process, three process variants were used for the investigation of advanced broadband switching with the aim to reach 2 GHz operation.

2.1 Epitaxy and Technology

The epitaxial structures used in this work were grown by metal-organic chemical vapor deposition (MOCVD) on 3-inch semi-insulating SiC substrates. The layers consist of a highly-resistive c-plane GaN buffer, followed by an $Al_{0.22}Ga_{0.78}N$ barrier and finally a thin GaN cap layer. Room temperature Hall measurements on the two-dimensional electron gas (2DEG) formed at the buffer to barrier interface resulted in a sheet resistance, a sheet carrier concentration, and a mobility of 500 Ω/sq, 8×10^{12} cm^{-2}, and 1600 cm^2/(Vs), respectively. After epitaxial growth, ohmic contacts were formed, showing a low contact resistance of 0.2 Ωmm [3]. The nitride-assisted T-gate was used with three different gate lengths of 0.5 μm, 0.25 μm, and 0.15 μm, and was defined by e-beam lithography and trench etching into the SiN passivation [2]. Table 1 gives an overview on performance parameters of the three process variants investigated in this paper. The comparison is performed on the same epitaxy, while contact spacings and pitches are matched to the needs of the individual process nodes. Results on the powerbar capabilities of the process with a gate

Table 1 Some analog features of the AlGaN/GaN device technologies applied.

Gate length	[μm]	0.5	0.25	0.15
Operation bias	[V]	50	28	20
BV_{GD}	[V]	160	100	20
f_T	[GHz]	15	32	50
PAE	%	65	55	29
@ frequency	[GHz]	2	10	27

length of 0.5 μm have been reported elsewhere, e.g., [2]. In analog class-A-B operation, the process yields a very high PAE of up to 65%, as given in Table 1. Reasonably-high analog efficiency figures are given for two other gate lengths for higher frequencies of 10 GHz and 27 GHz for reference.

Furthermore the coplanar MMIC-process includes NiCr based 50 Ω/sq thin film resistors, metal-insulator-metal (MIM) capacitors as well as a thick plated Au-based air bridge technology.

2.2 Device Simulation of Switch-Mode HEMTs

To clarify the needs for switch-mode operation, the AlGaN/GaN devices are analyzed by means of two-dimensional hydrodynamic simulations using MINIMOS-NT, which was successfully employed for the development of AlGaN/GaN HEMTs [4], [5]. Material properties, such as band energies, carrier mobilities, and carrier energy relaxation times are properly modeled. The densities of the polarization charges at the channel/barrier interface and at the barrier/cap interface are determined by calibration against the experimental data to be 9×10^{12} cm^{-2} and -2×10^{12} cm^{-2}, respectively. Self-heating effects are accounted for by using substrate thermal contact in the simulation.

Devices with T-gates of 0.25 μm length are analyzed with respect to their input capacitance, their transconductance, and with respect to their gate-to-channel separation. For switch-mode operation, several trade-offs have to be considered, which differ from the analog needs. Enhancement-mode devices are very desirable in order to simplify biasing. Thus, the cap and part of the barrier layer under the gate of the EHEMT can be recessed by Cl_2-plasma etching. At the same time, fast current-mode switching requires low on-resistances and low-capacitances. Further, high-speed switching with high-oversampling requires low capacitances to reduce the dynamic switching losses. As example of the optimization, Fig. 2 gives the simulated transfer characteristics as a function of barrier thickness under the gate. The simulation shows the impact of the change of the threshold voltage with etch depth.

Figure 3 further gives the simulated gate-source capacitance C_{gs} as a function of barrier thickness. This is important to quantitatively estimate the change in the input capacitance for switch-mode devices. Since the gate capacitance depends on the gate-channel distance, we perform several simulations with variable recess depths, i.e., variable barrier thickness t_{bar} under the gate. As expected, a shift in the threshold voltage is observed (Fig. 2), and g_m (not explicitly shown) increases with decreasing t_{bar} due to the lack of charge control for thicker layers. Figure 3 shows that the gate-source capacitance C_{gs} increases with decreasing t_{bar}. The simulations in agreement with measurements further show that the f_T remains relatively constant with barrier variation. The transconductance g_m and input capacitance change simultaneously. Three conclusions can be drawn from Fig. 2 and Fig. 3. First, enhancement-mode devices can be achieved with a reasonable barrier thickness. Second, the input capacitance C_{gs} increases significantly with the reduction of the barrier thickness, which is a disadvantage for devices being driven in current-mode switching. However, also the C_{on} to C_{off} ratio improves with

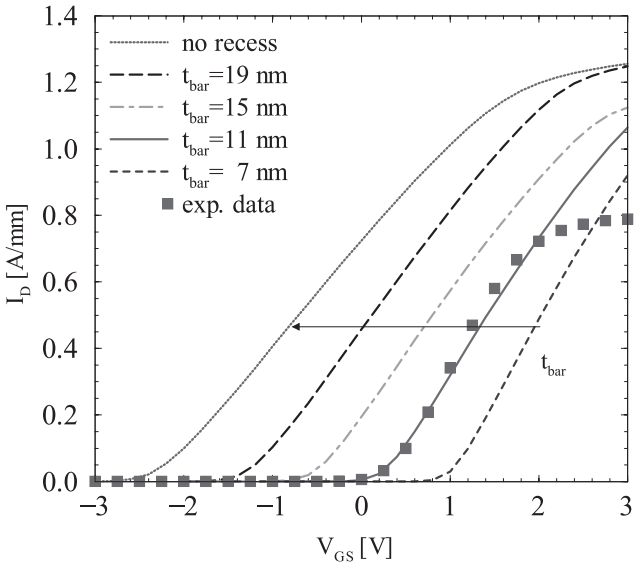

Fig. 2 Simulated and measured transfer characteristics as a function of barrier thickness under the gate.

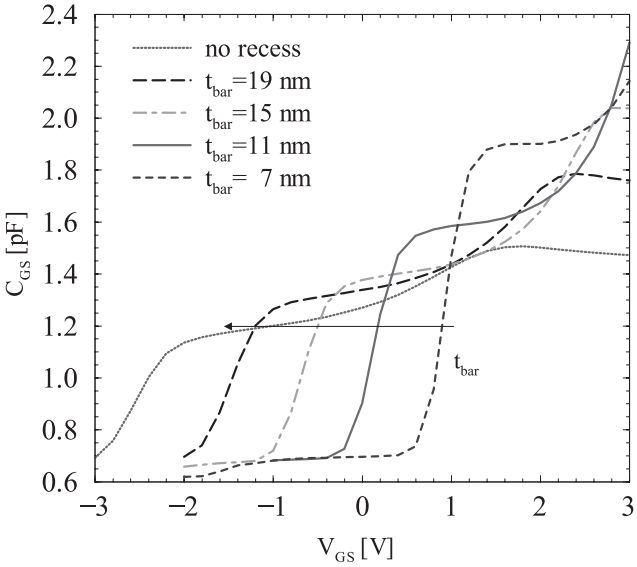

Fig. 3 Simulated transfer C_{gs} as a function of barrier thickness under the gate.

reduced barrier thickness. Third, as the transconductance also increase accordingly, the current-drive capability of the switch-mode FETs improves. Overall, moving the threshold voltage closer to 0 V improves the switching capabilities even without actually reaching enhancement-mode operation. For a given cut-off frequency, it is further desirable to have a high transconductance in order to improve the capability to drive parasitic lines in a current-mode amplifier. Last, reduction of the on-resistance R_{on} is key to minimize ohmic switching losses while maintaining reasonable device pinch-off at high-bias. In this study this is achieved by proper scaling of the contact separations for reduced gate-lengths accordingly.

3. GaN Doherty Amplifiers

Still based on silicon LDMOS and conventional GaN depletion-mode HEMTs, Doherty amplifiers are the workhorse of ourdays base-station replacing more conventional class-A-B amplifiers for linear efficiency reasons [6]. To that end a symmetric Doherty amplifier based on GaN HEMTs was realized and was linearized under realistic base station conditions. The fundamental gate periphery of the amplifier is $W_g = 2 \times 32$ mm. The AlGaN/GaN HEMTs is based on a gate length of 0.5 μm in this case with a threshold voltage of −3 V. The baseline technology refers to the non-recessed version in Fig. 2. The powerbar devices are packaged in conventional ceramic packages. The image of the complete amplifier is given in Fig. 4. The devices are biased at $V_{DS} = 30$ V. The peak amplifier was biased in class-C $V_{GS} = -4$ V, while the carrier amplifier was biased in class-A-B equivalent to a quiescent current of $I_{D,q} = 100$ mA/mm. At a high frequency of 2.7 GHz a small-signal gain of 9 dB is obtained.

One-carrier W-CDMA performance with digital predistorsion (DPD) and clipping reaches an average output power of 44.9 dBm (30.9 W) and a peak power of 50.5 dBm (112 W) at 2.7 GHz. The linearized spectrum at 2.7 GHz is given in Fig. 5. The markers for the 5 MHz and 10 MHz offset from the carrier are indicated. The measured associated drain efficiency (DE) of the linearized operation is >45% at 2.7 GHz and the 3GPP-ACLR specifications are met with −47 dB at 5 MHz and with −55 dB at 10 MHz offset. This example shows the excellent potential of conventional GaN FETs under realistic operating conditions up to a high frequency of 2.7 GHz with excellent linear PAE.

4. Switch-Mode Core MMICs

More advanced amplifier concepts such as class-S amplifiers have been suggested, e.g., in [7], however, operating at 450 MHz only. It is the aim of this work to demonstrate switch-mode core chips for data rates of >5 Gbits/s equivalent to 2.14 GHz operation, i.e., realistic mobile communication frequencies. Some aspects of circuit design of core chips based on a gate length of 0.25 μm were reported in [8]. For reference, the schematic is given in Fig. 6. The in-

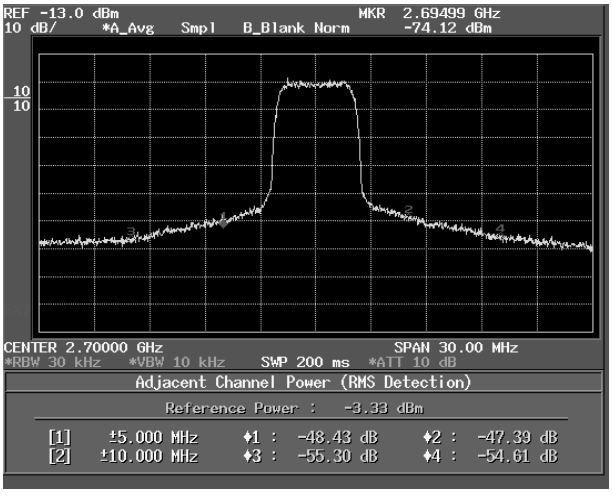

Fig. 5 Output power spectrum of the GaN Doherty amplifier at 2.7 GHz.

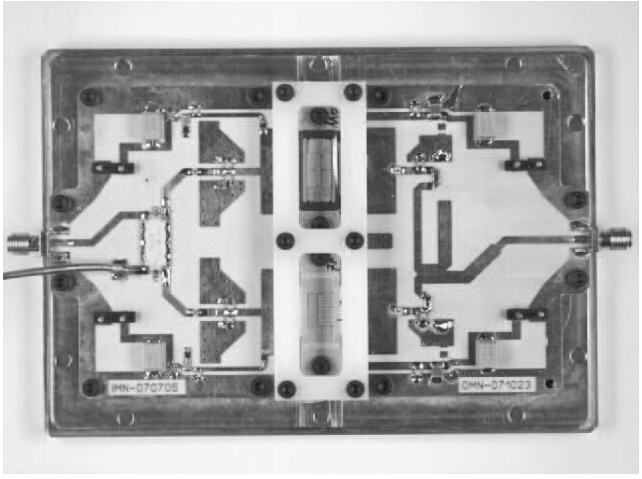

Fig. 4 Image of the symmetric GaN Doherty amplifier.

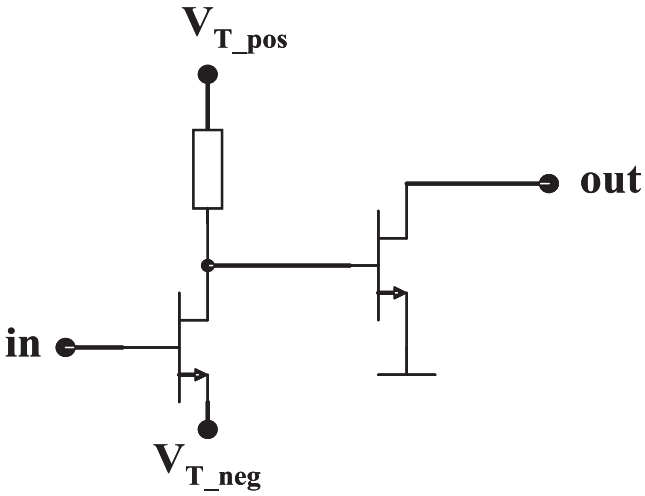

Fig. 6 Schematic of the dual-stage source follower core chip.

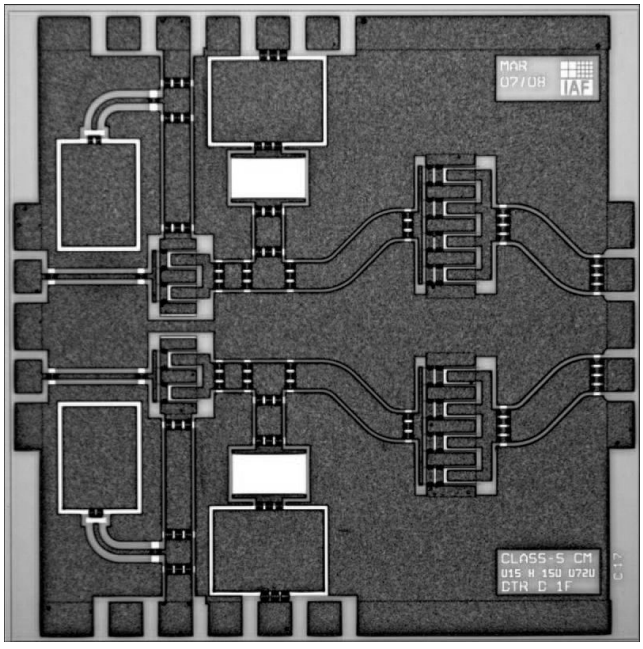

Fig. 7 Micrograph of a CMCD MMIC, chip size 2 mm × 2 mm.

put stage of the driver is biased externally. The output stage is biased with the DC-V_{DS}. The major application of such an MMIC PA is either a current-mode class-S operation or a current-mode class-D operation. In the experiment for estimating the class-D or class-S operation a square wave input signal (class-D) or a BPDS modulated signal (class-S) were applied to a dual-stage common source amplification circuit. The gate of the driver is biased at a typical DC-bias in class-A ($V_{GS} = -1.3$ V), which is adjusted via an external bias-Tee and the the two bias $V_{T_{pos}}$ and $V_{T_{neg}}$.

Figure 7 gives the micrograph of a broadband amplifier core chip in differential configuration investigated for various gate technologies in the following. For class-S operation band pass delta-sigma (BPDS) modulated signals request a very high signal bandwidth, which is the reason for applying a technology with a gate length as low as 0.15 μm. The frequency spectrum of the BPDS signal is defined from nearly DC to at least 4th harmonic due to a four times signal oversampling in generating the BPDS signal. A typical spectrum in class-S operation is given in Fig. 8 for a data rate of 5.2 Gbit/s. The main areas of interest include the loss mechanisms at high-data rates and the dependence of PAE and output power as a function of bias.

4.1 MMIC Circuit Design and Broadband Measurements

Circuit simulation and design were carried out using Agilent's ADS simulation environment including our in-house developed GaN HEMT large signal model. Because of the very high signal bandwidth of the modulated input signal, no conventional matching circuit can be applied to the input/output of the MMIC. Thus, the particular amplifiers can be operated at any bitrate within their particular bandwidth

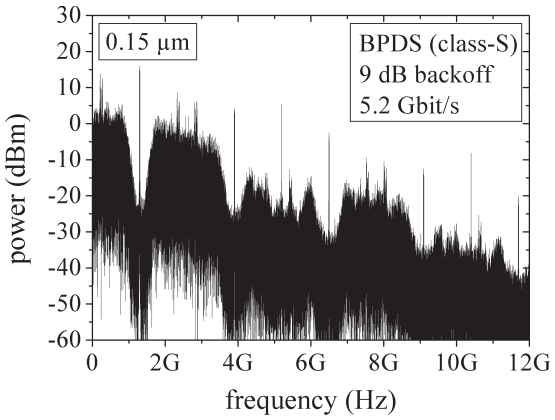

Fig. 8 Output spectrum under class-S operation for 5.2 Gbit/s.

determined mainly by the active device technology. Circuit design consist of waveform shaping for the particular maximum bitrate of the individual MMIC.

Broadband measurements were performed on a high-bandwidth (50 kHz to 40 GHz) measurement setup. The input signal source consists of an Anritsu MP1758A pattern generator with a series-connected preamplifier. A high power attenuator was used as broadband 50 Ω output load. The input and output bias networks were chosen very carefully to preserve the minimum and maximum available frequency of the measurement setup. A 50 GHz Agilent sampling scope (86100 with 83484A) combined with a software-based spectral S-parameter correction was utilized for broadband measurements of the waveforms. All data given in the following refer to measured broadband signals without any filtering, which, however, has to be applied for proper class-D/S operation in the final amplifier module. The measurements were taken for one amplifier of the differential amplifier pair shown in Fig. 7. For a full differential amplifier including a filter, a doubling in output power with nearly no decrease in efficiency is expected, as evaluated by circuit simulations. As an example for the signals, Fig. 9 gives the time-domain measurements at 0.9 Gbit/s, and 4 Gbit/s, respectively, for a core chip with a gate length of 0.15 μm.

4.2 Core Chip Realization

Power amplifier core-chip CMCD-MMICs based on GaN HEMTs with gate lengths of 0.5 μm, 0.25 μm, and 0.15 μm using advanced III-N MMIC processes are compared in this work. The CMCD-MMICs are designed in a dual-stage configuration with a gate width of 2 × 1.2 mm (for all gate lengths). The stages are mirrored for differential operation, as shown in Fig. 7.

4.3 Digital Class-D Operation

The class-D operation is induced by a periodic square wave input signal. The measured output bit-sequence at a data rate of 0.9 and 4 Gbit/s in square-wave operation was already

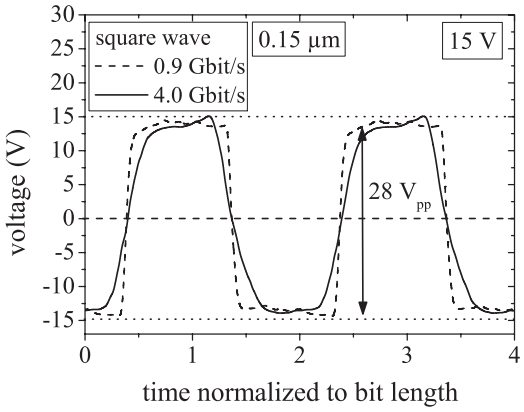

Fig. 9 Time domain measurements in current-mode class-D operation at 0.9 Gbit/s and 4 Gbit/s at an operation bias V_{DS} = 15 V.

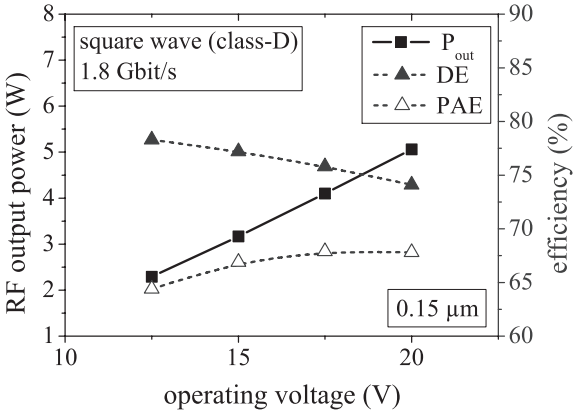

Fig. 11 Output power and PAE vs. DC-voltage V_{DS} at 900 MHz (1.8 Gbit/s) in class-D operation.

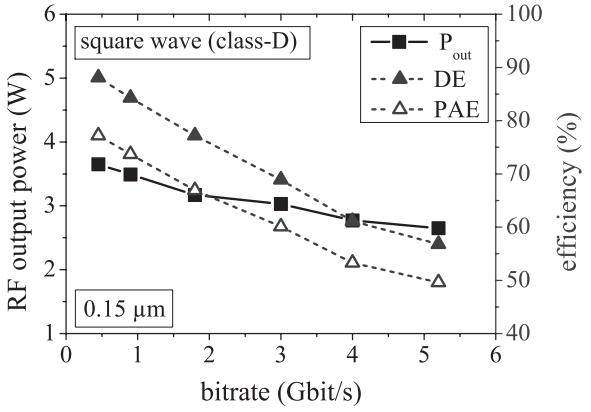

Fig. 10 Output and PAE power vs. bitrate in class-D operation.

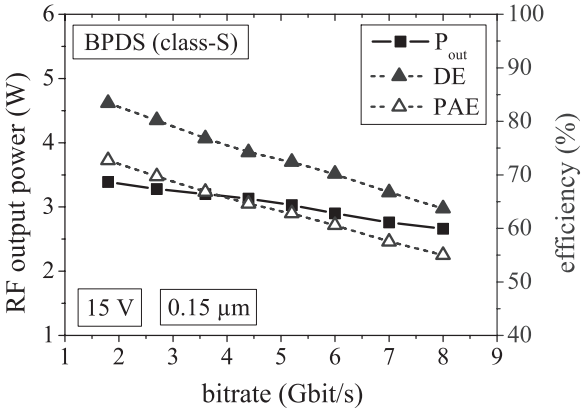

Fig. 12 Output and PAE power vs. bitrate in class-S operation for V_{DS} = 15 V.

given in Fig. 9 for a device with a gate length of 0.15 μm. We observe a voltage swing of 28 V at a DC-bias of V_{DS} = 15 V. The dependence of the switch-mode output power, broadband drain efficiency (DE), and broadband power-added efficiency (PAE) on bit rate in square-wave class-D operation is given in Fig. 10 for half of the circuit shown in Fig. 7. We use a calibrated and frequency corrected spectrum analyzer as a receiver for the broadband signal between near DC and 18 GHz. The passive losses in the set-up are accounted for likewise. The efficiency quantities drain efficiency (DE) and power-added efficiency (PAE) are calculated from the total broadband output and input power and the DC-power. The figure yields a maximum PAE of 74% at 0.9 Gbit/s and 53% at 4 Gbit/s. The output power level reaches 3–3.5 W for a gate width of 1.2 mm, which is equivalent to an output power density of up to 2.9 W/mm at V_{DS} = 15 V. For a given bias, the impact of the dynamic switching losses for this high-bit rate operation can be deduced from this figure.

Figure 11 gives the dependence of output power and PAE as a function of operation bias at 900 MHz in class-D operation, again for a gate length of 0.15 μm. An increase of the output power to 5 W is observed when increasing the operation bias, and likewise, the maximum voltage swing of the switch. The efficiency drops for two reasons: first, the design is optimized with respect to the reduction of the switching losses at a particular operation bias; second, and a bit more subtle: although the broadband device is not really matched to 50 Ω load in an analog microwave sense, however, when increasing the operation bias, the average mismatch of the HEMT impedance over frequency moves away from the 50 Ω load offered by the output line, which reduces PAE.

4.4 Digital Class-S Operation

For class-S operation a numerical generated 128k BPDS bit stream related to a 1-tone carrier at the specific fundamental frequency is used for the input signal. Figure 12 gives output power and PAE vs. bitrate for a MMIC, again with a gate length of 0.15 μm, measured up to 8 Gbit/s.

In this case for the same bit rate the PAE values are higher than in class-D and reach 63% at 5 Gbit/s. This can explained by the pulse-length modulation of the class-S signal, which has lower and higher frequency contributions, so that the devices are not always operated at the critical maximum of the frequency range.

Table 2 MMIC comparison in class-D operation at 900 MHz (1.8 Gbit/s).

l_g	[μm]	0.5	0.25	0.15
W_g	[mm]	1.2	1.2	1.2
V_{DS}				
20 V	PAE (DE)	59% (67%)	62% (69%)	68% (74%)
20 V	P_{out}	4.0 W	4.3 W	5.1 W
15 V	PAE (DE)	59% (71%)	62% (73%)	67% (77%)
15 V	P_{out}	2.7 W	2.8 W	3.2 W

Table 3 MMIC comparison in class-D operation at 450 MHz (0.9 Gbit/s).

l_g		0.5 μm	0.5 μm
W_g		2 mm	1.2 mm
V_{DS}			
20 V	PAE (DE)	70% (79%)	69% (76%)
20 V	P_{out}	6.0 W	4.9 W
15 V	PAE (DE)	66% (80%)	67% (80%)
15 V	P_{out}	3.6 W	3.1 W

5. MMIC Technology Comparison at 900 MHz (1.8 Gbit/s)

Among the MMICs discussed in the last section, a systematic comparison is performed including all three gate processes. Table 2 compares CMCD-MMICs in class-D operation for a data rate of 900 MHz. Several trends typical for switch-mode operation are observed: for a given bias and data rate the efficiency and output power increase with reduced gate lengths due to the improvement of the switching losses and the reduction of of the on-resistance. In this comparison, 900 MHz is the highest frequency for which measurements for all three gate lengths can be taken, particularly with respect to the gate lengths of 0.5 μm. One general limitation of the power measurements is the voltage and power limitation of the broadband bias-tees (up to 40 GHz), which are limited to 5 W and 20 V, thus measurements beyond these values are not taken.

Larger gate widths allow switching of higher currents and thus increased output power levels. However, larger gate widths also mean a reduction in speed and thus efficiency for a given data rate. Table 3 gives the comparison of two MMICs with the same gate length of 0.5 μm in class-D operation at 450 MHz. In this case the speed of the device is sufficient and only then the output power increases with gate width for nearly identical PAE and DE values.

6. Conclusions

In summary, this works demonstrates the enormous potential in efficiency and linearity potential of optimized AlGaN/GaN HEMTs in both conventional linear and switch-mode applications. Based on device simulations, the different requirements of AlGaN/GaN HEMTs for the switch-mode operation become visible, where threshold voltage, R_{on}-reduction, and capacitance reduction are dominant and have a direct impact on PAE and DE of the RF-power amplifier. Further, GaN Doherty base-station amplifiers demonstrate the enormous linearity potential at high operation frequencies of 2.7 GHz.

The use of AlGaN/GaN HEMTs in high-speed current-mode class-D/class-S MMICs for data rates of up to 8 Gbit/s in switch-mode operation equivalent to 2 GHz RF-operation shows the potential of GaN processes scaled to gate length of 0.15 μm for current-mode switching and the related efficiency vs. bitrate trade-offs. Very high switching efficiencies are reached for data rates as high as 8 Gbit/s, while the relative drop in PAE and DE suggests further reduction of the on-resistance and the parasitic capacitances for high-efficiency operation

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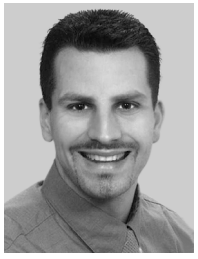

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