Interconnect Reliability Dependence on Fast Diffusivity Paths

Hajdin CERIC[1#], Roberto LACERDA DE ORIO[2], Siegfried SELBERHERR[1+]
[1]Institute for Microelectronics, Technische Universität Wien, Austria, *[2]Technische Universität Wien, Austria*
[#]Corresponding author: ceric@iue.tuwien.ac.at [+]Presenter

Electromigration experiments indicate that the copper interconnect lifetime decreases at every new interconnect generation.Modern interconnects, due to their reduced size, show a smaller void volume for failure, while a larger fraction of atoms is transported along fast diffusivity paths at copper interfaces to the surrounding layers and grain boundaries.This increasing dependence on fast diffusivity paths causes a significant variation in the interconnect performance and electromigration degradation. In order to produce more reliable interconnects, these fast diffusivity paths must be particularly addressed, when introducing new designs and materials.The electromigration lifetime depends on the variability of material properties at the microscopic and atomistic level. Microscopic properties are grain boundaries and grains with their proper crystal orientation. Atomistic properties are configurations of atoms at the grain boundaries, at the interfaces to the surrounding layers, and at the cross-section between grain boundaries and interfaces. Modern Technology Computer-Aided Design (TCAD), in order to meet the challenges of contemporary interconnects, must consist of three major areas: physically based continuum modeling, first-principle/atomic-level modeling, and statistical compact modeling.Our recent results from each of these three areas are presented. First, the theoretical background and description of methods for each component area will be given, followed by a presentation of the combined applications for each scenario.The source of electromigration performance variability lies in the atomistic level, for which first-principle methods must be employed. We use the results from such first principle methods in order to parameterize and modify the continuum level models.Furthermore, to investigate realistic three-dimensional interconnect layouts, continuum level models are used. The results of the corresponding simulations are applied to study failure scenarios and discuss implications to future interconnect designs.