Response of a single trap to AC Negative Bias Temperature Stress

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***Abstract* — We study the properties of a single gate oxide trap subjected to AC Bias Temperature Instability (BTI) stress conditions by means of Time Dependent Defect Spectroscopy. A theory for predicting the occupancy of a single trap after AC stress is developed based on first order kinetics and verified on experimental data. The developed theory can be used to develop circuit simulators and predict time dependent variability.**

***Index Terms* — Negative Bias Temperature Instability, constant voltage stress, AC stress, MOSFET, reliability, variability, SiON**

I. INTRODUCTION

Only a handful of gate oxide defects is expected to be active in future nm-sized CMOS devices [1-3]. Since digital circuits operate with binary AC signals, a good understanding of individual defect properties under AC conditions is compulsory to predict the device reliability [3] and to develop circuit simulators for future device generations [4-7]. Recently, a new methodology has been introduced to study the statistical properties of individual traps after Bias Temperature Instability (BTI) [8]. This new technique called Time Dependent Defect Spectroscopy (TDDS) is based on the quantized V_{TH} relaxation transients observed on nano-scale devices following constant stress [9,10]. It has been demonstrated that the emission and capture of single traps under constant stress are described by first order kinetics [8].

In this work, we study the response of a single gate oxide trap in a deeply-scaled SiON pMOSFET during AC negative bias temperature stress. We demonstrate that the behavior of individual traps as a function of the stress time and duty factor is dictated by their characteristic capture and emission times at DC high and low voltages. The developed AC model can be straightforwardly implemented in circuit simulators [5].

In this paper, a detailed description of the experimental setup is first given. The methodology to determine the emission and capture times of a single trap under DC stress is reviewed [8]. Afterwards, the statistical properties of the traps are studied under different AC stress conditions and temperatures. The theory to explain the experimental data is elaborated based on first principle kinetics and successfully verified.

II. EXPERIMENTAL

The setup used in our experiment is schematically depicted in Fig. 1. The four terminals of *a single selected 70×90 nm² 1.6 nm-SiON pMOSFET* were connected to Keithley 2602 source measurement units (SMUs). The SMU voltages were V_{RELAX} at gate, V_D = -0.1 V at drain, and $V_S = V_B$ = 0 V at source and bulk.

The device was gate stressed with an AC signal switching from V_{STRESS} to V_{RELAX} with a frequency f =100 kHz and duty factor DF (= $f \times t_H \times 100$ where t_H is the time that the signal is at high level) for stress time t_{STRESS}. During t_{STRESS} the gate terminal was connected to an HP8110 pulse generator.

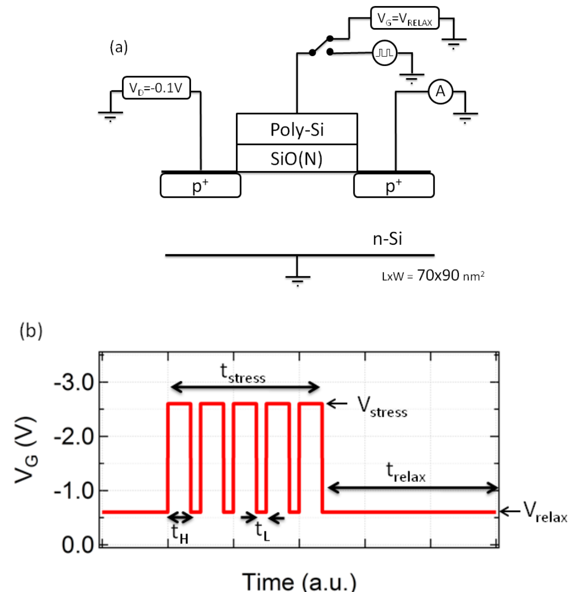

Fig. 1: Measurement procedure for investigating AC trap response. (a) AC signal is applied to the gate of *a selected 70×90 nm² SiON pMOSFET* and the source current I_{SOURCE} is registered as a function of time. (b) The applied AC signal switches between V_{STRESS} and V_{RELAX} for a stress time t_{STRESS}. Afterwards, the relaxation transient is registered at V_{RELAX} for a relaxation time t_{RELAX}.

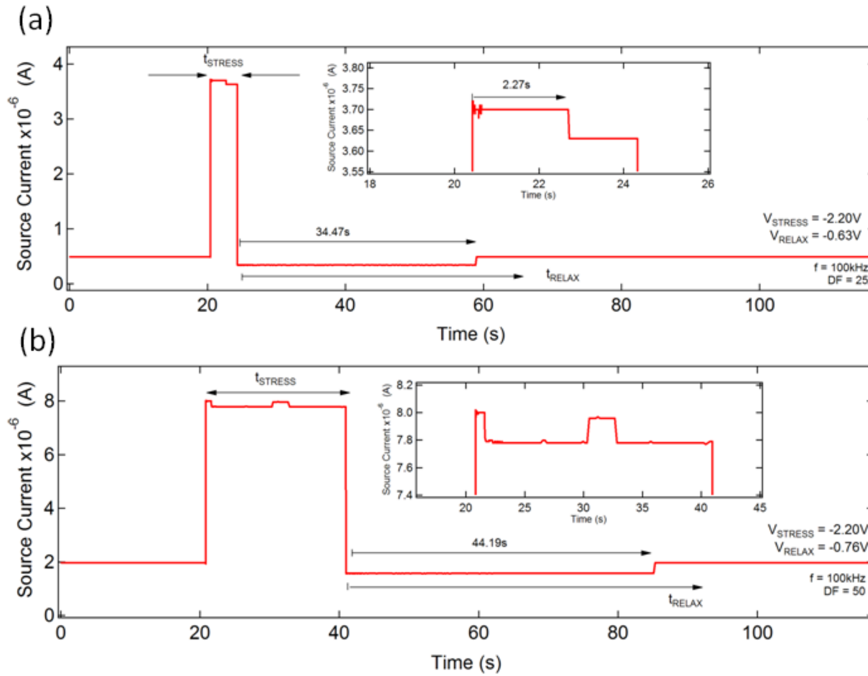

Fig. 2: Typical I_{SOURCE} vs. time curves obtained from *the single selected device* during the experiment. Measured I_{SOURCE} during stress is integrated over many AC periods. In (a) hole capture is observed at t_{STRESS} = 2.27 s, the charge is emitted after 34.74 s at V_{RELAX}. In (b), *capture* and *emission* are observed during stress.

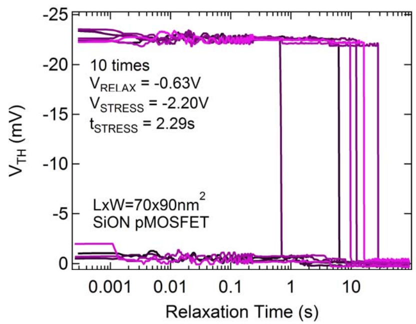

Fig. 3: 10 typical V_{TH} transients after DC stress at 25 °C and -2.2 V for 2.29 s. Note that 6 out of 10 traces show a giant discrete step of ~ 23 mV.

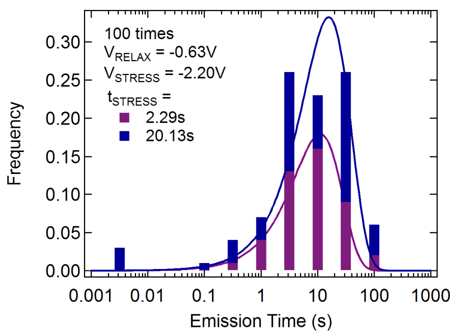

Fig. 5: Histograms f_E of the emission times t_e extracted from 100 V_{TH} relaxation transients under the condition of Fig. 3 for two different stress times 2.29 s and 20.13 s. Note that the emission times are binned on the logarithmic scale. The histograms can be fitted with eq. 2.

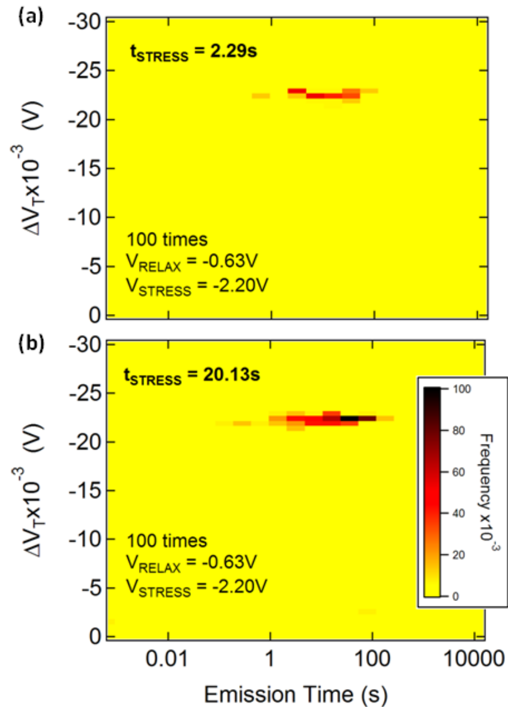

Fig. 4: TDDS spectra for two stress times (a) t_{STRESS} = 2.29 s and (b) t_{STRESS} = 20.13 s extracted from 100 recovery traces from the selected device one after the other under the condition of Fig. 3. A homogenous cluster appears at ~14 s and 23 mV for both spectra. Note that the intensity increases with increasing t_{STRESS} indicating that trap occupancy after longer stress increases.

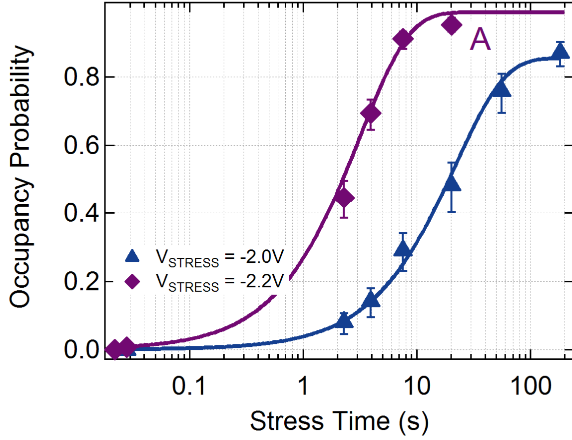

Fig. 6: Trap occupancy probability P_C with ±σ error bars vs. t_{STRESS} for a constant V_{STRESS} of -2.0 and -2.2 V and at 25 ºC. For the V_{STRESS} of -2.0 V, the occupancy does not reach 1, indicating that the emission time at V_{STRESS} = -2.0 V is comparable to the capture time. Capture and emission times extracted from the fitting to the data with eq. 3 are shown in Table I.

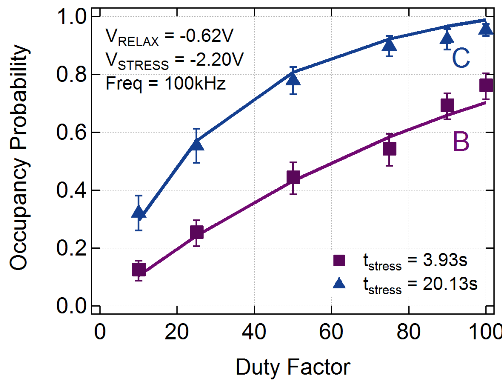

Fig. 7: (Symbol) Trap occupancy probability P_C (number of traces that presents the giant step / number of trials) applying Benard correction with ±σ error bars for V_{STRESS} = -2.2 V. (Lines) Predicted occupancy according to the proposed theory considering the emission and capture times at V_{STRESS} = -2.2 V and V_{RELAX} = -0.62 V (see Fig. 10 line B for t_{STRESS} = 3.93 s and line C for t_{STRESS} = 20.13 s).

T (°C)	V_G (V)	$\tau_{capture}$ (s)	$\tau_{emission}$ (s)
25	-0.62	> 200	14 ± 1
60	-0.62	> 200	0.14 ± 0.01
25	-0.76	> 200	57 ± 3
25	-2.0	25.5 ± 1.6	150 ± 32
60	-2.0	5.9 ± 0.3	5.7 ± 0.5
25	-2.2	3.2 ± 0.2	> 315

Table I. Emission and capture times obtained from the fitting of the experimental data acquired under DC stress with the maximum likelihood method to eq. 2 for emission times and eq. 3 for capture times.

Afterwards, the gate electrode was switched within less that a ms range to the SMU during a relaxation time t_{RELAX} = 200 s. The reed relay between the gate SMU and the pulse generator was controlled by the gate SMU. During this entire process the source current I_{SOURCE} was registered as a function of the time.

Fig. 2 shows typical I_{SOURCE} vs. time curves obtained in the experiment *on the selected device*. Note that measured I_{SOURCE} during stress is integrated over many AC periods due to the slow response of the SMU with respect to the applied signal (f = 100 kHz). In Fig. 2a, an abrupt drop of the source current I_{SOURCE} is observed at t_{STRESS} = 2.27 s, indicating a hole capture event. When the gate voltage switches again to V_{RELAX}, the source current is lower than the current at the start of the measurement (t = 0 s). The current suddenly recovers at t_{RELAX} = 34.75 s when the hole is emitted. Fig. 2b shows a trace where both capture and emission events are detected during stress. During relaxation the hole is emitted at t_{RELAX} = 44 s. The events observed during stress indicate that the occupancy at the end of the stress period is determined by the convolution of emission and capture processes.

III. DETERMINATION OF EMISSION TIME UNDER DC STRESS

Fig. 3 shows the relaxation curves at V_{RELAX} = -0.63 V after DC stress at 25 °C and -2.2 V. The V_{RELAX} is chosen close to the threshold voltage of the device so that ΔI_{SOURCE} varies strongly with respect to the absolute value of I_{SOURCE}. The source current I_{SOURCE} obtained following the procedure of Fig. 1 was transformed into a V_{TH} shift via a reference I_{SOURCE}-V_G curve of the device taken prior to stress [12]. Conversely to the continuous relaxation curves obtained in large devices [11,13], a discrete behavior is observed. Fig. 3 shows a giant V_{TH} shift of ~ 23 mV for 6 out of 10 traces at the start of the relaxation period that drops abruptly to 0 mV at t_{RELAX} ~ 14 s. This step height is significantly larger than the expected threshold voltage shift by the simple charge sheet approximation. This is due to the amplifying effect of the random dopants in the FET channel [2,14]. The step heights from device to device follow an exponential distribution and the number of steps per device is Poisson distributed [15]. The device under study on this paper was selected because it presented a large and single step, simplifying the analysis of the data.

Fig. 4 shows the corresponding TDDS spectra, i.e. two-dimensional histogram of the emission times t_e and the V_{TH} step heights, obtained from 100 traces of the device under study for two stress times: (a) 2.29 s and (b) 20.13 s. A homogenous cluster is observed at about 23 mV (cf. Fig. 3), indicating the presence of a single active trap. Fig. 5 shows the histograms of the emission times t_e (i.e. relaxation time at which the step is detected) obtained at the two stress times 2.29 s and 20.13 s shown in Fig. 4. The emission time t_e follows an exponential distribution as expected from first-order kinetics, i.e., in a Markov-process the transitions between two neighboring states are exponentially distributed [5,8]

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{RELAX}\right]\right\} \quad (1)$$

The emission times can be fitted with the maximum likelihood method and the histogram f_E when binned on logarithmic scale follows:

$$f_E(t_{RELAX}) = \frac{t_{RELAX}}{\tau_e}\exp\left[-t_{RELAX}\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)\right] \quad (2)$$

where τ_e and τ_c are the mean emission and capture times at V_{RELAX}, respectively. The fit of the data presented in Fig. 5 provides a characteristic emission time τ_e of about 14 s for both stress times. The characteristic emission time is independent of the stress time [8,11]. On the other hand, the characteristic capture time τ_c cannot be fitted accurately since this time is at least one order of magnitude larger than τ_e according the fit.

When the experiment was repeated at a higher absolute value of the relaxation voltage, V_{RELAX} = -0.76 V, the characteristic emission time increased to 57 s, i.e., the higher the relaxation voltage is, the larger the emission time is. Therefore, the characteristic emission time τ_e depends strongly on V_G (see Table I) [8], and, for this reason, τ_e has to be always referred to a particular voltage. The capture time for low voltages (-0.62 and -0.76 V) was estimated to be larger than 200 s for the modeling purpose presented in section VI.

IV. DETERMINATION OF CAPTURE TIME UNDER DC STRESS

The TDDS spectra of Fig. 4 show that the number of traces which present the giant step increases with t_{STRESS}. Fig. 6 shows the intensity of the cluster, i.e. the cumulative probability of charging the trap P_C (=occupancy probability), as a function of t_{STRESS} for V_{STRESS} -2.0 and -2.2 V. Note that the probability of occupancy saturates at 1 for V_{STRESS} = -2.2 V, and at 0.82 for V_{STRESS} = -2.0 V. As soon as the emission time at stress condition enters the same range as the capture time, the probability of intermediate emission during the stress cannot be neglected (see Fig. 2b). All these features can be described by first order kinetics

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{STRESS}\right]\right\} \quad (3)$$

where τ_e and τ_c are the mean emission and capture times at V_{STRESS}. If τ_c is much shorter than τ_e, the probability of occupancy reaches 1 as shown in Fig. 6 for V_{STRESS} = -2.2 V. In the case of the occupancy saturating at a lower value, the emission events during stress are not negligible and the characteristic emission and capture times can be determined simultaneously from the fit of the data. The corresponding likelihood function to maximize becomes:

$$\prod_{k=1}^{n_k} P_C(t_{STRESS,k})^{n_k}\left[1 - P_C(t_{STRESS,k})\right]^{n_k - p_k} \quad (4)$$

where p_k is the number of traces that show the step out of n_k traces observed for each stress time $t_{STRESS,k}$. Table I shows the obtained values for the different conditions applied in this experiment.

Note that the capture time decreases (i.e. the probability of capture increases) and emission time increases with increasing V_{STRESS} [8]. Therefore, at high gate voltages the capture events are dominant, while at low voltages it is the emission events.

V. PROBAILITY OF OCCUPANCY UNDER AC STRESS

Fig. 7 shows the occupancy probability P_C of the trap as a function of the duty factor DF of the AC signal for two values of t_{STRESS}. The AC signal switched between V_{STRESS} = -2.2 V and V_{RELAX} = -0.62 V. For both cases, P_C increases with DF up to the value corresponding to DC (see Fig. 6 for V_{STRESS} = -2.2 V).

For low DF (10, 25, and 50%), the capture and emission processes can be detected from the I_{SOURCE} traces during stress. For larger DF values, the delta of I_{SOURCE} with respect to the total I_{SOURCE} produced at the emission and capture events was too low to be distinguished with a reasonable level of certainty from the noise. Fig. 8 shows four typical I_{SOURCE} traces during stress at DF = 10%. In Fig. 8a, the source current keeps constant, conversely to Fig. 8b where a clear drop of the source current is visible at about 5.5 s, indicating the capture of a hole. In addition to the single capture process shown in Fig. 8b, emission events can also be visible during stress. In Fig. 8c, the hole capture is observed at ~7 s and its emission 2 s afterwards. In Fig. 8d, a second capture process is observed at ~16 s. Therefore the occupancy after a stress time t_{STRESS} is determined by the capture and emission events that take place during that period. Additionally, the number of traces that does not contain any capture event reduces with reducing the DF, i.e. the time that the voltage is at high level.

Consequently, the trap occupancy at the end of the stress time depends on the stress time and the capture and emission processes that take place during the AC stress. Additionally, the capture and emission processes are governed by the characteristic emission time τ_e and capture time τ_c at V_{STRESS} and V_{RELAX}, respectively. In the next section a theory to explain these features is developed.

VI. AC MODEL

In the sections III and IV, it has been demonstrated that the emission and the capture events are described by first-order kinetics and the occupancy probability are given by τ_e and τ_c at certain voltage. Therefore, the occupancy probability for the special case of digital signal switching between two levels (high (H) and low (L) levels) is described by considering the occupancy probabilities at high voltage P_{CH} and at low voltage P_{CL}, the times t_H and t_L that each voltage is applied during each period (see Fig. 1b), and the previous state. For the n-th period we can thus write

$$P_{CH}(n) = \frac{\tau_{eH}}{\tau_{eH} + \tau_{cH}} + \left\{P_{CL}(n-1) - \frac{\tau_{eH}}{\tau_{eH} + \tau_{cH}}\right\}\exp\left[-\left(\frac{1}{\tau_{eH}} + \frac{1}{\tau_{cH}}\right)t_H\right] \quad (5)$$

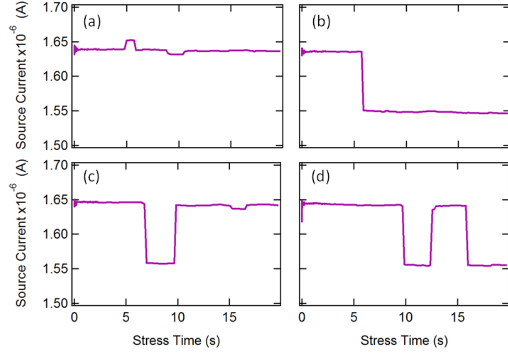

Fig. 8: Four typical I_{SOURCE} integrated over many AC cycles of frequency f = 100kHz vs. stress time t_{STRESS} curves obtained for V_{STRESS} = -2.2 V, V_{RELAX} = -0.62 V, and DF = 10%. During stress time at these conditions, different capture and emission processes are observed.

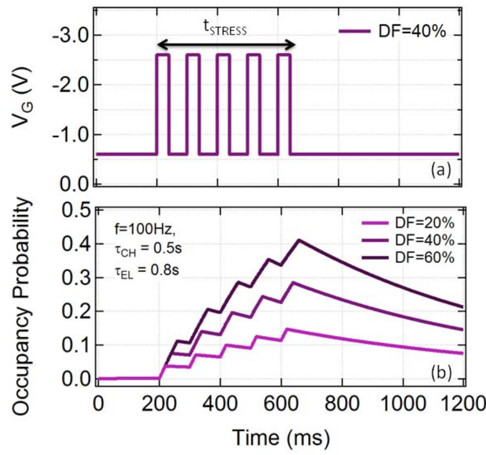

Fig. 9: Calculated occupancy probability P_C as a function of stress time t_{STRESS} (b) for the stress signal shown in (a). Occupancy was calculated according to eqs. (5) and (6) for the emission and capture times shown in (b). P_C after stress time t_{STRESS} depends on capture time τ_c, emission time τ_e at high (H) and low voltages (L), stress time t_{STRESS}, and duty factor DF.

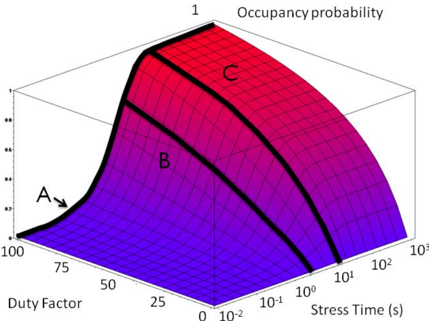

Fig. 10: Occupancy probability P_C as a function of t_{STRESS} and DF considering the conditions of experiment presented in Figs. 6 and. 7. Line A traces P_C vs. t_{STRESS} at DC stress (see Fig. 6). Lines B and C trace P_C vs. DF (see Fig. 7). The model can predict correctly P_C for all t_{STRESS} and DFs provided that the emission and capture times are known under DC conditions.

$$P_{CL}(n) = \frac{\tau_{eL}}{\tau_{eL}+\tau_{cL}} + \left\{P_{CH}(n) - \frac{\tau_{eL}}{\tau_{eL}+\tau_{cL}}\right\}\exp\left[-\left(\frac{1}{\tau_{eL}}+\frac{1}{\tau_{cL}}\right)t_L\right] \quad (6)$$

Fig. 9 shows the occupancy probability evaluated according to these equations. It is observed that the occupancy probability increases during the high level and decreases during the low gate voltage level. The occupancy probability increases up to a saturation level which can be lower than 1. This curve resembles the behavior of the charge and discharge of a capacitor under an AC signal. It is also noted that the higher the duty factor, the higher the occupancy probability P_C. When the stress signal is removed, the system returns to the occupancy probability dictated by eq. 6, i.e., the low voltage occupancy probability P_{CL}.

Expressing the increase in P_{CL} per period during the AC stress period, one can obtain the occupancy probability P_C as a function of the number of applied pulses n (= $f \times t_{STRESS}$):

$$P_C(n) = \frac{b}{a}\left(1 - e^{-an}\right) \quad (7)$$

where a and b are functions of τ_{eH}, τ_{cH}, τ_{eL}, τ_{cL}, DF, and f [5]. Fig. 10 shows P_C as a function of t_{STRESS} and DF calculated using eq. 7 and using the emission and capture times corresponding to the V_{STRESS} = -2.2 V and V_{RELAX} = -0.62 V (see Table I): the experimental conditions in Fig. 6 and Fig. 7. Line A in Fig. 10 corresponds to DF = 100% (DC stress). Line A is also a trace in Fig. 6. Under DC conditions, t_L is equal to 0 and eq. 7 becomes eq. 3.

Lines B and C in Fig. 10 correspond to the occupancy probability as a function of DF at fixed stress time t_{STRESS} of 3.93 s and 20.13 s. These lines are also traced in Fig. 7. It can be noted that the derived model follows correctly the experimental data.

If the characteristic emission and capture times are significantly larger than the period of the stress signal, eq. 7 can be simplified to a more intuitive equation

$$P_C(t_{STRESS}) = \frac{\tau_e^*}{\tau_c^* + \tau_e^*}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e^*}+\frac{1}{\tau_c^*}\right)t_{STRESS}\right]\right\} \quad (8)$$

where τ_c* and τ_e* are the effective capture and emission times under AC stress which depend on capture and emission times at V_{STRESS} and V_{RELAX}. These effective times are defined as:

$$\frac{1}{\tau_c *} = \frac{DF}{\tau_c(V_{STRESS})} + \frac{1-DF}{\tau_c(V_{RELAX})} \quad (9)$$

$$\frac{1}{\tau_e *} = \frac{DF}{\tau_e(V_{STRESS})} + \frac{1-DF}{\tau_e(V_{RELAX})} \quad (10)$$

Eqs. 7 and 8 provide the same occupancy probability since all the characteristic times of the trap under study (see Table I) are significantly larger than the period (1/f) of the AC stress signal.

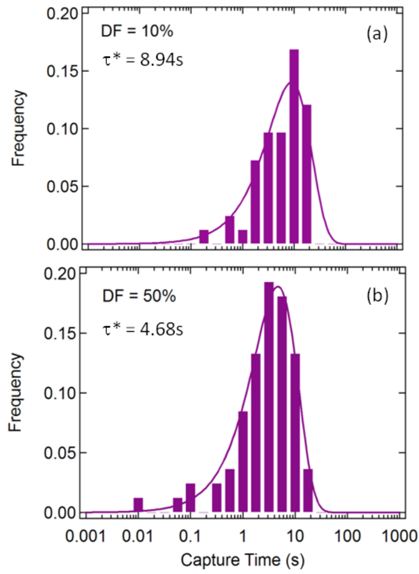

Fig. 11: Histograms of the first capture time t_c extracted from 80 I_{SOURCE} stress transients under V_{STRESS} = -2.2V and V_{RELAX} = -0.62V at (a) DF = 10%, and (b) DF = 50%. The capture times are binned on a logarithmic scale. Note that the effective time τ* obtained from the fit of the date to eq. 11 is longer than the capture time τ_c obtained at DC stress (Table I). τ* decreases with increasing the DF.

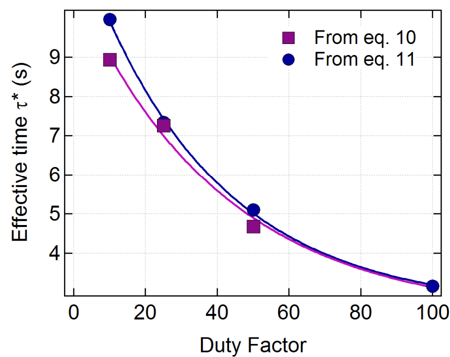

Fig. 12: Effective time τ* vs. DF obtained (■) from the fit of the capture times t_c registered during stress (see Fig. 11) to eq. 11 and (●) from the τ_e and τ_c obtained under DC conditions and eq. 12.

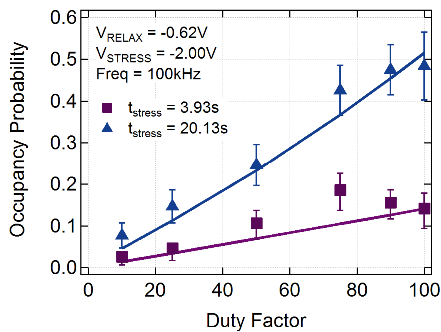

Fig. 13: (Symbols) Trap occupancy probability P_C with ±σ error bars for V_{STRESS} = -2.00 V and V_{RELAX} = -0.62 V as a function of the AC duty factor DF for two different values of t_{STRESS} (3.93 and 20.13 s). (Lines) Predicted occupancy according to eq. 7. Note that the experimental data match the derived model.

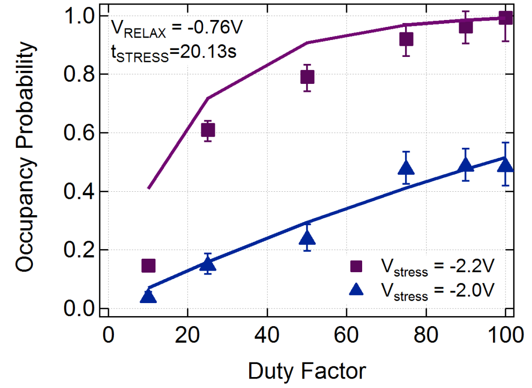

Fig. 14: (Symbol) Trap occupancy probability P_C with ±σ error bars for V_{RELAX} = -0.76 V. (Lines) Predicted occupancy according to the derived model matches the experimental data.

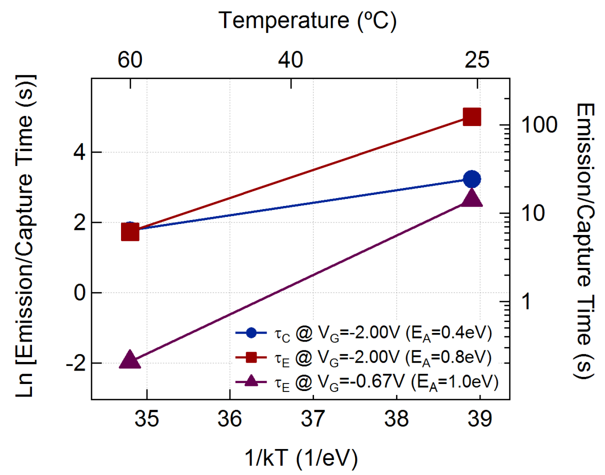

Fig. 15: Arrhenius plot of τ_e and τ_c. Note the large shift of the values for only a 35 °C increase of temperature, indicating that the capture and emission of charge are thermally activated processes [8,11]. The reduction of E_A for τ_e with increasing V_G is in line with the prediction of ref. [8].

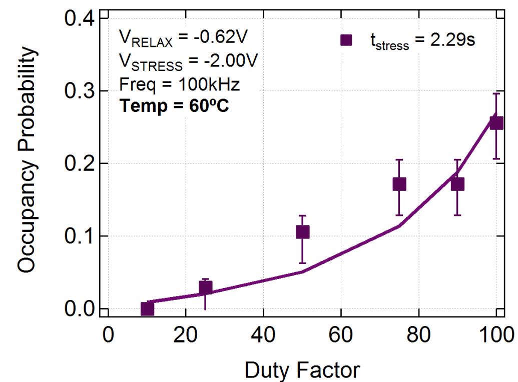

Fig. 16: (Symbols) Trap occupancy probability P_C with ±σ error bars as a function of duty factor DF at the temperature of 60 °C. Stress and relaxation voltages are the same as in Fig. 13. (Lines) Calculated occupancy probability obtained by means of eq. 7. Again, the experimental data match the derived model.

VII. Further Experimental Validation of the Model

Fig. 11 shows the histograms for the first capture time registered from 80 I_{SOURCE} *stress transients* under V_{STRESS} = -2.2 V and V_{RELAX} = -0.62 V at two different values of *DF*. Similarly to the emission times t_e, the capture times t_c follow the exponential distribution shown in eq. 7 and 8. The histogram of the capture times when binned on a logarithmic scale is given by

$$f_C(t_{STRESS}) = \frac{t_{STRESS}}{\tau_c *} \exp\left(-\frac{t_{STRESS}}{\tau *}\right) \quad (11)$$

where τ^* is the effective time:

$$\frac{1}{\tau^*} = \frac{1}{\tau_e^*} + \frac{1}{\tau_c^*} \quad (12)$$

Fig. 12 shows (1) the effective times τ^* obtained from the fit of the data in Fig. 11 to eq. 11, and (2) the effective times τ^* obtained by eq. 12 using the characteristic times obtained previously under DC stress (see Table I). Note that Fig. 12 only shows the effective time τ^* obtained by eq. 10 for low *DF* values, since only for low *DF* values, the capture/emission processes during stress are detectable (see Fig. 8). Fig. 12 shows a perfect agreement between both sets of data. Note that the average time τ^* decreases with increasing *DF* down to the value at DC stress, *DF* = 1, $\tau^* = \tau^*_c = \tau_c$. This again shows that the emission and capture event and the stress time are important parameters to determine the occupancy.

To further check the validity of the equations extracted in the last section, different stress and relax conditions were applied (Figs. 13 and 14). Note that the stress and relaxation voltages determine the capture and emission times of the trap (see Table I). Fig. 13 shows the occupancy probability P_C as a function of the duty factor *DF* for two stress times t_{STRESS}: 3.93 and 20.13 s. In this figure, V_{STRESS} was reduced to -2.0V with respect to the stress condition of Fig. 7, therefore the capture time τ_{cH} increases and the emission time τ_{eH} decreases (see Table I). The characteristics times (τ_{cL} and τ_{eL}) at low voltage are constant with respect to Fig. 7 since V_{RELAX} was not changed. Comparing Figs. 7 and 13, one can observe that the occupancy probability P_C increases with V_{SENSE}. The occupancy P_C according to eq. 7 is also traced in Fig. 13. We can observe that the equations developed in this paper correctly predict the experimental data.

In Fig. 14, the occupancy probability is plotted for two stress voltages V_{STRESS} at fixed t_{STRESS} =20.13s and V_{RELAX} = -0.76 V. The V_{RELAX} was increased with respect to Figs. 7 and 13, so the emission time τ_{eL} at low level was increased (see Table I). An increase of the emission time means an increase of the occupancy since the probability of emission at low voltage is reduced. This fact is observed in Fig. 14 when it is compared to Figs. 7 and 13. Once more, the lines represent the predicted occupancy according to eq. 7 using the emission and capture times corresponding to the stress and relax voltages of the experiment. The experimental data and eq. 7 developed in the last section based on first order kinetics are once again in agreement.

VIII. Temperature Dependence

Finally, the capture and emission processes were studied at a higher temperature (60 °C) under the stress and relax conditions of Fig. 13: V_{STRESS} = -2.0 V and V_{RELAX} = -0.62 V. Remarkably, during this experiment, the step height produced by the trap was reduced to 10mV with respect to the 23mV step height observed at 25°C. This feature has already been observed in Refs. [8] and [11]. The splitting of the cluster was explained by the electrostatic interaction with another charge trap [8].

By means of a DC stress, the emission and capture times at V_{RELAX} and V_{STRESS} were again first determined (see Table I) following the procedure presented in Sections III and IV. Fig. 15 shows the Arrhenius plot for the obtained characteristic emission and capture times at high and low voltages. As expected, these times decrease with increasing temperature. Large activation energies were extracted from the Arrhenius plots (see Fig. 15). Note that the activation energy for emission was about 1eV. These values are close to the activation energies for capture and emission times obtained for pMOSFETs in ref. [8] and for nMOSFETs in ref. [11]. This indicates that without any doubt the capture and emission times are thermally activated processes [16,17].

In Fig. 16, the probability occupancy P_C at 60°C is displayed as a function of *DF*. The lines show the predicted occupancy according to eq. 7 using the emission and capture times at 60°C. Experiment and theory are in agreement once more.

Summarizing, the model can predict correctly the P_C for all t_{STRESS} and *DFs* provided that the emission and capture times under DC conditions are known. Furthermore, the model can be used in simulations of the response of CMOS circuits under AC conditions [5], taking into account that (1) the V_{TH} shift produced by a single defect is exponentially distributed, (2) the number of defects per device follows a Poisson distribution [15], and (3) the emission and capture times are distributed inversely with time [10]. A circuit simulator based on the AC theory presented in this paper has been developed in ref. [5].

IX. Conclusions

In conclusion, we have studied thoroughly the response of a single trap under various DC and AC stress conditions. The theory to explain the obtained experimental data under AC stress has been elaborated based on first-order kinetics. This theory passes all sets of performed experimental tests. The model can thus be transferred to circuit simulators in order to simulate the effect of individual traps under AC workloads.

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