A Comprehensive Study of Nanoscale Field Effect Diodes

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Abstract

The performance of nanoscale Field Effect Diode as a function of the doping concentration and the gate voltage is investigated. Our numerical results show that the I_{on}/I_{off} ratio which is a significant parameter in digital application can be varied from 10^1 to 10^4 as the doping concentration of source/drain regions increased from 10^{16} to $10^{21}cm^{-3}$. The figures of merit including intrinsic gate delay time and energy-delay product have been studied for the field effect diodes which are interesting candidates for future logic application.

1. Introduction

According to the Moore's law, miniaturization of Si devices is reaching its limits. However, ultra scaled transistors suffer from short channel effects. By employing a Field Effect Diode (FED) structure one can improve such effects [1]. The performance of digital and analog circuits can be improved by replacing conventional MOSFETs by FEDs. They have many interesting properties and applications such as electrostatic discharge (ESD) protection [2-4] and memory cells application [5,6].

A FED is similar to a conventional MOS transistor with the exception of using two gates over the channel region and oppositely doped source and drain regions. As the channel length shrinks to dimensions less than 100nm, the regular FED has a large off-current. To overcome this problem, modified FED (M-FED) structure has been recently proposed [7]. In this structure, oppositely doped regions called reservoirs are introduced to the source and drain regions [1]. FEDs have superior properties to SOI-MOSFETs, since pinch-off, which limits current in MOSFETs, does not occur in FEDs.

In this work, the influence of the Gate voltage and source/drain doping concentration on device performance are studied. The I_{on}/I_{off} ratio, a very significant parameter in digital applications, is analyzed and compared to that of MOSFETs. We compare M-FED, with a MOSFET in terms of figures of merit, which are intrinsic gate delay time and energy-delay product.

2. Field Effect Diode Structure

A FED is a structure with two gates over its channel called GS and GD (see Fig. 1a) and oppositely doped source and drain regions. The gate contacts of a FED can be biased such that either a pn- or an np-channel replaces the lightly doped or intrinsic region between the source and the drain areas. Based on the gate biases, the source/channel/drain areas act as n^+npp^+ and n^+pnp^+ structures in the on and off states, respectively. Fig. 1a shows a regular FED, where the source and the drain have n-type and p-type doping, respectively. This FED will be in the on state if a positive voltage and a negative voltage are applied to the GS and the GD, respectively. By just reversing the gate voltage polarities the device will be turned off. In the off state, the device has a structure similar to a silicon-controlled rectifier (npnp). However, as the channel length shrinks below 100nm, regular FEDs can not be turned off [1]. To suppress this problem, M-FEDs have been proposed [1]. In this structure, oppositely doped regions called reservoirs are introduced to the source and drain areas of regular FEDs (Fig. 1b), where they assist the gate contacts to accumulate more holes and electrons under GS and GD, respectively, and induce a larger surface potential.

In other words, in the off state, the excess minority carrier injection takes place across the forward-biased n^+p (source side) and np^+ (drain side) junctions, causing an increase in the electron and hole concentrations in the p (under GS) and n (under GD) regions, respectively. This increase of the electron and hole concentrations obstructs the formation of a reverse-biased pn-junction in the channel. Therefore, to achieve a proper off-current, excess electrons and holes under GS and GD should be reduced. The reservoirs connect the p region under GS to the source and the n region under GD. As a result, the forward bias of the n^+p junction and the np^+ junction decreases and the carrier injection into the channel is reduced. In a forward biased FED, the drain voltage and the neighbouring gate have opposite polarities, therefore, pinch-off does not occur in FEDs and they do not suffer from hot electron effects, unlike short channel FETs [8,9].

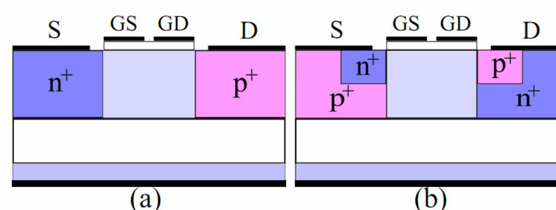

Figure 1: Schematic structures of (a) regular and (b) modified FED.

3. Simulation Results

The numerical device simulation results are obtained from MINIMOS-NT [10], which can be used to simulate nanoscale devices with an acceptable level of

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approximations. We have solved the Poisson and continuity equations to obtain the electrical characteristics of the M-FED, including current-voltage characteristics, and band-edge profiles. We studied M-FED with a channel length of 75nm, a gate length of 35nm, a body thickness of 50nm, and a gate oxide thickness of 2nm. The depths of reservoirs and source/drain regions are 50 and 25nm, respectively [11], and a device width of 1µm.

The effect of the gate voltage on the performance of M-FED is investigated. Fig. 2 shows the output characteristics of the M-FED at different gate voltages. The corresponding band-edge profiles along the channel are shown in the insets of Fig. 2.

The transfer characteristics at different V_{DS} are shown in Fig. 3. The subthreshold slope is approximately 140mV/decade at V_{DS}=1.0V.

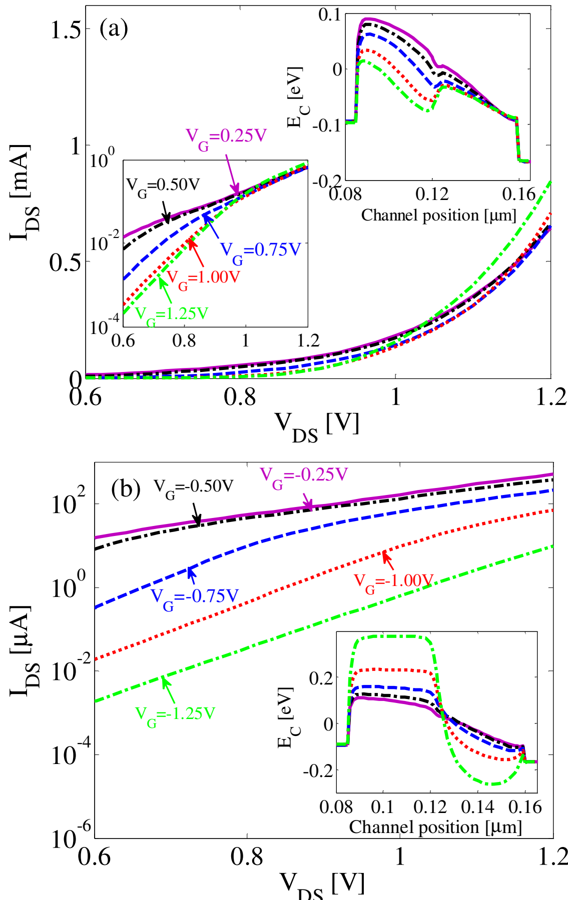

Figure 2: Output characteristics of the M-FED as a function of the gate voltage in the (a) on and (b) off state. $V_G = V_{GS} = -V_{GD}$. The insets show the band-edge profiles along the channel of M-FED in the (a) on and (b) off state.

Fig. 4 demonstrates the output characteristics of M-FED as a function of doping concentration in the on and off states. This figure shows the device has similar current-voltage characteristics to that of a forward-biased pn-junction diode and a negligible off-current. As shown in Fig. 4a, as the doping concentration of source and drain regions increases, the on-current increases and the I_{on}/I_{off} ratio varies corresponding to the decrease of off-current in various doping concentrations.

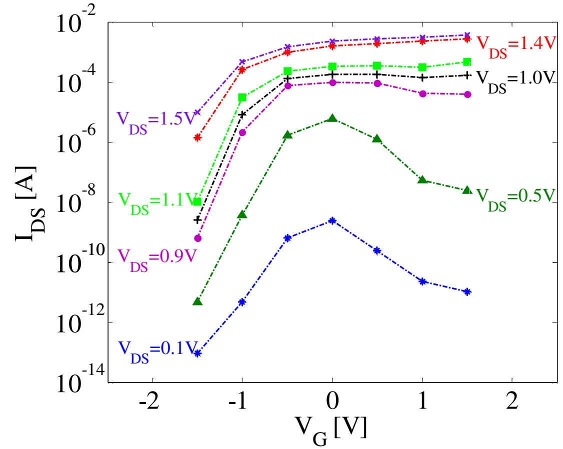

Figure 3: The transfer characteristics of M-FED at different V_{DS}. $V_G= V_{GS}=-V_{GD}$.

The corresponding band-edge profile along the channel of this structure is shown in the insets of Fig. 4. In both the on and off states, the BGN effect is observed in the highly doped source and drain regions, where the band gap is smaller than that of the channel. In this structure, the reservoirs help the gates to induce a larger potential onto the channel and reduce the off-current.

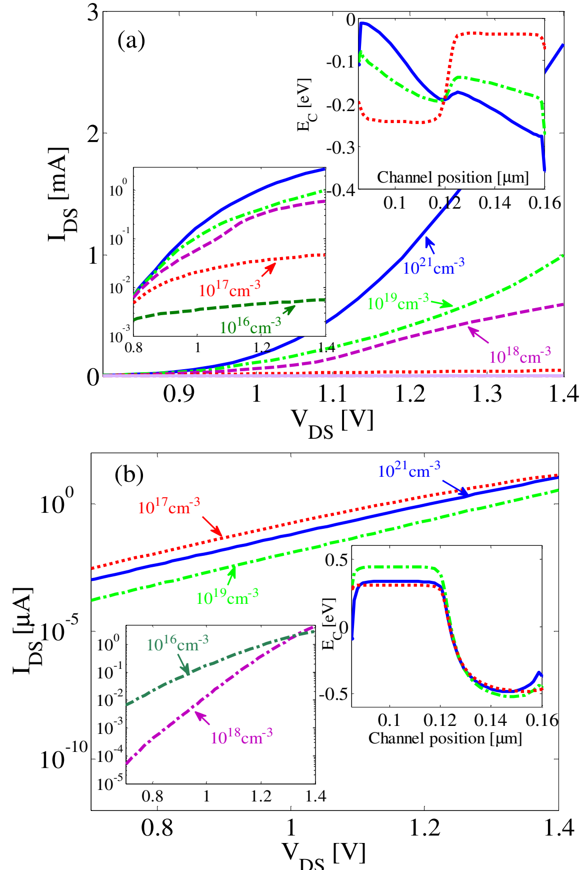

Figure 4: Output characteristics of the M-FED as a function of the doping concentration in the (a) on and (b) off state. The insets show the band-edge profiles

along the channel of M-FED in the (a) on and (b) off state.

Fig. 5 compares the output characteristics of M-FED with optimum doping concentration of 10^{21}cm^{-3} and a MOSFET with similar geometrical parameters. Unlike MOSFETs, the drain currents of FEDs do not saturate at high drain voltages which is due to the absence of pinch-off in FEDs. Furthermore, the I_{on}/I_{off} ratio of M-FED is at least two orders of magnitude higher than that of MOSFET.

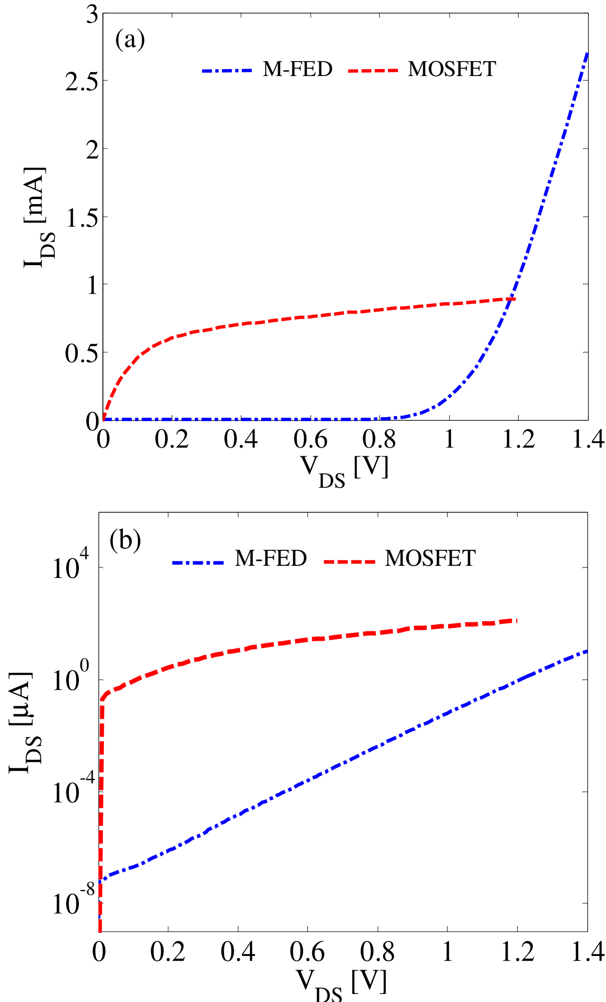

Figure 5: The output characteristics of M-FED and MOSFET in the (a) on and (b) off state.

We have compared the figure of merit of a MOSFET and M-FED as a function of the channel length. The same geometrical parameters have been considered for all these structures. The results have been compared at channel length of 35, 55, 75, 95, and 115nm. Fig. 6 compares I_{on} as a function of I_{off} for various channel lengths. Apparently, short channel effects are less pronounced in M-FEDs. Apparently, for channel lengths shorter than 100nm, M-FEDs show a better performance than MOSFETs. At a given I_{on}, the I_{off} of the FEDs is at least two orders of magnitude smaller than that of the MOSFET.

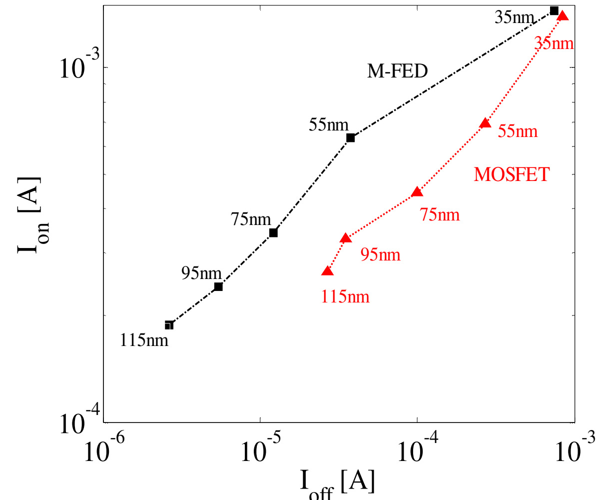

Figure 6: The comparison of I_{on} versus I_{off} for a MOSFET and M-FED as a function of the channel length.

The intrinsic gate delay time with respect to the I_{on}/I_{off} ratio can be employed to compare devices with different geometrical and material parameters [12]. The gate delay time, which characterizes the switching response of a transistor, is an important metric for digital electronic applications. The gate delay time of a transistor is defined as the time taken to charge a constant gate capacitance C_G to a voltage V_{DD} at a constant current I_{on}:

$$\tau = \frac{C_G V_{DD}}{I_{on}}$$

Fig. 7 compares the gate delay time as a function of I_{off} for MOSFETs and M-FEDs. The intrinsic capacitance (C_G) is calculated from simulation results by the derivation of the total charge present in the channel with respect to V_{GS}. The results shown in Fig. 7 demonstrate obvious advantages of FED devices.

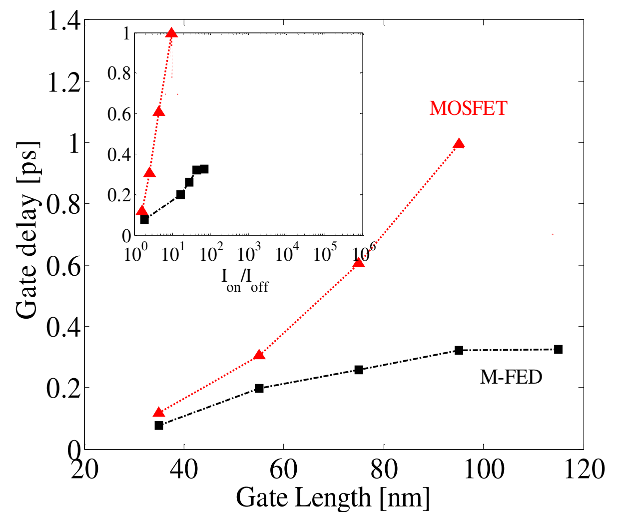

Figure 7: The intrinsic gate delay time as a function of

the physical gate length of MOSFET and M-FED. The inset shows the intrinsic gate delay time as a function of the I_{on}/I_{off} ratio for various channel lengths.

The intrinsic device speed of the MOSFET and M-FED with respect to the physical gate length is compared in Fig. 7. The gate length of M-FEDs is defined as the sum of two gate lengths and the spacer between them. The results shown in Fig. 7 indicate that M-FEDs exhibit a significant improvement over MOS devices. This improvement is primarily due to the suppression of short channel effects in FEDs. Based on the presented data, the speed of M-FEDs is higher than that of MFEDs at gate lengths shorter than 80nm. The inset of Fig. 7 compares the gate delay time as a function of I_{on}/I_{off} ratio for the MOSFET and M-FED with different gate lengths. The results show that M-FEDs have a smaller gate delay time in comparison to MOSFETs at gate lengths below 100nm.

The energy-delay product (EDP) is another figure of merit important for logic applications. EDP is a design metric for optimizing both energy efficiency and high performance. A smaller value of energy-delay implies a lower energy consumption at the same level of performance or in other words, a more energy efficient design. Fig. 8 compares the energy-delay product of the MOSFET and M-FED. Due to a higher on-current and lower off-current, M-FEDs show a smaller energy-delay product in comparison to MOSFETs.

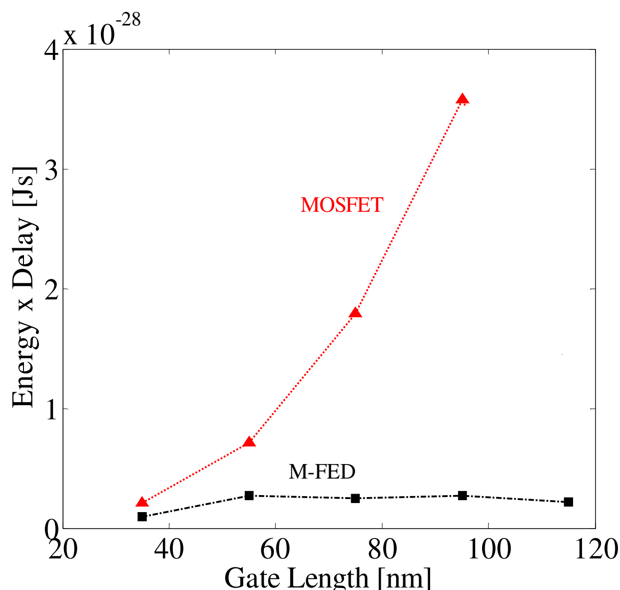

Figure 8: The comparison of the energy-delay product of a MOSFET and M-FED as a function of the physical gate length.

4. Conclusions

In this paper, the effect of the gate voltage and the doping concentration on the performance of M-FED is investigated. Our results indicate that by appropriate selection of the applied gate voltage, the I_{on}/I_{off} ratio can be varied and also show that by appropriate selection of the doping concentration, the I_{on}/I_{off} ratio can be increased to 10^4 for M-FEDs. Important figures of merit of M-FED for digital applications have been compared against those of MOSFETs. The results indicate that short channel FEDs, outperform MOSFETs. Results demonstrate that M-FEDs can be considered as interesting candidates for future digital applications.

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