Strain Engineering Techniques: A Rigorous Physical Review

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Starting with the 90-nm CMOS technology node, strain engineering takes a key position among other technological innovations, because it is cost effective and the beneficial effect of strain on the device performance is comparatively large. Ever since, increasing emphasis is put on strain technologies to further enhance chip performance in upcoming CMOS technology nodes.

The band structure of silicon under arbitrary stress/strain conditions is calculated using the empirical nonlocal pseudopotential method. The method is discussed with a special focus on the strain induced breaking of crystal symmetry. It is demonstrated that under general stress the relative movement of the sub-lattices has a prominent effect on the conduction band masses. This displacement, which cannot be determined from macroscopic strain, is extracted from ab initio calculations.

The transport properties of strained silicon are investigated by solving the semi-classical Boltzmann equation using the Monte Carlo method. It is shown that the change of the electron effective mass induced by uniaxial stress has to be included in accurate models of the electron mobility. The main findings are summarized, and important directions for future research are recommended.