Hot-Carrier Degradation Modeling Using Full-Band Monte-Carlo Simulations

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***Abstract*-We propose and verify a model for hot carrier degradation based on the exhaustive evaluation of the energy distribution function for charge carriers in the channel by means of a full-band Monte-Carlo device simulator. This approach allows us to capture the interplay between "hot" and "colder" electrons and their contribution to the damage build-up. In fact, particles characterized by higher energy are able to produce interface traps by a single-carrier process while colder ones trigger multivibrational mode excitation of a Si-H bond. For the model validation we use long-channel MOSFETs and represent the degradation of the linear drain current. The single-carrier component dominates degradation (this is the usual tendency for long devices), however, the multiple-carrier process is still considerable being less and less pronounced as the source-drain stress voltage increases.**

I. INTRODUCTION

The aggressive scaling of the building element of modern microelectronics – MOSFET – suggested that starting from a certain technological node hot carrier (HC) degradation will not remain such a crucial concern as it was last several decades. In fact, for MOSFETs with a channel length of more than about 100 nm power supply scaled slower than device dimensions resulting in a dramatic increase of the electric field in the channel. As a consequence, carriers being accelerated by the field are able to gain considerable energies and thus to produce damage via breaking Si-H bonds, i.e. generating interface states [1-3]. These states (when populated) act as additional Coulombic centers thereby distorting the electrostatics of the device and introduce additional scattering events for charge carriers.

However, when the modern CMOS technology entered the deep-submicron era, supply voltages of ultra-scaled device lie substantially below those ensuring carrier heating up to energies required for triggering the Si-H bond-breakage process. Therefore, the halt of HC degradation was assumed for those extremely-small devices. However, in practice even modern transistors employed in integrated circuits for logic applications are subjected to HC degradation [4-6].

Such a tendency can be described within the concept that the dominating mechanism for Si-H bond-breakage is changed while switching from long channel and/or high voltage (HV) transistors to low voltage (LV) scaled devices [4-6]. According to the first scenario, in a HV device carriers impinging the interface are already rather hot thereby triggering silicon-hydrogen bond rupture by a single collision (single-carrier mechanism). On the contrary, in scaled devices several particles bombarding a bond excite it eventually leading to its rupture (multiple-carrier process). These two scenarios are just limiting cases and in a particular device geometry under certain operation/stress conditions a superposition of these two mechanisms is realized.

In order to explain the double-power law behaviour observed during the hot-carrier stress, two types of bond-breakage mechanisms have been employed by the group of Hess [7,8]. Independently, Bravaiax also distinguish between these two scenarios while analyzing HC degradation for different types of devices [4,5].

Another important consideration consistent with this concept is the change of the worst-case conditions while switching from long-channel/HV devices to scaled ones. In the former situation these conditions are realized at the maximum substrate current (controlled by impact ionization) while in the latter one the maximum drain current (i.e. the maximum carrier flux) corresponds to the severest regime [4-8].

Another essential feature of hot-carrier degradation is its strong localization near the pinch-off region – close to the area where the electric field (driving force) peaks and where carriers are characterized by high energies. Moreover, this circumstance is valid for both long- and short-channel devices in spite of the different dominant contributions to the interface state generation.

All these considerations unequivocally demonstrate that the matter is controlled by the manner how carriers are distributed over energy in a particular point in the channel. This is described by the carrier energy distribution function (DF) which e.g. controls the interplay between populations of "hot" and "colder" carriers and thus different mechanisms of

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bond-breakage. For both processes the energy distribution of carriers enters the acceleration integral (AI) of the interface state generation rate [4,9]. Although the necessity of thorough calculations of these factors has been acknowledged [9], in practice simplified versions of the model are being used [4,5]. In these approaches evaluation of the AI for a particular device topology (based on the assessment of the carrier distribution function) is substituted by some empirical factors related to the real operating/stress conditions. However, in order to capture such an essential feature of HC degradation as its strong localization and the dependence of the trap density on the lateral coordinate (along the interface) a precise calculation of the DF is desired.

In this work we present and verify a HC degradation model based on the thorough evaluation of the carrier energy distribution function for a certain device architecture. For this purpose we employ full-band Monte-Carlo device simulator.

II. Model Description

The single-carrier process is related to the excitation of the bonding electron to the antibonding state and further designated as AB-process [9]. The multiple-particle process presumes a sequence of interactions of several particles (not obligatory "hot") with a S-H bond resulting in multivibrational mode excitation of the bond (MVE-process) [4,9]. Both processes are controlled by the carrier acceleration integral and thus strongly dependent on the shape of the carrier DF in a particular point near the Si/SiO_2 interface.

Following [6] we write the generation rate for the AB-process as:

$$\lambda_{AB} = \nu_{AB} \int_{E_{th}}^{\infty} I(E)\sigma_{AB}(E)dE, \tag{1}$$

where the integration is performed beginning from the threshold energy E_{th}; ν_{AB} is the attempt frequency and $\sigma_{AB}(E) = \sigma_{0,AB}(E - E_{th})^p$ is the Keldysh-like reaction cross section with $p = 11$ [4,9,10]. $I(E)$ is the carrier flux. Evolving $I(E)$ we obtain:

$$\lambda_{AB} = \nu_{AB} \int_{E_{th}}^{\infty} f(E)g(E)\sigma_{AB}(E)v(E)dE, \tag{1a}$$

with $f(E)$ being the energy distribution function obtained using full-band Monte-Carlo simulations, $g(E)$ the density-of-states and $v(E)$ the carrier velocity. Treating the interface states generation as a first-order chemical reaction one writes:

$$N_{AB}(t) = N_0(1 - e^{-\lambda_{AB}t}), \tag{2}$$

N_{AB} designates the density of interface states created due to the AB-process and N_0 is the number of passivated bonds [9].

As for the MVE-process, a silicon-hydrogen bond is treated as a truncated harmonic oscillator with corresponding phonon states characterized by the highest level N_{last} in this quantum well. This concept first was proposed while studying the bombardment of the hydroginated silicon surface by electrons tunneling from the STM tip (see e.g. [11,12]) and then adopted for the case of hot carriers impinging the Si/SiO_2 interface being also hydrogen annealed [13-15].

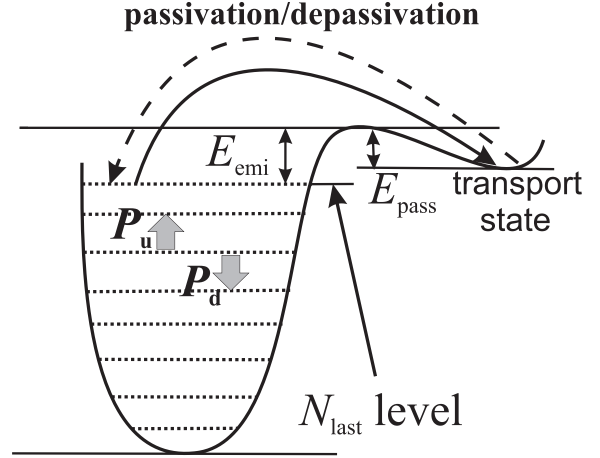

Fig.1. The MVE-process for silicon-hydrogen bond-breakage. The Si-H bond is treated as a truncated harmonic oscillator.

This truncated oscillator is sketched in Fig. 1. The bond-breakage process includes excitation of the system followed – if the last state is already reached – by hydrogen transition to the transport state. This hydrogen emission is described by an Arrhenius-law rate $\lambda_{emi} = \nu_{emi}\exp(-E_{emi}/kT)$ with the corresponding energetical barrier E_{emi} and prefactor ν_{emi} which is the attempt frequency (k is the Boltzmann constant and T is the lattice temperature). The reciprocal process related to the passivation of dangling bonds occurs when the H atom overcomes the barrier separating the highest level and the transport state (E_{pass}) and becomes bonded. This rate has a similar structure, i.e. $P_{pass} = \nu_{pass}\exp(-E_{pass}/kT)/N_0$, but the total concentration of passivated Si-H bonds enters this expression to warrant the dimensionality in (5c).

The upwards and downwards transitions of the oscillator are characterized by corresponding rates $P_u = I_{MVE} + w_e\exp(-\hbar\omega/kT)$ and $P_d = I_{MVE} + w_e$ related to the HC acceleration integral having similar structure as Eq. (1a) (w_e is the phonon frequency, $\hbar\omega$ is the distance between oscillator levels):

$$I_{MVE} = \nu_{MVE} \int_{Eth}^{\infty} f(E)g(E)\sigma_{MVE}(E)v(E)dE \tag{4}$$

To describe the kinetics of the oscillator we employ the system of equations similar to those proposed in [4,5] but with modifications for the last level (e.g. the term corresponding to the passivation reaction is included):

$$\frac{dn_0}{dt} = P_d n_1 - P_u n_0 \tag{5a}$$

$$\frac{dn_i}{dt} = P_d(n_{i+1} - n_i) - P_u(n_i - n_{i-1}) \tag{5b}$$

$$\frac{dn_{N_{last}}}{dt} = P_u n_{N_{last}-1} - P n_{N_{last}} - \lambda_{emi} n_{N_{last}} + P_{pass} N_{MVE}^2 \qquad (5c)$$

This system of equations is to be solved taking into account the time scale hierarchy. In fact, the steady-state of the oscillator is being established practically momentarily comparing to the hydrogen exchange between the highest bonded and the transport state. Therefore, while solving the sub-task related to the oscillator level occupancy we maintain only the first 2 terms in (5c) and recurrently obtain $n_i/n_0 = (P_u/P_d)^i$. After that, the passivation/depassivation rates are considered and the solution of (5) is written as:

$$N_{MVE} = N_0 \left(\frac{\lambda_{emi}}{P_{pass}} \left(\frac{P_u}{P_d} \right)^{N_{last}} \left(1 - e^{-\lambda_{emi} t}\right) \right)^{1/2}, \qquad (6)$$

Note that if the stress time is much shorter than the reciprocal depassivation rate ($\lambda_{emi}t << 1$) the solution (6) tends to the same dependence of the interface state density as was obtained in [4] (compare with Eq. 27).

While considering the total concentration of the interface states one should take into account the competing nature of AB- and MVE-processes and thus weight them with certain probabilities, i.e. express the trap density as $N_{it} = p_{AB}N_{AB} + p_{MVE}N_{MVE}$.

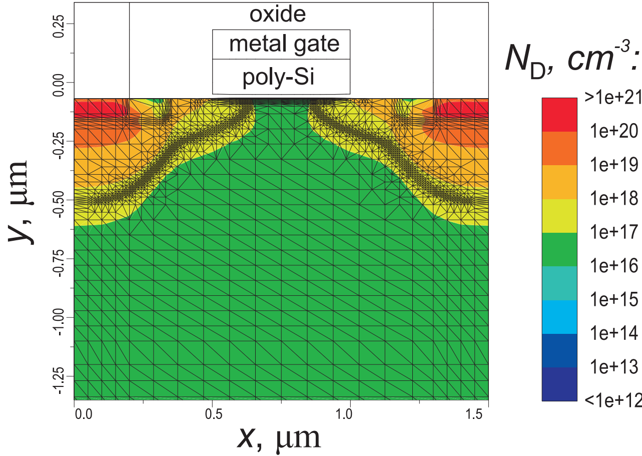

Fig. 2. The sketch of the n-MOSFET used for this work (device is cut at y ~ 1.4 µm). The phosphorous doping is represented by color map.

III. Model Verification

Low voltage 5V n-MOSFET designed on a standard 0.35 µm technology (device topology is sketched in Fig. 2) were stressed at a fixed gate voltage V_{gs} = 2.0 V and a series of 5 drain voltages: V_{ds} = 6.25, 6.5, 7.0, 7.25 and 7.5 V at $T = 25^0$ C during 10^4 s. The transfer characteristics of the fresh transistor are depicted in Fig. 3 and reproduced by the device simulator MINIMOS-NT [16] employed for the calculation of the device parameters. Since the transistor channel length is sufficiently large (~ 0.5 µm, Fig. 2) the macroscopic drift-diffusion and hydrodynamic models (implemented into MINIMOS-NT) for treatment of the carrier transport are well-suited.

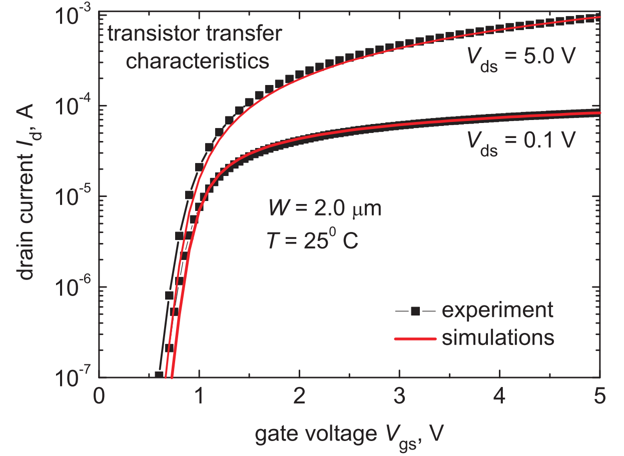

Fig. 3. Comparison between experimental and simulated I_d-V_g characteristics.

For evaluation of the DF of carriers the full-band Monte-Carlo device simulator based on a solution of the Boltzmann transport equation MONJU [17] has been used. Such important scattering mechanisms as electron-phonon scattering as well as scattering on ionized impurities and impact ionization, etc. are included into MONJU. Due to the statistical nature of the Monte-Carlo approach and in order to be sure that the chosen carrier packet is large enough both device simulators are used consistently providing comparable results.

The transformation of the DF calculated in the channel close to the source and drain, in the position with maximal AI (Fig. 5) and just after the gate electrode with increasing V_{ds} is shown in Fig. 4. One can see that when the applied bias V_{ds} increases the distribution function transforms in the manner to become deeper penetrating into high energies. At the same time the acceleration integrals (1a) and (4) also increase (Fig 5). Since the integrand in the AI is a superposition of the rapidly decreasing (with energy) DF and drastically increasing capture cross section, the peak of the AI is related to the area of most extended high-energy tails of the DF, but nevertheless is shifted out (this tendency is examined in our accompanying work [18]).

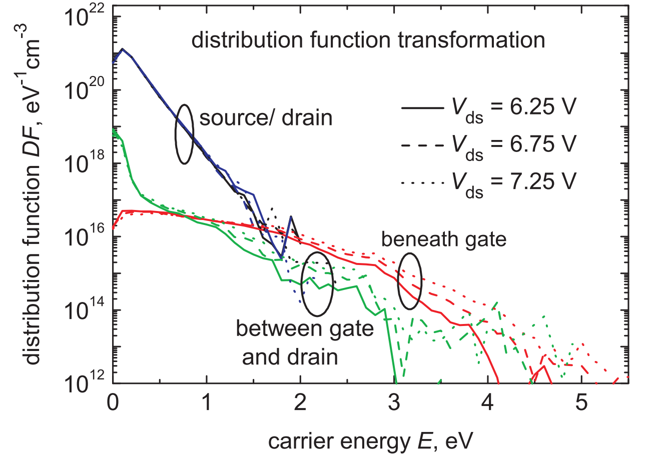

Fig. 4. Transformation of the DF with V_{ds} increase calculated for 4 different positions.

We calibrated the model in a manner to represent I_{dlin} (for V_{ds} = 0.1 V and V_{gs} = 5.0 V) degradation curves depicted in Fig. 6. The N_{it} profiles for V_{ds} = 6.25 V calculated for each time step are plotted in Fig. 7a (profiles correspond to the case of Fig. 6b, i.e. both AB- and MVE-components are presented) and the relative contribution of the MVE-mechanism (i.e. N_{MVE}/N_{it}) is plotted in Fig. 7b. Fig. 7a demonstrates strong localization of the HC degradation in the area featuring the peak of the acceleration integral (Fig. 5b), i.e. near at the drain end of the gate electrode.

The area where the AI is not peaking (i.e. for x < 0.8 μm and x > 1.1 μm, Fig. 5a) corresponds – of course, conditionally – to the situation of "colder" carriers. Thererore, it is reasonable that the degradation is favored by the MVE-process because electrons do not reach sufficient energy to rupture Si-H bonds by a single impact.

Comparison between Fig. 6a and Fig. 6b shows that curves simulated employing a superposition of the AB- and MVE-mechanisms – in spite of the small relative contribution of N_{MVE} (Fig. 7b) – better fit experimental data, especially for lower V_{ds}. This means that the interplay between "cold" and "hot" carriers is still important (even for relatively large devices and high stressing voltages), because the MVE-component is still presented, however, is less pronounced at V_{ds} > 7.0 V. This circumstance also seems quite reasonable because higher stress voltages lead to deeper high-energy tails of DFs and, hence, to higher average energies of carriers. As a consequence the "colder" fraction of carriers diminishes and the MVE-related contribution is thus neglected.

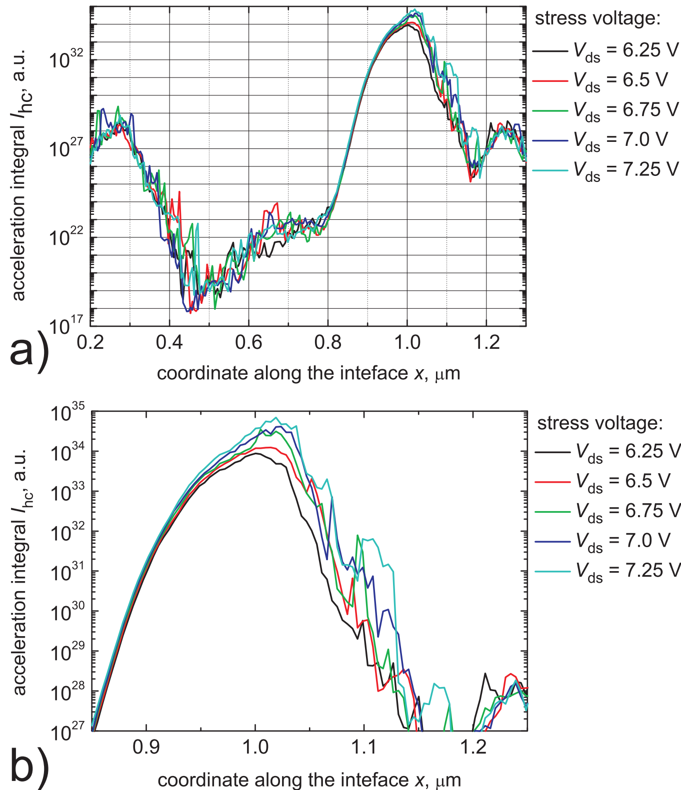

Fig.5. The dependences of the acceleration integral vs. x-coordinate calculated for different V_{ds}: (a) for the whole channel and (b) near the pinch-off region.

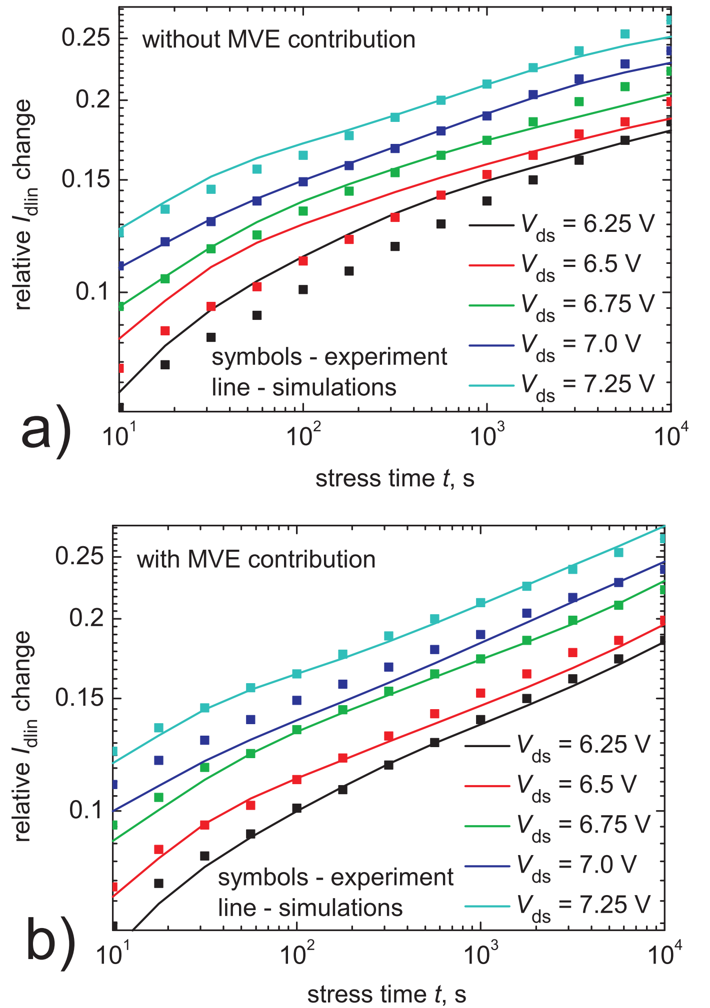

Fig. 6. Representation of I_{dlin} degradation curves by simulations: (a) without consideration of the MVE-mechanisms and (b) with the MVE being taken into account.

IV. Conclusion

In this work we have proposed a HC degradation model based on the thorough evaluation of the carrier distribution function in the channel employing a full-band Monte-Carlo device simulator. For model verification long-channel (~ 0.5 μm) MOSFETs characterized by relatively high operation voltage of 5V were used. The model has been verified by representing the linear drain current degradation for diverse stress conditions, and good agreement between experiment and simulations was achieved.

It has been shown that the concentration of interface states generated during the stress peaks at the drain end of the gate electrode, i.e. just in the area where the DF demonstrates most extended high-energy tails and where, hence, the carrier acceleration integral features its maximum. Therefore, the model captures one of the essential features of the HC degradation – its strong localized nature.

For these long-channel devices the main contribution to the damage is due to by the single-carrier process. However, as we have demonstrated, the MVE-mechanism still plays a

substantial role, especially in the region where the distribution function does not deeply expand and electrons are characterized by relatively low energies. It is worth mentioning that the relative contribution of the multiple-carrier process becomes less pronounced for higher source-drain voltages. Such a tendency is found to be quite reasonable because at stress voltages of ~ 7 V the fraction of "hot" carriers which are able to rapture Si-H bonds by a single collision becomes dominating.

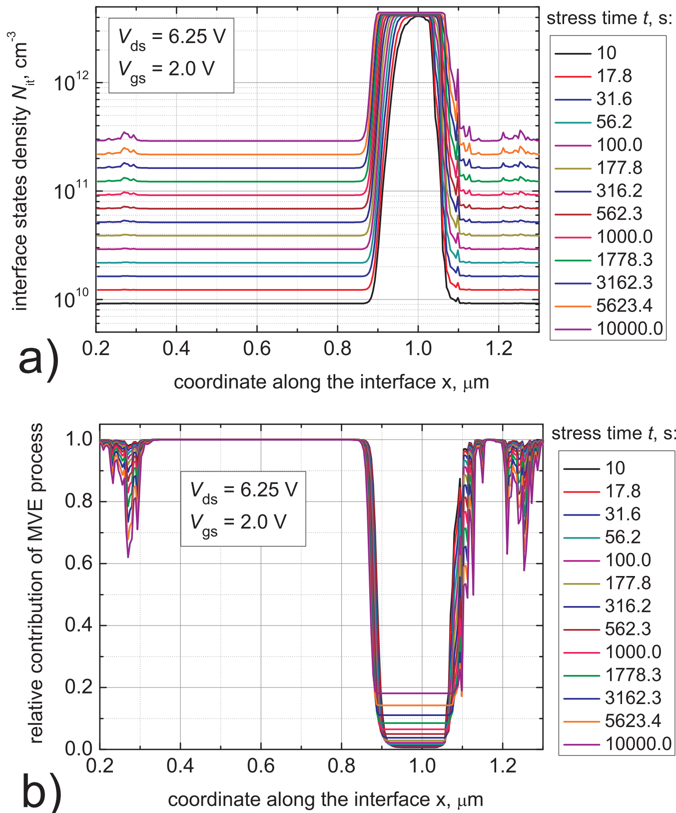

Fig. 7. The interface trap density vs. time and the position along the interface: (a) the total density N_{it} and (b) the relative contribution of N_{MVE}.

REFERENCES

[1] A. Acovic, G. La Rosa, Y.C. Sun, "A review of hot carrier degradation mechanism in MOSFETs", Microel. Reliab., vol. 36, No. 7/8, pp. 845-869, 1996.

[2] M.G. Ancona, N.S. Saks, D. McCarthy, "Lateral ditribution of hot-carrier-induced interface traps in MOSFET's ", IEEE Trans. Electron Dev., vol. 35, No. 12, pp. 2221-2228, 1988.

[3] Y. Leblebici, S.-M. Kang, "Modeling of nMOS transistors for simulation of hot-carrier-induced device and circuit degradation", IEEE Trans. Computer-Aided Design, vol. 11, No. 2, pp. 235-246, 1992.

[4] A. Bravaix, C. Guerin, ,V. Huard, , D. Roy, J.M. Roux, E. Vincent, "Hot-carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature" Proc. IRPS, 2009, pp. 531-546, 2009.

[5] C. Guerin, V. Huard, A. Bravaix, Journ. Applied Phys. , vol. 105, pap. No. 114513 (2009).

[6] W. McMahon, A. Haggaag, K. Hess, "Reliability scaling Issues for nanoscale devices", IEEE Trans. Nanotech., vol. 2, No. 1, pp. 33-38, 2003.

[7] K. Hess A. Haggag, W. McMahon, K. Cheng, J. Lee, J. Lyding, "The physics of determining chip reliability" Curcuits and Devices Mag., pp. 33-38, May 2001.

[8] A. Haggag, W. McMahon, K. Hess, K. Cheng, J. Lee, J. Lyding, "High-performance chip reliability from short-time-tests", in Proc. IRPS, 2001, pp. 271-279.

[9] W. McMahon, K. Matsuda, J. Lee, K. Hess, J. Lyding, "The Effects of a multiple carrier model of interface states generation of lifetime extraction for MOSFETs", 2002 Int. Conf. Mod. Sim. Micro, vol. 1, pp 576-579.

[10] J. Bude, K. Hess, Journ. Applied Phys., "Thresholds of impact ionization in semiconductors" vol. 72, No. 8, pp. 3554-3561, 1992.

[11] B.N.J. Persson, Ph. Avourisb, "Local bond breaking via STM-induced excitations: the role of temperature", Surface Science, vol. 390, pp. 45-54, 1997.

[12] K. Stokbro, C. Thirstrup, M. Sakurai, U. Quaade, Ben Yu-Kuang Hu, F. Perez-Murano, F. Grey, "STM-Induced Hydrogen Desorption via a Hole Resonance", Phys. Rev. Lett., vol. 80, pp. 2618-2621, 1998.

[13] R. Biswas Y.-P. Li, B. C. Pan, "Enhanced stability of deuterium in silicon", Appl. Phys. Lett., vol. 72, No. 26, pp. 3500-3503, 1998.

[14] Zh. Chen, P. Ong, A.K. Mylin, V. Singh, and S. Cheltur, "Direct evidence of multiple vibrational excitation for the Si-H/D bond breaking in metal-oxide-semiconductor transistors", Appl. Phys. Lett., vol. 81, No. 17. pp. 3278-3280, 2002.

[15] G. Ribes, S. Bruyére, M. Denais, F. Monsieur, V. Huard, D. Roy, G. Ghibaudo, "Multi-vibrational hydrogen release: Physical origin of T_{bd},Q_{bd} power-law voltage dependence of oxide breakdown in ultra-thin gate oxides", Microel. Reliab, vol. 45, pp. 1842-1854, 2005.

[16] MINIMOS-NT Device and Circuit Simulator, User's Guide, Institute for Microelectronic, TU Wien.

[17] C. Jungemann, B. Meinerzhagen, Hierarchical Device Simulation, Springer Verlag Wien/New York, 2003.

[18] I.A. Starkov, S.E. Tyaginov, O. Triebl, J. Cervenka, C. Jungemann, S. Carniello, J.M. Park, H. Enichlmair, M. Karner, Ch. Kernstock, E. Seebacher, R. Minixhofer, H. Ceric, T. Grasser, "Analysis of Worst-Case hot-carrier conditions for high voltage transistors based on Monte-Carlo simulations of distribution function", in Proc. IPFA, 2010, accepted.