preference for oral presentation

Interface states charges as a vital component for HC degradation modeling

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Abstract – We refine our approach for hot-carrier degradation modeling based on a thorough evaluation of the carrier energy distribution by means of a full-band Monte-Carlo simulator. The model is extended to describe the linear current degradation over a wide range of operation conditions. For this purpose we employ two types of interface states, namely, created by single- and by multiple-electron processes. These traps have different densities of states which is important to consider when calculating the charges stored in these traps. By calibrating the model to represent the degradation of the transfer characteristics, we extract the number of particles trapped by both types of interface traps. We find that traps created by the single- and multiple-electron mechanisms are differently distributed over energy with the latter shifted toward higher energies. This concept allows for an accurate representation of the degradation of the transistor transfer characteristics.

1. Introduction

Hot carrier (HC) degradation is associated with the build-up of defects at or near the silicon/silicon dioxide interfaced of an MOS transistor. This is due to the bombardment by carriers which have gained sufficiently high energy and thus called “hot” carriers (see [1] and references therein). These interface states, characterized by a density N_{it}, are able to capture charge carriers and, hence, become charged. These additional charges introduced into the system are distributed along the channel and perturb the electrostatics of a transistor. Furthermore, they act as additional scattering centers thereby degrading the linear drain current I_{dlin} and the transconductance.

The current understanding of the matter is that there are two competing mechanisms responsible for silicon-hydrogen bond-breakage, i.e. the single-electron (SE) and multiple-electron (ME) processes [2,3]. As we showed in our previous work [4] even for long-channel devices with relatively high operation voltages of 5V the ME-process still has a substantial impact on the device degradation and both SE- and ME-mechanisms are to be considered together.

At the same time different types of traps characterized by different density-of-states (DOS) profiles have been repeatedly reported in the literature (see e.g. [5-7]). Moreover, Hess et al [3,8] have explained different time slopes of degradation employing different types of defects, namely SE- and ME-induced; this concept is also supported by *ab initio* calculations [9].

We extend our previous approach for HC degradation modeling [4] which is based on a thorough calculation of the carrier energy distribution function (DF) by means of a full-band Monte-Carlo device simulator MONJU [10]. The model is refined in a manner to represent the evolution of the whole transfer characteristic (i.e. I_{dlin} degradation for various gate voltages V_{gs}). We demonstrate that this is possible by careful extraction of the DOS profiles of the two trap types. The density-of-states eventually determines the effective charge stored in the defects which determines the electrostatic and scattering contributions. Only charged traps affect the local band diagram of a transistor and play as Coulombic centers.

2. HC degradation model: basics

In this section we provide a short summary of our previous version of the HC degradation model [4] and then describe the refined model.

Both SE- and ME-processes are controlled by the carrier acceleration integral which has the following functional form [3,11,12]:

$$I_{SE} = \int_{Eth}^{\infty} f(E) g(E) \sigma_{SE}(E) v(E) dE \cdot \qquad (1)$$

Eq. 1 is written for the SE-mechanism while for the ME-process all indexes are to be replaced by “ME”. In (1), $f(E)$ is the carrier distribution function computed using the

Monte-Carlo simulator, $g(E)$ the density-of-states, $v(E)$ the carrier velocity and σ the Keldysh-like reaction cross section [3,4,11,12]. For the SE-process I_{SE} directly enters the interface state generation rate, i.e. $\lambda_{SE} = \nu_{SE} I_{SE}$ with ν_{SE} being the attempt rate. For the description of the ME-process the Si-H bond is treated as a truncated harmonic oscillator and the bond-breakage is thus a jump of the H atom from the highest bonded level to the transport state. The passivation of dangling bonds is treated as a backward reaction (for a detailed description see [4,11-13]).

Since only charged interface states impact the device behavior we calculate the charge stored in SE- and ME-related traps (total charge is $Q_{it} = Q_{SE} + Q_{ME}$) as:

$$Q_{SE/ME} = e\int g_{SE/ME}(E,x) f(E,x) dE, \qquad (2)$$

where $g_{SE/ME}(E)$ is the density-of-states for the SE- and ME-traps, e is the electron charge and $f(E)$ is the carrier distribution function. The DOS is a position dependent function as it reflects different degradation levels in different areas of the device. The distribution $f(E)$ also varies along the interface since the carrier concentration does. The integration over x is performed along the SiO_2/Si interface. We calibrate the model in order to represent the I_{dlin} degradation for all operation V_{gs} by proper determination of $Q_{SE/ME}$.

3. Results and discussion

For the evaluation of the HC degradation model we used low voltage (LV) n-MOSFETs fabricated on a standard 0.35 µm technology depicted in Fig.1.

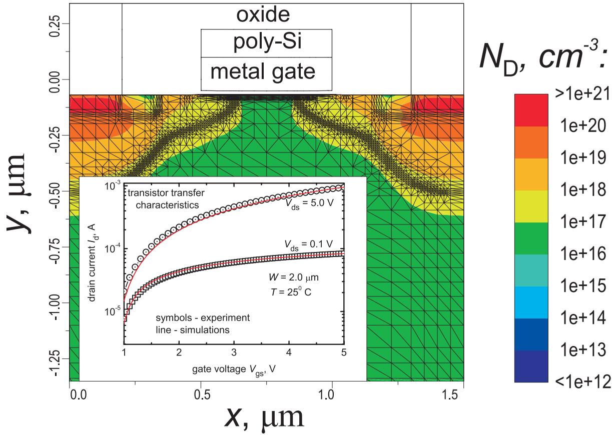

Fig.1. The n-MOSFET architecture. The phosphorous profile is represented by the colour map. Inset – the transfer characteristics of the fresh device: experiment vs. simulations.

The I_{ds}-V_{gs} characteristics of the virgin device are shown in the inset where the experimental curves are compared to the simulation obtained by our device simulator MINIMOS-NT [14] used within the Global TCAD Solutions framework [15]. We stressed the devices at various drain voltages V_{ds} = 6.25, 6.5, 7.0, 7.25 and 7.5 V and a fixed gate voltage V_{gs} = 2.0 V. Devices were tested for 10^4 s at the ambient temperature of $T = 25^0$ C.

The family of effective $Q_{it}(x)$ profiles calculated for various operation conditions (a set of gate voltages) but at a fixed stress time t of 10s is shown in Fig. 2. One can see that ME-induced defects come into play only for $V_{gs} \geq 3.0$. This circumstance means that SE- and ME-related defects are differently distributed over energy and last ones are shifted to higher energies. The result is conceivable with the concept proposed by Hess et al [3, 8]. This approach describes the double-power law dependence of the degradation by introducing different time slopes for defects created by different processes, namely, by SE- and ME-mechanisms.

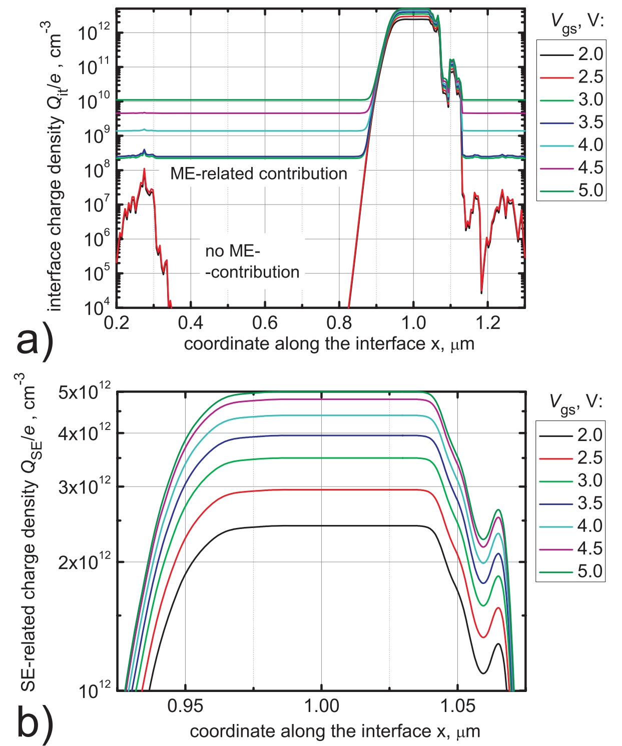

Fig. 2. The interface charge density (a) Q_{it} vs. the x-coordinate obtained for different operation conditions and (b) Q_{SE} plotted in the region of the N_{it} peak.

Fig. 2b resolves the dependences of density of particles captured by the SE-traps in the region where the total trap concentration N_{it} peaks vs. the lateral coordinate calculated for different V_{gs}. Since out of the N_{it} peak the main contribution to the total density Q_{it} is made by the ME-process one may compare the behaviour of densities related to the different types of traps. For the SE-process the distance between the curves saturates, meaning that interface states of this type are almost fully occupied. In contrast, for the ME-process the increase of charge density continues indicating the fact that ME-traps are shifted to

higher energies.

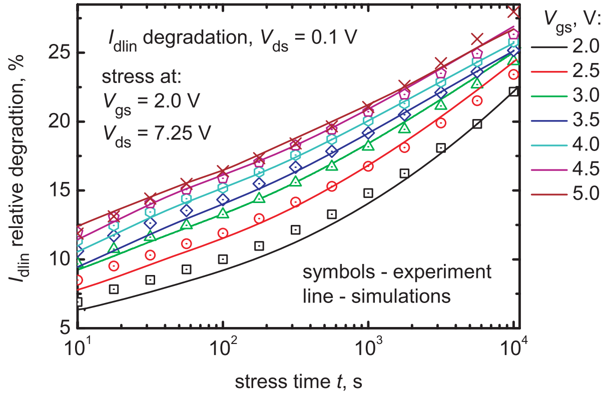

Fig. 3. I_{dlin} degradation obtained for different V_{ds} and for fixed stress conditions.

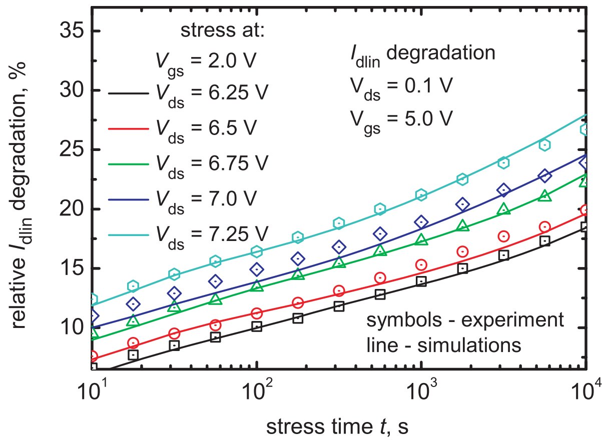

Fig. 4. Degradation of I_{dlin} obtained for different stressing V_{ds} and for a fixed V_{gs} V_{gs}.

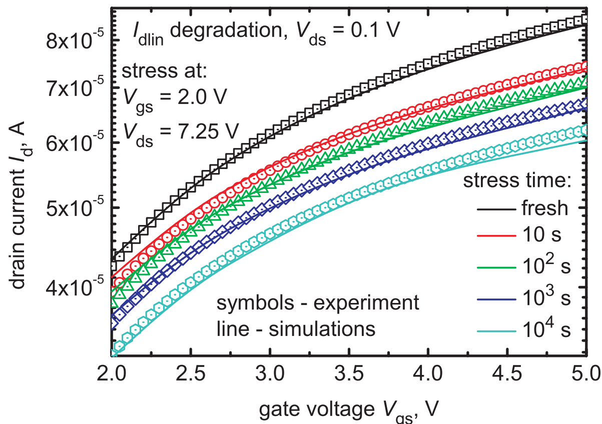

Fig. 5. The transformation of I_{ds}-V_{gs} curve during the HC stress.

The model calibrated in the aforementioned manner allows us to represent the I_{dlin} degradation at various gate voltages (Fig. 3) and for different stress conditions, i.e. different V_{ds} (Fig. 4). It is worth mentioning that we do not introduce any additional fitting parameters into the model meaning that N_{it} effectively changes while switching from certain stress conditions to another. Finally, using this approach we are now able to represent the transfer characteristics of the degraded device at each time step. Fig. 5 – demonstrating measured I_{ds}-V_{gs} curves vs. the simulated ones – reveals a very good agreement between experiment and theory.

4. Conclusion

Based on the previous version of our model for HC degradation we have extended it in order to capture the transformation of the whole I_{ds}-V_{gs} characteristic. The charges stored in different types of traps (rather than net concentrations of these traps) are responsible for the degradation of the device output characteristics and thus are important. In order to capture this effect we have to calculate the corresponding charges as fitting parameters and extracted them by calibrating the model in order to represent the transistor transfer characteristics. Our simulations confirm that SE- and ME-related traps are differently distributed over energy, i.e. latter being shifted toward higher energies. This strategy allowed us to perfectly represent the I_{dlin} degradation in a wide range of V_{gs}.

References

[1] A. Acovic et al, *Microel. Reliab.*, v. 36, p. 845 (1996).
[2] W. McMahon et al, *IEEE Trans. Nanotech.*., v. 2, p. 33 (2003).
[3] K. Hess et al, *Curcuits and Devices Mag.*, May 2001, p. 33.
[4] S.E. Tyaginov et al, IPFA-2010, accepted.
[5] C. Jastrzębski et al, *Microel. Reliab.*, v. 40, p. 755 (2000).
[6] P.E. Blöchl, *Phys. Rev. B*, v. 62, p. 6158 (2000).
[7] Y. Wang, *Solid-State Electron.*, v. 52, p. 264 (2008).
[8] A. Haggag et al, *IRPS-2001*, p. 271.
[9] B. Tuttle at al, *Phys. Rev. B*, v. 59, p. 12884 (1999).
[10] C. Jungemann, B. Meinerzhagen, Hierarchical Device Simulation, Springer Verlag Wien/New York, 2003.
[11] A. Bravaix et al, *IRPS-2009*, p. 531 (2009).
[12] C. Guerin et al, *Journ. Appl. Phys.*, v. 105, pap. No. 4513 (2009).
[13] W. McMahon et al, *2002 Int. Conf. Mod. Sim. Micro*, v. 1, p. 576.
[14] MINIMOS-NT Device and Circuit Simulator, User's Guide, Institute for Microelectronic, TU Wien.
[15] http://www.globalTCADsolutions.com