'Atomistic' Simulation of RTS Amplitudes Due to Single and Multiple Charged Defect States and Their Interactions

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ABSTRACT

We investigate the experimentally observed gate voltage dependence of the step heights induced by charged defects. Taking into account the intrinsic variability source of random dopants, our simulations confirm that the location of the defect with respect to the critical current percolation path affects the response of the trap to the applied gate bias. However, the details of the bias dependence of this response depend on the exact location relative to the percolation path. Furthermore, the impact of the various charge states of the defect on the step heights is investigated.

INTRODUCTION

Statistical variability introduced by discreteness of charge and matter is a major challenge for scaling and integration. It approaches more than 60% of the total variability in the 45 nm technology generation [1], and with the introduction of restricted design rules it is becoming the dominant component of the variability at the 32 nm technology generation [2]. Statistical variability already profoundly affects SRAM design, causes statistical timing problems and increasingly leads to hard digital faults. In both cases the statistical variability restricts the supply voltage scaling, adding to the power dissipation problems [3]. In addition, discrete trapped charges associated with degradation processes in combination with sources of statistical variability can result in rare but exceptionally large changes in the device parameters and also acute statistical reliability problems [4]. This is already a fundamental problem in flash [5] and DRAM memories [6], and starting to dramatically reduce the lifetime of digital chips. Charge exchange events between border states and the channel lead to random telegraph signals (RTS) in small-area MOSFETs [7].

A characteristic property of each defect is its step height, which results from the strongly correlated interaction of the defect charge with the underlying random discrete dopants (RDD) in the channel [8]. The recently suggested time dependent defect spectroscopy (TDDS) [9] now allows simultaneous monitoring of multiple defects responsible for RTS and NBTI in addition to their interaction in a single experiment. The experimentally observed step heights have been found to be much larger than expected from a simple 1D charge sheet approximation and continuous doping. In particular, the individual charged defects also display an unexpected V_G-dependence shown in Figure 1: in a previous study [8] a *decrease* of the step height with increasing gate bias was observed, while here most defects show an *increase* of the step height. In order to gain proper understanding of these effects, we have carried out full 3D physical 'atomistic' simulations in the realistic environment of a fluctuating potential landscape coming from the RDD in the channel. Since the defect responsible for charge trapping appears to be able to exist in multiple configurations, e.g. singly positive, doubly positive, singly negative, doubly negative [10], we also calculate the configuration dependence of the step heights.

SIMULATION METHODOLOGY

The simulations were carried with the well-established Glasgow atomistic drift diffusion device simulator [11], which can accurately resolve individual discrete impurities and trapped charges inside the transistor using density gradient quantum correction. A 35 nm gate length pMOSFET carefully designed using a realistic process simulator was used as a test bed device for this study. Based on the device's continuous doping profile, the simulator generated RDD by randomly placing dopant atoms on the silicon lattice sites, thereby creating a statistical sample of macroscopically identical devices with microscopically different random dopant configurations and statistically different I_D-V_G characteristics.

Density Gradient quantum corrections are implemented in the simulations to handle the artificial localisation of mobile charge in the potential wells associated with the introduction of discrete dopants [12], [13], and also to reduce the mesh-size sensitivity of the simulations, thus ensuring physically-consistent simulations. While it is
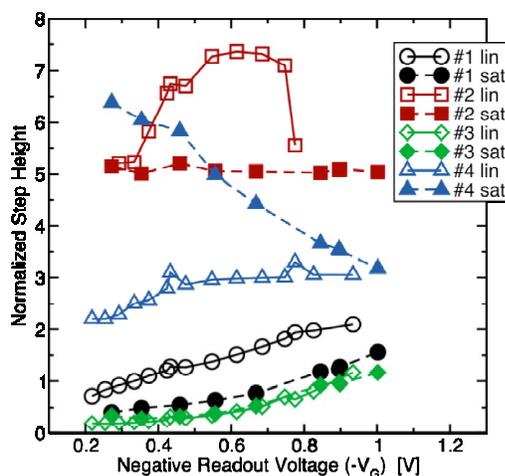

Fig. 1. Experimentally recorded step heights by single defects in a pMOSFET across varying readout voltages.
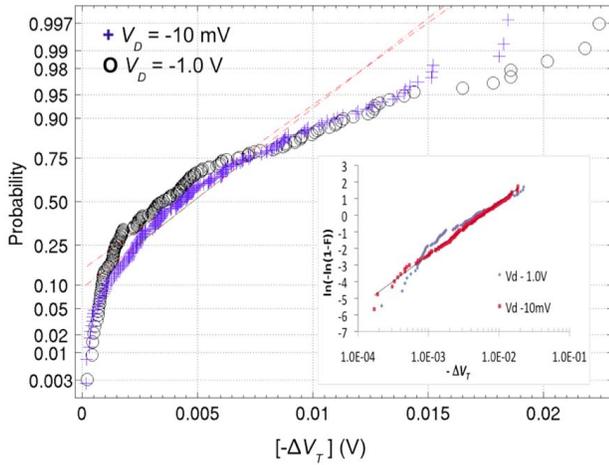
Fig. 2. The distribution of threshold voltage shifts (VT) recorded in the simulation of 200 35 nm square pMOSFETs with a single randomly positioned trapped charge at the oxide-channel interface. Inset: Same data in a Weibull plot (cf. Fig. 3).
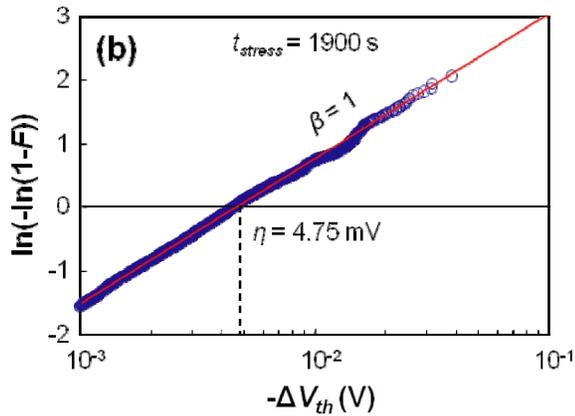

Fig. 3. Experimentally observed threshold voltage shifts due to single discharge events shown in a Weibull plot. Weibull shape factor $\beta = 1$ corresponds to an exponential distribution.
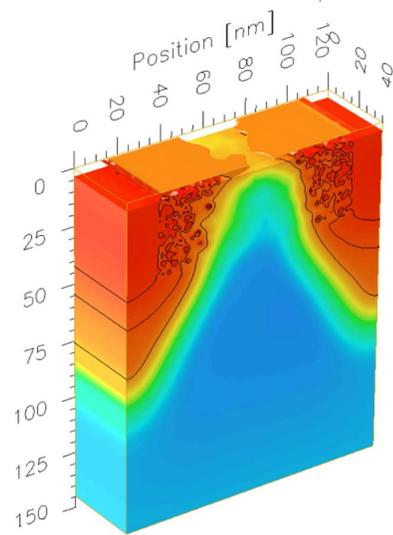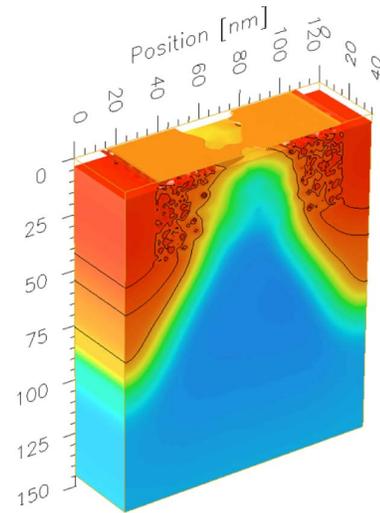

Fig. 4. Top figure shows a narrow percolation path formed in the fluctuating potential landscape of the random discrete dopants; bottom figure shows the same transistor with a single trapped charge cutting off this critical path a resulting in a giant $\otimes V_T$.

acknowledged that the drift-diffusion approach does not include non-equilibrium transport and therefore underestimates the on-state drain current in nanometer scale devices, it is well-suited for evaluating the electrostatic effects of the trapped charge through the solution of the 3-D Poisson/density gradient equations. The local carrier velocity modulation around the trapped charge is not taken into account in our simulations because carrier number fluctuations dominate the RTS amplitudes in n-channel MOSFETs, at least below and around threshold [14], [15]. However at high gate bias our simulations underestimate the current reduction due to the additional scattering from the trapped electrons, particularly at high current levels [15]. In order to select a device with a suitable configuration of RDD

which results in large RTS amplitudes as seen experimentally, a full-scale statistical simulation of 200 transistors has been performed, each with unique random doping configuration and with a randomly positioned single trapped charge at the interface. The resulting distribution of threshold voltage shifts ($\otimes V_T$) is illustrated in Figure 2, which closely replicates the experimentally measured distributions [6] shown in Figure 3. A device with a gigantic response was then selected from the tail of the distribution. Careful inspection of this particular device reveals the origin of the large $\otimes V_T \downarrow$ a narrow current percolation path formed in the landscape of fluctuating potentials of the dopant atoms exist in the 'virgin' transistor. This path is cut off when a single charge is, by chance, trapped above this path, as shown in Figure 4, resulting in a large threshold voltage shift.

In order to study the V_G-dependence behavior of the trapped charge at different strategic positions, we first mapped the aerial sensitivity of the device across its entire channel

area, as illustrated by the inset in Figure 5. Then a single trapped charge is moved across the width of the device on a path normal to the percolation path, intersecting it at the most sensitive position, while registering the resulting $\otimes V_G$ (evaluated at constant current) over a diverse range of V_G. Simulations have been carried out also for multiple charge states and the resulting gate voltage dependence $\otimes V_G$.

RESULTS

Figure 5 shows the $\otimes V_G$ (normalized to $\otimes V_T$ expected from the charge sheet approximation) as a function of the position of a single trapped charge across the width of the device, clearly showing its bias and positional dependence. The $\otimes V_G$ is calculated by the difference in the gate bias to produce a reference current, before and after the charge-trapping. When the trapped charge is in close proximity of the most sensitive position in the percolation path (the interval 20-30 nm in Figure 5), the resulting $\otimes V_G$ decreases with the increase of V_G, replicating the experimentally observed behavior of defect #4 in Figure 1 and as expected from our previous studies [8]. However, the opposite trend is observed when the trapped charge is located further away from this region, replicating the behavior of the more common other defects in Figure 1. This is also consistent with the fact that most defects show the opposite trend as reported previously, since the probability of being close to percolation path is much higher than being right in the most sensitive area of it. These responses are reproduced in Figure 6, which shows close qualitative similarities to some of the experimental measurements shown in Figure 1. Similarly to Figure 1 the responses of all defects converge at high absolute value of the gate voltage.
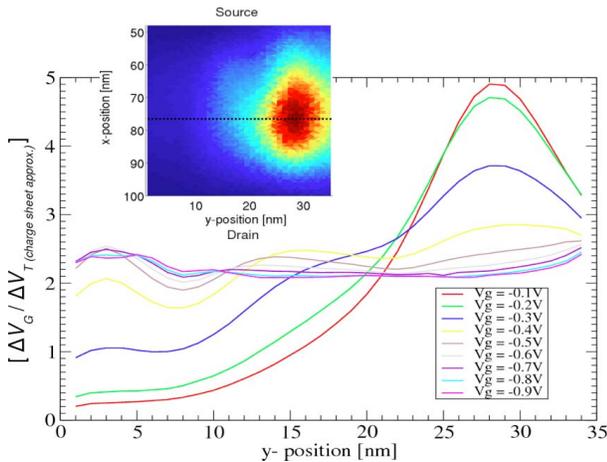
Fig. 5. The normalized VG registered by a single trapped charge at positions across the width of the device. Inset figure shows the sensitivity map of the entire channel area; the dotted line marks the path along which the trapped charge is placed. Large responses are observed when the charge is trapped in the sensitive regions, which decreases with the increase in gate bias. The opposite VG-dependence behaviour is observed when the charge is trapped further away.

Figure 7 shows the resulting step heights when a single defect existing in 4 possible charge states is placed in
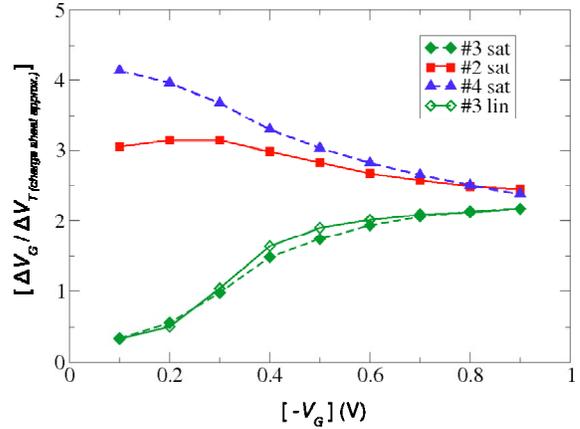
Fig. 6. The responses generated by the simulation of four different defects at various distances from the percolation path.
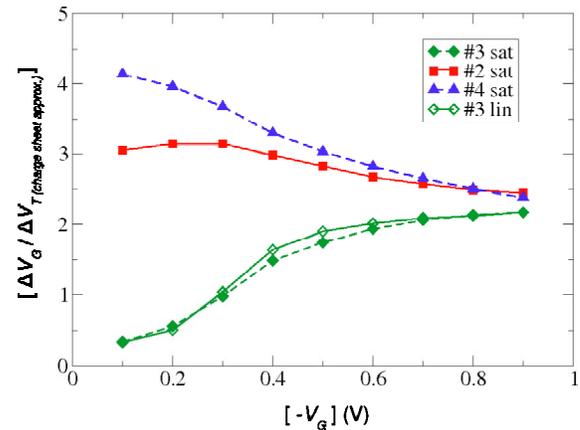
Fig. 7. Normalized VG registered with the most sensitive defect occupied by 4 possible charge state configurations. Non-symmetric response between positive and negative trapped charge is observed across the operational regime of the transistor.

the most sensitive position of the percolation path. It can be observed that: (i) In the case of a single trapped charge, a negative charge has bigger effect in sub-threshold and positive charge has bigger effect above threshold. (ii) The second positive trapped charge has a smaller effect in the sub threshold compared to the first positive charge, but has almost the same effect in strong inversion. (iii) The second negative charge has almost the same effect in sub threshold as the first negative charge, but has a smaller effect in strong inversion. Naturally, a statistical analysis of this effect is required to make a more precise statement.

CONCLUSIONS

Using 3D drift-diffusion simulation we have investigated the experimentally observed V_G-dependence of the step heights induced by charge trapping into defect states. The simulations indicate the role of the location of the trap with respect to the dominant current percolation path. When the trap is in/near

the critical path, the step height decreases with the increase in the applied gate voltage; the inverse situation happens with the trap located further away from the percolation path. The step height also depends on the charge of the trapped carriers and its configuration (single/double), and the bias condition of the transistor.

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