# The Impact of Recovery on BTI Reliability Assessments

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## ABSTRACT

BTI is shown to be the most important device degradation mechanism for combinational logic. Significant benefits regarding lifetime predictions and the total effort in measurement time can be expected from measurements minimizing recovery by a short measuring delay or/and assessments being done with AC stress for applications ensuring AC operation only.

## INTRODUCTION

Recovery after NBTI- or PBTI-stress in MOSFETs with SiON or HiK dielectric has been addressed in roughly 200 conference papers - not counting the journal papers - in the past decade [1]. The controversy about the physical origin is still ongoing. Currently a new JEDEC BTI standard [2] trying to minimize recovery effects has been prepared and will be published soon. On the other hand it has hardly been addressed yet to what degree and in which direction this recovery affects the reliability assessments. Thus one goal of this paper is to study the impact of recovery and measuring delay on predicted lifetimes. We will show that fast measurements are beneficial for both DC- and AC-stress, for SiON as well as HiK-metal gate FETs. The effect of AC-stress has long been known to have a beneficial effect on lifetime [3-5]. In the case of a 50% duty factor AC-stress the recovery occurring during the non-stressing half-periods reduces the degradation by about a factor 2 compared to DC stress. Note that due to the $\Delta VT \propto t_{stress}^n$ power law dependence, with n around 0.2, only a minor fraction of 10% of this reduction of degradation is due to the shorter net stress time for AC stress. All the conclusions drawn here will be based on the experimental facts only. Thus they will be independent of any physical models and assumptions.

## SAMPLES and MEASUREMENTS

The threshold voltage *VT* has been measured using a measure-stress-measure sequence and our ultrafast direct *VT*-measurement [6]. Measured $\Delta VT$ values for short 1 µs and long 1 s measuring delays always are from the same recovery trace (cmp. Fig. 4) and thus all comparisons fast/slow are for the **same** sample and measurement, meaning the elimination of any chip-to-chip variation. The propagation delay degradation for logic circuits under AC-stress has been measured using "aging monitors" composed from modified ring-oscillators. In these ring-oscillators the oscillation can be inhibited externally by an on-chip control unit interrupting the feedback. This way degradation due to hot carrier injection can be controlled and separated. More details on these ring-oscillator experiments have been reported recently [7].

## RELEVANCE of BTI

Fig. 1 gives a comparison for the degradation of the oscillation frequency $\Delta f$ of 3 ring oscillators (RO) stressed with the **same** amount of BTS-stress but **different** amounts of HCI-stress. The 3 RO's are identical, but the feedback of the "50% activity" RO is controlled in a way to have the RO oscillating at 50% of the full speed (≈1GHz) while the feedback of the ".01% activity" is inhibited most of the time so that the oscillation frequency is 100kHz only. Thus the "50% RO" is subjected to heavy hot carrier injection (HCI)

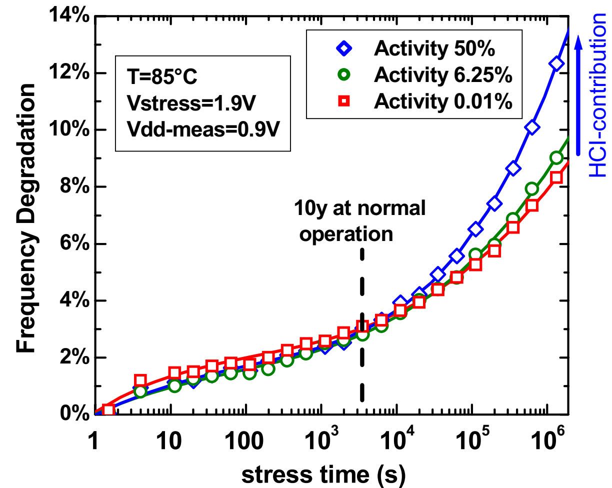


**Fig. 1** – Degradation of 40nm CMOS ring-oscillators (RO) at Vstress=**1.6****Vdd*. The "activity 0.01%" RO is toggled at a very low speed and thus "sees" only BTI stress. The "50%" RO oscillates at full speed and thus is degraded by HCI stress **in addition** to BTI. The dashed line marks the degradation reached at 10y operation at nominal *Vdd*=1.2V. (All Figs in color online)

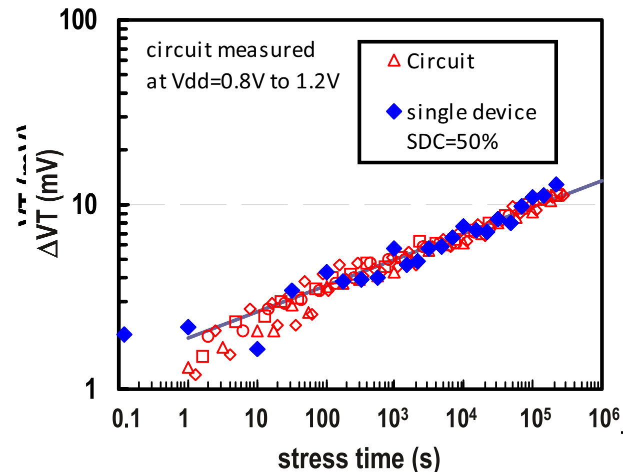


**Fig. 2** – Comparison of circuit degradation to the degradation of a single pMOSFETs. The circuit frequency degradation has been simulated by considering the pMOS $\Delta VT$ only, neglecting all other (minor) contributions. The "circuit" symbols correspond to this simulation of the measured frequency degradation at Vdd=0.8V, 0.9V.......1.2V. The single devices have been stressed at the same stress voltage / temperature as the circuits, at a frequency of 100kHz and a duty factor=50%.


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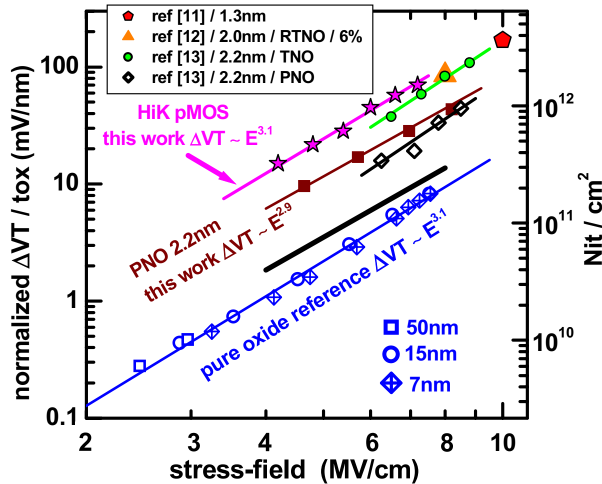


**Fig. 3** – A thickness-independent comparison of BTI degradation after $t_{stress}$=10ks at 150°C. for nitrided thin $SiO_2$, non-nitrided thick $SiO_2$ and HiK pFETs. In the legend the data taken from literature are described w: thickness / type of oxide / N content.

while the "0.01% RO" essentially does not see any HCI. Both RO's experience the same amount of BTI stress, corresponding to a 50% BTI-duty factor. As indicated in Fig. 1 for the given stress voltage of 1.6**Vdd*, a ≈4000s stress time corresponds to 10y real operation at *Vdd*. A measurable HCI contribution to the total degradation is seen only after stress times >$10^4$s. Considering that HCI has a higher field acceleration factor than BTI it becomes clear that for combinational CMOS logic the device lifetime is limited by BTI only and that HCI is negligible. Fig. 2 shows a simulation of the frequency degradation $\Delta f$ in comparison to the measured AC-$\Delta VTs$ of discrete pMOSFETs (cmp. Fig. 7). It could be shown that $\Delta f$ can be perfectly explained by considering exclusively the pMOS $\Delta VT$ shift. Though charge trapping is known to cause a mobility degradation $\Delta\mu$ in addition to $\Delta VT$ this $\Delta\mu$ mostly affects the mobility peak and may apparently be neglected to first order.

## TECHNOLOGY DEPENDENCE of BTI

The conclusions to be drawn in this paper are meant to be general for all recovery-affected BTI, that is for N/P-BTI, independent of the technology and also for HiK metal gate technologies. Thus at this point a BTI technology comparison makes sense. NBTI degradation among different publications in the literature is hard to compare in general. It is usual to give just the degradation of threshold voltage or drain current as a function of stress voltage without any normalization done. For a meaningful comparison of the amount of trapped charges created during BTI in different gate oxides it is imperative to normalize both stress voltage and $\Delta VT$. Such a normalization has been done in Fig. 3. The measured $\Delta VT$ (which is a function of the thickness) has been converted to an effective density of charged near-interface states using the relation $\Delta VT= e*N_{it} / C_{ox}$. The stress field in the oxide has been calculated from the corresponding CV-curve and Gauss' law [8] for our samples. For the literature data in Fig. 3 we used the equivalent oxide thicknesses given and estimated substrate and gate surface charge layer thicknesses. It can be concluded that there is only a minor amount of trapped charge for thick, "clean" non-nitrided oxides. For all the thin, nitrided gate oxides and HiK oxides the normalized BTI effect is about equal (within a factor 2). Most interestingly the field dependences for thick non-nitrided, thin nitrided as well as HiK are very similar (≈$E^3$) suggesting that the origin of NBTI is due to a common origin like oxide oxygen vacancies [9]. It is worth noting that FETs in CMOS circuits are operated typically around an $SiO_2$-equivalent gate field of ≈3.5 MV/cm corresponding to an inversion carrier density of $8*10^{12}cm^{-2}$, independent of the dielectric thickness.

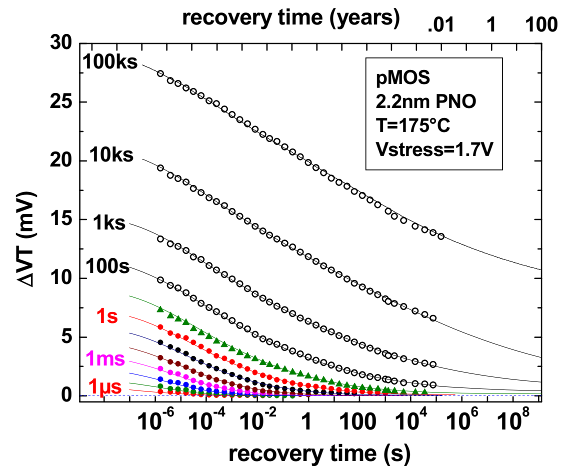


**Fig. 4** – Example for recovery traces taken after stress times from 1 µs to 100ks. (symbols=exp. data, lines=model fit). The recoverable part of $\Delta VT$ does **not saturate** after a ≈>1s stress time and even after t-rec>$10^5$s a plateau due to a permanent part is not evident. Note that the stress voltage is just 5% above nominal *Vdd*.

## EFFECT of DC-RECOVERY on ASSESSMENTS

Fig. 4 gives an example for recovery measured for very long recovery times after stress times from 1 µs to $10^5$ s. It is often claimed (e.g. in [2, 10]) that (i) the "fast" contribution due to hole trapping is saturating after ≈1 s stress time and (ii) recovery is an effect apparent at high stress fields only, and is irrelevant at use condition. Both claims are wrong in general. As clearly seen in Fig. 4 there is a continuous build-up of recoverable $\Delta VT$ for stress times *ts* far above 1 s, w/o any tendency to saturate even for *ts*>100ks. Though the electric field in Fig. 4 is only 5% above use condition, a major part of the $\Delta VT$ recovers. It is worth noting that recovery after a stress time as long as 1ks is more than 50% between a fast measuring delay of 1µs and a slow one of 1s. In contrast to the findings in [10] a plateau due to a permanent, non-recoverable contribution does not exist, due to the fact that the recovery-rate has been kept high by keeping the temperature at 175°C, rather than freezing it by cooling to 25°C.

A short measuring delay delivers higher, less recovered measured $\Delta VTs$ than a long measuring delay. Thus another wide-spread belief is that a fast measurement **decreases** the predicted lifetimes compared to a slow measurement. Quite to the **contrary**, as shown in Figs. 5 and 6, fast measurements lead to **increased** lifetimes. The root cause lies in the inevitable extrapolations which have to be done. For measurements done at high fields in general the stress times are long enough to nearly reach or even exceed the $\Delta VT$ criterions. As shown in Fig. 5 for these cases the lifetime from the slow measurement is indeed shorter than from the fast measurement. The extrapolated power law exponent (see the slope of the straight extrapolations in Fig. 5) must be **always** lower for the fast measuring delay and the "fast" curve must be **always** above the "slow" curve. When going to lower stress fields the difference in extrapolated lifetime between fast and slow measurement tends to decrease and eventually reverses the sign as the straight lines cross below the $\Delta VT$ criterion. This is shown to happen for the "-2.0V" curves for PNO in Fig. 5.

The lifetimes extrapolated (analogously to Fig. 5) to use voltages are shown in Fig. 6 for all stress voltages. Due to the recovery-driven

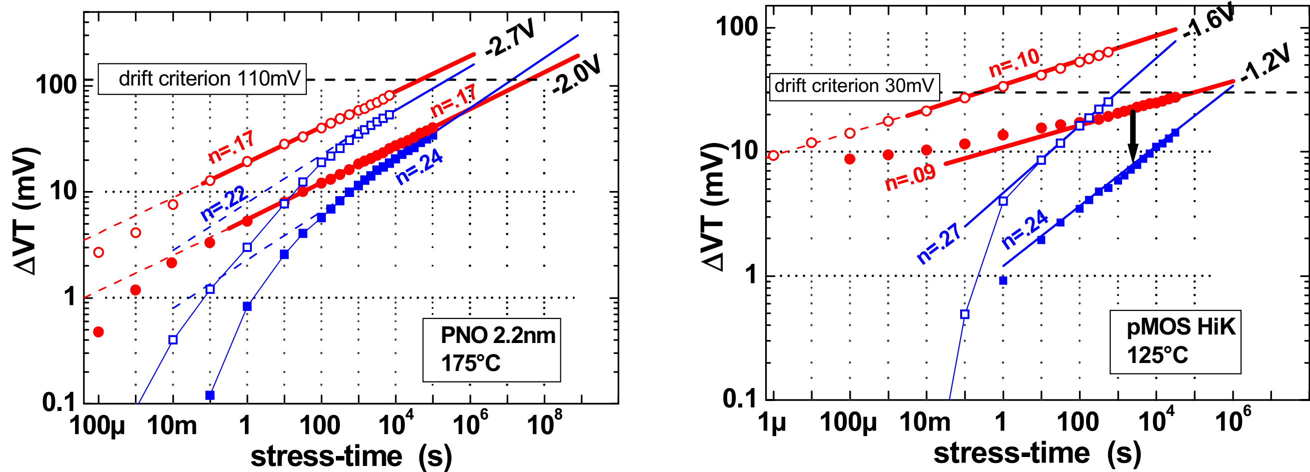


**Fig. 5** – Measured curves $\Delta VT$ vs stress-time for PNO (**left**) and for HiK (**right**). For high and low stress fields a **pair** of curves fast+slow (fast=red=thick line and slow=blue=thin line) is shown. Fast corresponds to a 1µs and slow to a 1s measuring delay. Both fast and slow are readouts taken from the **same** measurement. The black vertical arrow in the right plot marks an example for the recovery between 1µs and 1s. The curve labels denote the stress voltages and the power-law slopes $n$ in $\Delta VT \propto t_{stress}^n$. For the high fields the extrapolations to the drift criterion result in a **lower** lifetime for the fast measurement than for the slow one, due to recovery. For the low fields the differences in the slopes lead to a **higher** extrapolated lifetime for the fast measurement (cmp. crossover in left Fig.). For the fast measurement the extrapolated lifetime is (due to the straight line) independent of stress time down to stress-times as short as 10s, => a factor >100 less stress time is required. Note that recovery is much more severe for the HiK sample.

extrapolation effects the fast measurement lead to a steeper slope in the lifetime vs. stress voltage curves and thus to a significantly longer lifetime from the fast measurements. Though the difference fast/slow might be only in the mV-regime, the amount of this lifetime increase is about 1 to 2 orders of magnitude when comparing measurements with fast (1µs) and slow (1s) measuring delay. It varies with technology, stress parameters and criterions used as the comparison PNO/HiK in Fig. 5 is showing. But in general, due to the nature of recovery, short measuring delays increase the estimated lifetime.

Another most important fact is that recovery causes the "slow" $\Delta VT$ vs time data to be curved and deviating from the straight power law (see Fig. 5). Thus the slow measurements require excessively long

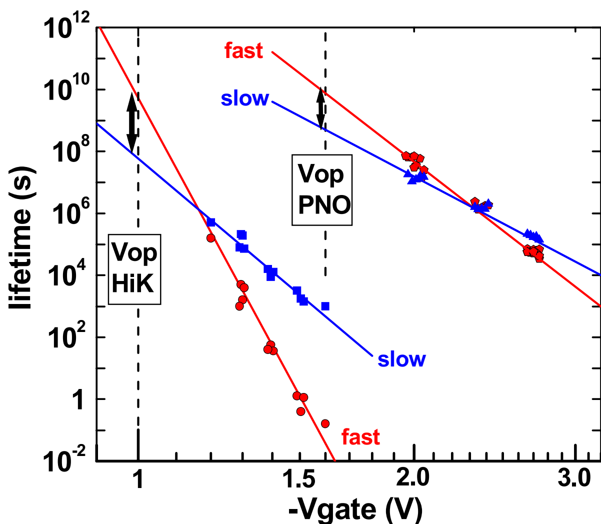


**Fig. 6** – Lifetime extrapolation (power law) from stress voltage down to operation voltage $Vop$ for fast and slow measurement. Data correspond to PNO and HiK from Fig. 5. Double arrows mark the gain in lifetime from using fast measurement technique.

measurement times in order to yield a lifetime extrapolation which is reasonably close to the "correct" straight line power law being produced by the fast measurements. In contrast the "fast" curve is a straight line down to short times; it thus allows a correct lifetime extrapolation from short measurement times. As seen for the example in Fig. 5 for the PNO case the fast measurement delivers the same perfect straight line independent of the stress time, even for the low field, as long as the stress times are at least 1000s. In contrast the slow measurement has to be at least 100ks long to get to the reasonably straight regime. Thus, for the PNO example, the whole assessment takes roughly 100 times longer with the slow measurement while still the extrapolated lifetime is a factor of 10 worse than from the fast measurement. For the HiK example the differences between the fast/slow slopes of $\Delta VT$ vs stress time are higher and do not seem to approach each other even for very high stress times.

## AC STRESS AND BENEFITS FROM AC RECOVERY

Fig. 7 shows examples of degradation due to AC stress as a function of the duty factor. The reduction seen compared to DC-stress is much larger than the one which is expected from the reduction of the net stress time. It can be explained by the repetitive recovery during the off-stress half cycles occurring during AC stress. Actually all curves $\Delta VT$ vs duty factor so far published (see [4, 14] for example), no matter if PNO-pMOS or HiK, show the same general features: A roughly flat part between 10% and 90% and a sharp increase above 90%. It should be noted that the main differences between technologies are in the amount of this increase. On the other hand this increase significantly depends on the measuring delay. For our measurements the measurement delay has been 1µs. For the AC case it is clear that the term "measuring delay" - if it is shorter than the AC-period, as in our case - only makes sense if the measurement is synchronized with the AC stress signal and the measuring delay starts right after completing the stress period of the

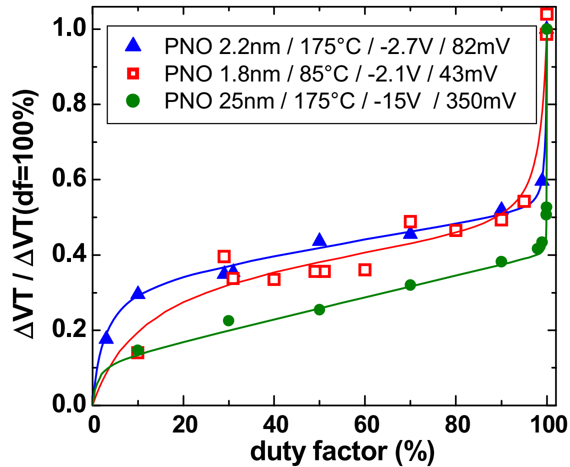


**Fig. 7** – $\Delta VT$ vs duty factor for 100kHz AC stress and $t_{stress}$=10ks, normalized to 100% duty factor. Recovery during the off-stress cycles reduces degradation significantly. Data are measured with a 1µs measuring delay, relative to the completion of the stress cycle. Data in legend denote: sample type / stress temperature / stress voltage / $\Delta VT$ after 10ks DC-stress.

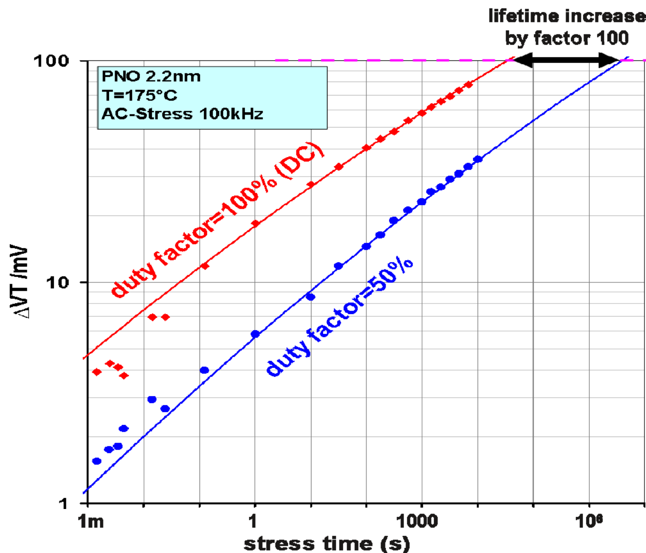


**Fig. 8** – $\Delta VT$ vs stress-time at Vstress=-2.7V for DC and a 100kHz AC stress. For a duty factor of 50% recovery reduces degradation to about 40%. Lifetime increases by a factor 100.

full AC cycle. In Fig. 8 DC- and AC- degradation are compared as a function of stress time showing a lifetime increase by a factor 100 for the given stress condition. As seen in Fig. 8 the AC- to DC-degradation ratio is almost independent of the stress time, i.e. AC and DC curve are almost parallel. This ratio also does not change significantly with the stress voltage. For logic circuits - unlike for SRAMs - AC operation with a duty factor around 50% can be taken as the operation condition. Thus NBTI degradation is reduced to 30-40% compared to DC stress, as shown in Figs. 7 and 8. Considering the $\approx$Vgate$^3$ (cmp. Fig. 2) dependence of NBTI degradation a reduction of $\Delta VT$ to 40% allows an increase of the operation voltage *Vdd* by 35% until the DC degradation level for the same operating time is reached. As seen in Fig. 9 this *Vdd* increase creates a performance increase of 50%, although at the cost of increased power consumption. Though BTI has been shown to be the most severe degradation mechanism it has to be carefully checked if other

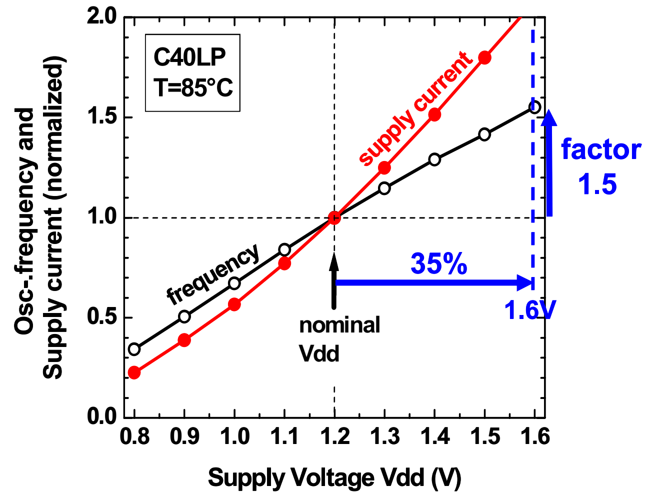


**Fig. 9** – Performance increase for ring oscillators due to a *Vdd* increased above the nominal *Vdd* of 1.2V, for a 40nm CMOS technology with 1.8nm PNO (cmp. Figs. 1, 7). The reduced degradation under 50% AC stress allows a 35% increase of *Vdd* corresponding to a 50% performance increase (at no extra cost). A penalty is the increased supply current.

degradation mechanisms (like TDDB) might inhibit such a large increase of operation voltage.

## CONCLUSION

**(1)** Assessments with a µs measuring delay allow for a much shorter (typ. factor 100) total stress time compared to a standard 1s delay because $\Delta VT$ vs stress-time is a straight curve in contrast to the long measuring delay (see Fig. 5).
**(2)** The predicted DC lifetime prediction obtained from fast 1µs-delay measurements is roughly a factor 10...100 longer than that obtained from a slow 1s measuring delay. A delay of some ms as proposed in [2] will lie in the middle between 1µs and 1s.
**(3)** Recovery during AC stress brings about a lifetime increase by typically a factor 100. For combinational logic applications this huge increase may be converted into a significant performance increase by increasing the supply voltage *Vdd*, keeping other constraints in mind.
**(4)** Recovery is qualitatively independent of the type of dielectric; thus our conclusions are valid for all types of samples (thin, thick nitrided, pure $SiO_2$ or NBTI/PBTI in HiK).
**(5)** Recovery after stress at electric fields corresponding to use condition (cmp. Fig. 4)or even far below [15] is equally important as at high stress fields.

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## Questions and Answers

Q1: p. 5: Is this more recent data than your previous IRPS work?

A1: Yes, these data, except another version of the inter-technology-comparison Fig. 3, have not been published in IRPS. Figs. 1 and 2 are from ref [7].

Q2: When the two cross over between fast and slow measurement techniques, should the slow merge to the fast and not cross over it?

A2: Due to recovery the $\Delta VT$ from the fast measurement is always larger than the one from the slow measurement. Due to the log vertical axis “fast” and “slow” curves in Fig. 5 look as if they would merge. In fact the difference $\Delta VT_{fast}$ - $\Delta VT_{fast}$ must be monotonously increasing with stress time. For example in Fig. 4 the difference in $\Delta VT$ between recovery time 1µs and 1s increases from stress time 1µs, 1ms ......100ks. There can never be a crossover of the **measured** $\Delta VT$ vs stress times curves. The crossover only can happen in the extrapolations of the curves.

Q3: Is the ^3 dependence based on Degradation or Time to failure?

A3: As seen in Fig. 3 the dependence of $\Delta VT$ on electric field $E$ is $\Delta VT \propto E^3$. For NBTI a typical dependence of $\Delta VT$ on stress time $ts$ is $\Delta VT \propto ts^{0.15}$ . Thus the time to failure $TTF$ goes with electric field $E$ like: $TTF \propto E^{-3/0.15} = E^{-20}$