Depth localization of positive charge trapped in silicon oxynitride field effect transistors after positive and negative gate bias temperature stress

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Positive charge trapped in the SiO(N) gate dielectric of deeply-scaled p-channel metal-oxide-semiconductor field-effect transistors is observed after both negative and positive gate bias temperature stress. Emission of elementary trapped charges is demonstrated and analyzed through the quantized threshold voltage transients observed after stress. The magnitude distribution of the threshold voltage steps is used to estimate the depth of the traps in the gate dielectric to be about 0.5 nm from the injecting silicon-dielectric interface in both cases. *© 2011 American Institute of Physics*. [doi:10.1063/1.3586780]

The negative bias temperature instability (NBTI) is one of the most serious reliability issues in p-channel metal-oxide-semiconductor field effect devices (pMOSFETs).[1] NBTI manifests itself as a negative threshold voltage shift (ΔV_{TH}) produced after the application of a negative gate bias at elevated temperature in pMOSFETs. This effect is due to the trapping of positive charge injected from the silicon substrate inversion layer.[2] In *polysilicon* pMOSFETs, negative ΔV_{TH} is also observed after *positive* gate bias stress.[3,4] We argue that this observation is in fact produced by the same mechanism as NBTI but with the positive charge originating from the polysilicon depletion layer. Additionally, the total ΔV_{TH} is, to the first order, proportional to the product of the trapped charge Q and the centroid of the charge distribution $\langle x_0 \rangle$, i.e., $\Delta V_{TH} \propto Q \times \langle x_0 \rangle$.[5,6] In order to separate the two contributing components, either the oxide charge Q or the centroid $\langle x_0 \rangle$ must be known independently.

Recently, *quantized* NBTI V_{TH} relaxation transients observed in nanoscaled devices have been explained by the emission of *individual* trapped holes from the dielectric.[9] Therefore, in this case the oxide charge Q is equal to the elementary charge q and thus known for each event. In this work, we rely on the *quantized NBTI V_{TH}* relaxation transients to assess the average depth of the trapped positive charges in nitrided silicon oxide SiO(N) dielectric gate after positive and negative stress. We find that the positive charge is captured at ~ 0.5 nm from the Si/oxide interface under the stress conditions of the experiment.

Deeply scaled pMOSFETs with SiO(N) gate dielectric and polysilicon (poly-Si) gate electrode were used in this experiment. Two wafers were studied; both of them followed the same process flow except for the SiO(N) deposition that resulted in two different SiO(N) thicknesses, 1.86 nm and 1.42 nm. The devices were gate stressed at either positive or negative 7 MV/cm oxide electric field for 2.3 s at 125 °C. The oxide electric field was determined from the fit of the capacitance voltage curves using the NCSU CVC program.[7]

The characteristic quantized V_{TH} relaxation transients for the deeply scaled pMOSFETs with 1.86 nm-SiO(N), drawn gate length $L=70$ nm and gate width $W=90$ nm after negative and positive stress conditions are shown in Fig. 1. As also seen for large gate area devices,[3,4] a negative V_{TH} shift is observed for both stress polarities. The discrete V_{TH} drops are single *hole* emission events from individual traps.[8] The number of discrete V_{TH} drops per device follows a Poisson distribution (not shown). The large step heights are caused by the nonuniform inversion charge caused by the random dopant fluctuations in the pMOSFET channel. This inversion charge can be modified by the capture and emission of individual oxide traps, thus varying the drain current I_D.[9] Taking the I_D-V_G curve of the fresh device as a reference, the changes in the drain current I_D can be transformed into the V_{TH} shift.

Comparing Figs. 1(a) and 1(b), we note that both the total V_{TH} shift and the magnitude of the step heights are lower for the case of positive gate stress. This becomes more evident in Fig. 2, where the averaged relaxation traces of 74 devices after positive and negative stress are plotted together. The resulting curves resemble the continuous curves obtained in large gate area devices for both negative and positive stress conditions (not shown here). This corroborates the assumption that the relaxation transients obtained on large devices are the result of the emission of multiple holes trapped in the gate dielectric.

The complementary cumulative distribution functions (CCDFs) of the step heights from Fig. 1 displayed in Fig. 3 further demonstrate that larger step heights are seen after negative stress. Both CCDFs follow an exponential distribution[10]

$$\mathrm{CCDF}(\Delta V_{TH}, \eta) = \exp\left(-\frac{|\Delta V_{TH}|}{\eta}\right), \quad (1)$$

where $\eta(=\langle \Delta V_{TH} \rangle)$ is the average step height for a single discharge. The normalizing constant for both CCDFs plotted in Fig. 3 N_t was ~ 150 for both polarities. This constant

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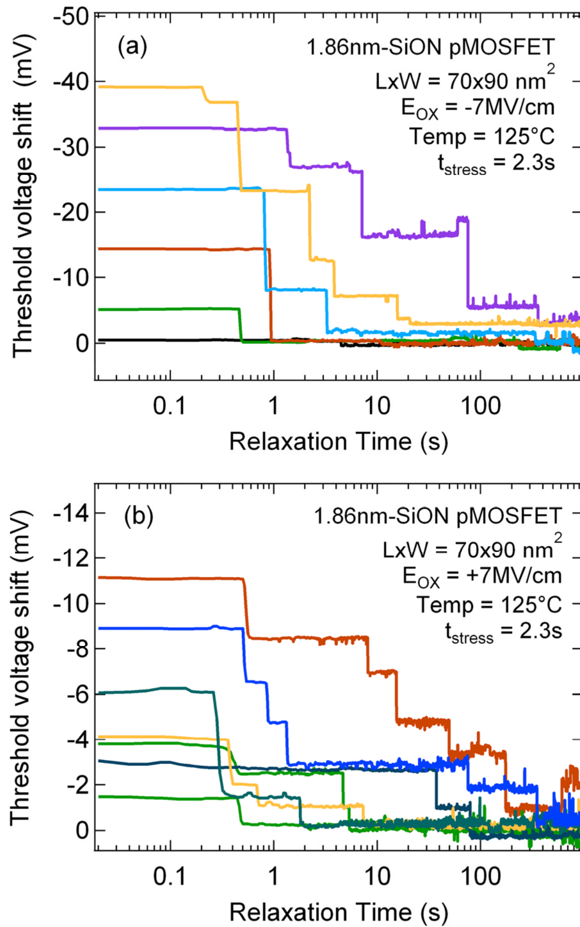

FIG. 1. (Color online) Selected relaxation (i.e., charge emission) transients after (a) negative and (b) positive gate bias temperature stress registered in different 70×90 nm^2 pMOSFETs with 1.86 nm-SiO(n). The time scale corresponds to the relaxation time after the stress voltage removal. Regardless of the stress polarity, a negative V_{TH} shift is observed. However, lower total ΔV_{TH} and lower step heights are measured in pMOSFETs after positive stress.

represents the total number of the emitted holes per 74 devices, that is about two emitted holes per device. The close value obtained for N_t under both conditions indicates that the number of positive charge trapped during both stress conditions was roughly the same. On the other hand, η is equal to

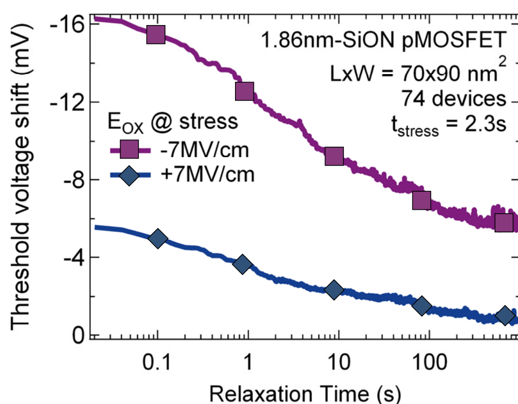

FIG. 2. (Color online) Relaxation curves obtained by averaging individual relaxation transients (see Fig. 1) from 74 different devices after positive and negative bias temperature stress. The obtained curve resembles the recovery behavior of large devices demonstrating the link between hole emission from individual traps and the relaxation component of NBTI.

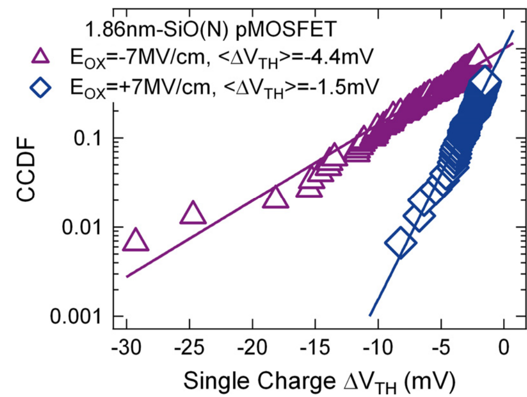

FIG. 3. (Color online) CCDFs of step heights for 74 pMOSFETs after negative and positive stress conditions follow an exponential distribution. The expected single V_{TH} shifts η obtained from the fit were -4.4 and -1.5 mV for negative and positive stress, respectively.

-4.4 and -1.5 mV for the negatively and positively stressed devices, respectively (Table I). We interpret this disparity as the consequence of the different average distance $\langle x_0\rangle$ (i.e., the depth) of the trapped holes in the oxide from the polysilicon gate after positive and negative stress conditions, as sketched in Fig. 4. This discrepancy allows us to estimate the average positive charge position when two simple assumptions are made. First, the average distance $\langle x_T\rangle$ from the injection interface (the substrate for the negative stress and the polysilicon for the positive stress) to the trapped holes is equal for both stress polarities. This assumption will be correct provided that the tunneling probabilities to both interfaces are comparable. The tunneling probability does not depend strongly on the electronic barrier between Si and SiO(N) but rather on the vibrational barriers.[11] Since the absolute value of the electric field is identical in both cases and the defect properties at the two interfaces are analogous, the tunneling probabilities can be expected to be practically identical. Second, the average threshold voltage shift produced by the single discharge $\eta=\langle\Delta V_{TH}\rangle$ is proportional to the charge centroid $\langle x_0\rangle$ from the polysilicon for negative and positive stress conditions, respectively, i.e.,

$$\eta(V_{\mathrm{STRESS}}<0)\propto(t_{\mathrm{SiON}}-\langle x_T\rangle) \tag{2}$$

and

$$\eta(V_{\mathrm{STRESS}}>0)\propto\langle x_T\rangle. \tag{3}$$

The ratio between the average single discharge η for negative and positive stress readily yields the expected $\langle x_T\rangle$ as

$$\langle x_T\rangle=t_{\mathrm{SiON}}\frac{\eta(V_{\mathrm{STRESS}}>0)}{\eta(V_{\mathrm{STRESS}}>0)+\eta(V_{\mathrm{STRESS}}<0)}. \tag{4}$$

TABLE I. Average step heights η produced by the emission of a single positive charge after negative and positive bias stress conditions for the two stacks studied in this experiment.

	Electric field (MV/cm)	
	-7	$+7$
$\eta(t_{\mathrm{SiON}}=1.86$ nm) (mV)	-4.4	-1.5
$\eta(t_{\mathrm{SiON}}=1.42$ nm) (mV)	-1.5	-0.8

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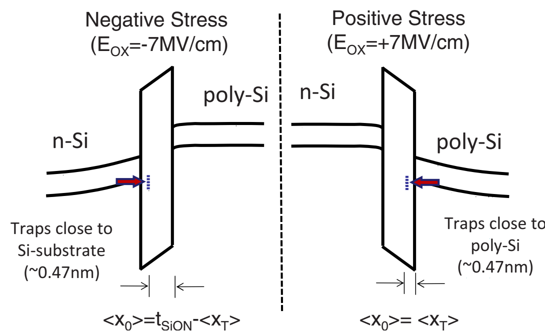

FIG. 4. (Color online) Band diagrams of the 1.86 nm-SiO(n) pMOSFET gate stack under the two stress conditions of the experiment. Holes are trapped closer to the gate after positive stress.

Substituting the values of η (see Table I) for the devices with 1.86 nm SiO(N) in Eq. (4), we obtain the average depth of the trapped positive charge $\langle x_T \rangle$ equal to 0.47 nm.

The experiment was repeated on a wafer with a thinner SiO(N) layer (t_{SiON}=1.42 nm) and slightly larger drawn gate size ($L \times W = 100 \times 100$ nm^2). The oxide electric field and the stress time were identical for positive and negative stress, resulting again in approximately the same number of defects, indicated by similar normalizing factors for both CCDFs. In this case, the average step heights η were -1.5 and -0.8 mV for the negative and the positive stress, respectively (Table I). Lower η values but higher normalizing factor for the CCDFs are obtained as expected for larger area devices ($L \times W = 100 \times 100$ nm^2), corresponding to a larger total number of defects but with a smaller average impact in the total threshold shift.[9] The trap position $\langle x_T \rangle$ obtained from these values via Eq. (4) is 0.49 nm.

The similar $\langle x_T \rangle$ values obtained from both the 1.86 nm and 1.46 nm SiO(N) pMOSFET devices (see Table I) lead us to conclude that under identical stress conditions (the oxide electric field and the stress time), the average trap position of the injected holes is equal.

In conclusion, the average depth position of positive trapped charge in poly-Si/SiO(N)/p-Si FETs has been determined by means of studying individual hole emission events after positive and negative stress.

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