Cryogenic to Room Temperature Effects of NBTI in high-k PMOS Devices

Richard G. Southwick III[1], Shem T. Purnell[1], Blake A. Rapp[1], Ryan J. Thompson[1], Shane K Pugmire[1], Ben Kaczer[3], Tibor Grasser[4], and William B. Knowlton[1,2]

[1]Dept. of Electrical and Computer Engineering,
[2]Dept. of Materials Science and Engineering; Boise State University; 1910 University Dr.; Boise, ID 83725 USA
208-426-5705; fax: 208-426-2470; e-mail: bknowlton@boisestate.edu
[3] IMEC, Kapeldreef 75, L3001, Leuven, Belgium; email: kaczer@imec.be
[4]Christian Doppler Laboratory for TCAD in Microelectronics, Institute for Microelectronics
Technische Universität Wien,1040 Wien, Austria; email: grasser@iue.tuwien.ac.at

ABSTRACT

We present experimental evidence that trapping mechanisms contributing to the negative bias temperature instability (NBTI) of high-k dielectric p-channel metal oxide semiconductor (pMOS) transistors are thermally activated. Device behavior during stress and recovery from 300 K down to 6 K indicate the dominance of the hole trapping mechanism commonly attributed to NBTI is reduced as temperature decreases. Further, trends in the temperature dependence of drain current shifts suggest more than one mechanism is responsible for NBTI. Specifically, below 240 K, current degradation immediately following stress is no longer observed. In fact, the opposite effect occurs, which is suggestive of electron trapping as the dominant mechanism at such temperatures.

INTRODUCTION

Shifts in crucial device parameters as a function of stress time can be observed when applying a negative bias to the gate of pMOS transistors. Upon removal of the negative stress voltage, the device characteristics are observed to recover. Hole traps and interface states have long been suspected to be the cause of degradation and recovery. A critical aspect of NBTI models hinges on the temperature dependence of the hole trapping component. While temperature independent hole trapping is still used to model NBTI [1], a growing body of evidence suggests that hole trapping is an inelastic process with a large temperature dependence [2-5]. However, these studies focus mostly on measurements performed at room temperature and higher.

A natural extension in the investigation of the temperature dependence of the hole trapping component of NBTI is to perform measurements down to cryogenic temperatures where temperature dependent processes can be suppressed. We performed just such an experiment on 2 nm SiO_2 pMOSFET devices which showed absence of drain current recovery at temperatures below ~140 K [6]. The work described here builds on that original work by examining the cryogenic to room temperature dependence of more relevant HfO_2/SiO_2 pMOSFETs where NBTI continues to be a reliability concern [7].

EXPERIMENTAL

The devices used in this study are high-k dielectric pMOSFETs with a 1.8nm HfO_2/1nm SiO_2 oxide layer. Device sizes are 10μm wide by 0.5μm length and 10μm wide by 0.35μm length fabricated in a 65nm technology by IMEC. Devices were stressed and recovered at temperatures ranging from 300K to 6K in 25K increments using a Keithley 4200SCS with remote pre-amps. Temperature control was achieved using a Janis Research variable temperature probe station (VTPS) with actively cooled probes. Devices were stressed (V_{Stress}) at either V_{Gate} = -1.8 V or -2 V for 100 seconds and relaxed at $V_{Gate} \approx$ threshold voltage, V_{th}, for 1000 seconds while monitoring the drain current. Drain current versus gate voltage, I_{Drain}-V_{Gate}, measurements with V_{Drain} = 50 mV or 0.1 V were taken prior to stressing the devices as well as at 10, 100, and 1000 second intervals during relaxation using a small gate voltage sweep range of V_{th} - 0.1 V to 0 V. Gate leakage current versus gate voltage tests (I_{Gate}-V_{Gate}) were also taken before stress and after relaxation over the same gate voltage range to monitor oxide degradation. The small gate voltage sweep range was used to minimize disruption to the device before stress. The final measurement performed was an I_{Drain}-V_{Gate} sweep from the stress voltage, V_{Stress}, to 0 V. These measurements are summarized in Table I.

Special care was taken to ensure the device temperature was held constant. An example of a device not in thermal equilibrium is shown in Fig. 1. In Fig. 1, the drain current is monitored at $V_{Gate} \approx V_{th}$ immediately after probing. A large change in the drain current is observed with a characteristic 'S' curve resulting from the device moving to thermal equilibrium. In Fig. 1, the device was placed on the stage using the force of gravity to create contact with the cryostage. This procedure resulted in poor thermal conductivity with the stage leading to a large time constant for the sample to become thermally stable. The time constant of this transient is significantly reduced with the application of thermal grease and metal clamps to increase thermal conductivity with the stage. It is the belief of the authors that the 'abnormal' NBTI we reported earlier in [6] were the result of insufficient thermal coupling of the device to the thermal chuck.

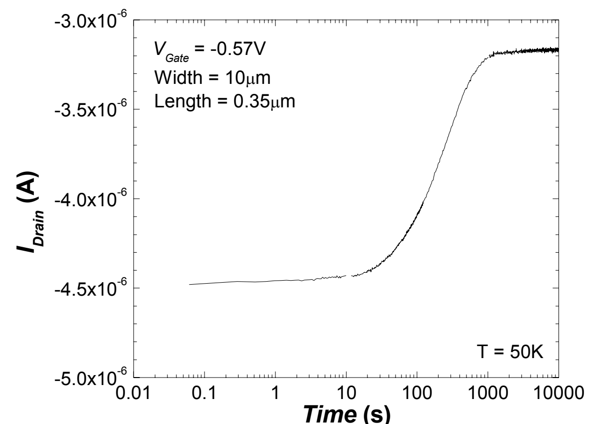

Fig. 1: Characteristic 'S' curve response of the drain current as the pMOSFET moves to thermal equilibrium with the stage after being heated due to illumination during probing.

978-1-4577-0115-3/11/$26.00 ©2011 IEEE

To promote device thermal stability, samples used in this experiment were mounted to the VTPS chuck using a thin layer of Apiezon N-grease and metal clamps. After device probing, the samples were placed in the dark for a minimum of 1000 seconds to allow the samples to recover from temperature gradients induced by light exposure during probing. As confirmation that no thermal instabilities were present in the device prior to characterization, a stability test was performed where the drain current is monitored for 1000 s while $V_{Gate} \approx V_{th}$. Devices were used for multiple temperatures (i.e., a fresh device was not used for each temperature). Devices were allowed to relax for a minimum of ~3 hours before being tested again.

Table I: Device Characterization Test Suite

1	Device kept dark for 1000 s after probing
2	Stability test 1000 s: $V_{Gate} \approx V_{th}$; V_{Drain} = 50 mV or 100 mV
3	I_{Gate}-V_{Gate}: V_{Gate} swept ~V_{th} – 0.1 V to 0 V
4	I_{Drain}-V_{Gate}: V_{Gate} = ~V_{th} – 0.1 V to 0 V; V_{Drain} = 50 or 100 mV
5	Stress for 100 s: V_{Gate} = -1.8 or -2 V; V_{Drain} = 50 mV or 100 mV
6	Relax for 10 s: $V_{Gate} \approx V_{th}$; V_{Drain} = 50 mV or 100 mV
7	I_{Drain}-V_{Gate}: V_{Gate} = ~V_{th} – 0.1 V to 0 V; V_{Drain} = 50 or 100 mV
8	Relax for 90 s: $V_{Gate} \approx V_{th}$; V_{Drain} = 50 mV or 100 mV
9	I_{Drain}-V_{Gate}: V_{Gate} = ~V_{th} – 0.1 V to 0 V; V_{Drain} = 50 or 100 mV
10	Relax for 900 s: $V_{Gate} \approx V_{th}$; V_{Drain} = 50 mV or 100 mV
11	I_{Drain}-V_{Gate}: V_{Gate} = ~V_{th} – 0.1 V to 0 V; V_{Drain} = 50 or 100 mV
12	I_{Gate}-V_{Gate}: V_{Gate} swept ~V_{th} – 0.1 V to 0 V
13	I_{Drain}-V_{Gate}: V_{Gate} = -2 V or -1.8 V to 0 V; V_{Drain} = 50 or 100 mV

RESULTS AND DISCUSSION

Typical drain currents measured during stress and relaxation are shown for 300 K in Fig. 2*a* and *b* respectively. In Fig. 2, the drain current is observed to degrade (reduce in magnitude) during stress and recover during relaxation. This behavior is the typical NBTI behavior reported in devices stressed above room temperature and thus expected. During the relaxation test, Fig. 2*b*, the test was interrupted twice to perform I_{Drain}-V_{Gate} measurement. The low gate voltages applied during I_{Drain}-V_{Gate} measurements increased device relaxation as observed by the jump in magnitude of I_{Drain} at 10 s. Device relaxation occurs faster the more positive the gate bias is applied during relaxation [8]. As the I_{Drain}-V_{Gate} measurement sweeps a voltage range down to zero V_{Gate} (Table I tests 7 and 9), larger drain currents are expected (associated with more recovery) during the rest of the relaxation test (Table I, tests 8 and 10).

Typical drain currents measured during stress and relaxation for 6 K are shown in Fig. 3*a* and *b,* respectively. While the drain current decreases in magnitude during stress at 6K, Fig. 3*a* (similar trend as 300 K), the current is observed to *also decrease in magnitude* during relaxation, Fig. 3*b*, an unexpected NBTI behavior. Discontinuities in the drain current during relaxation appear at 10 s and 100 s where I_{Drain}-V_{Gate} measurements were performed.

Focusing first on the relaxation trend differences between 300 K and 6 K, plots of the initial I_{Drain}-V_{Gate} measurement (Table I test 4) and the I_{Drain}-V_{Gate} measurements performed during relaxation at 10 s, 100 s, and 1000 s (Table I test 7, 9, and 11) for 300 K and 6 K devices are shown in Fig. 4 and Fig. 5, respectively. A magnified portion of the data is shown in the inset of Fig. 4 and Fig. 5.

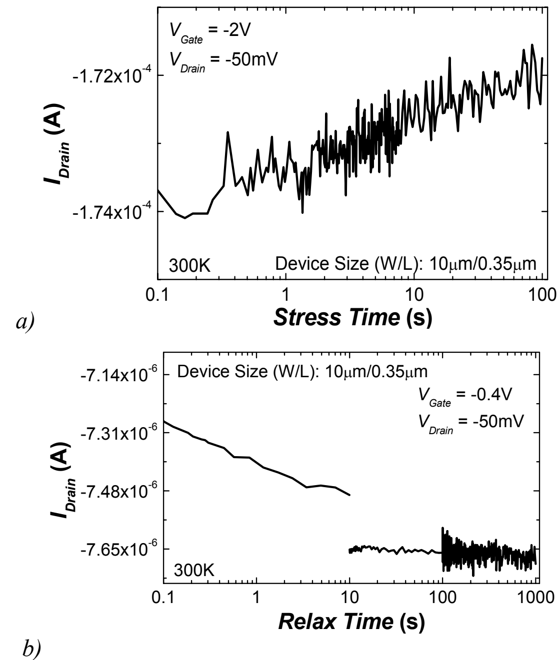

Fig. 2: Example of an NBTI *a*) stress and *b*) relaxation test performed at 300 K. Degradation in the drain current is observed during stress. Following stress the drain current is measured during relaxation. An increase in the drain current is observed during relaxation, a sign of recovery. The relaxation test was interrupted at 10 s and 100 s to perform low voltage I_{Drain}-V_{Gate} measurements.

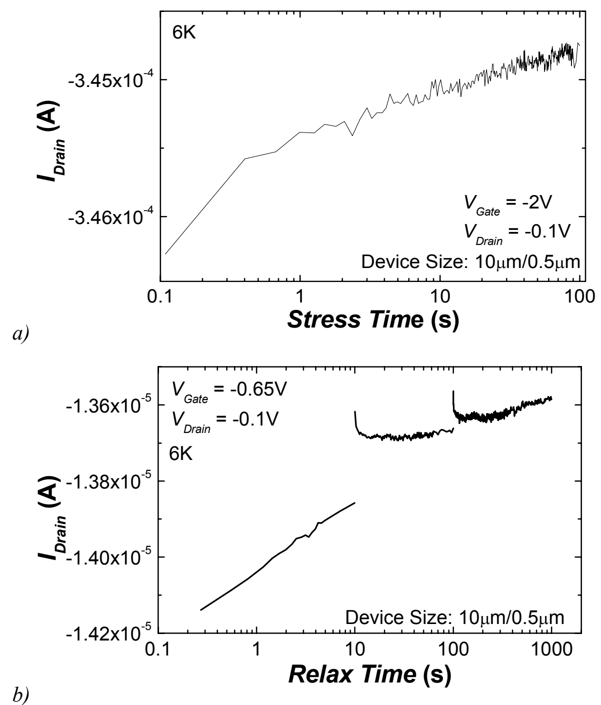

Fig. 3: NBTI stress (upper graph) and relaxation (lower graph) tests performed at 6 K. Degradation in the drain current is observed during both stress and recovery. The relaxation test was interrupted at 10 s and 100 s to perform low voltage I_{Drain}-V_{Gate} measurements leading to the observed discontinuities.

Fig. 4 indicates a shift to the left occurs during stress (between Pre-Stress and 10 s Relax) at 300 K followed by a shift to the right (between 10 s, 100 s, and 1,000 s Relax) during relaxation as indicated by the arrows. This behavior is expected in NBTI and consistent with positive charge accumulating in the oxide during stress and being removed from the oxide during relaxation. However, Fig. 5 indicates a shift to the right occurs during stress at 6 K followed by a shift to the left during relaxation as indicated by the arrows. This behavior is *not* consistent with positive charge but with negative charge accumulation and removal from the gate oxide during stress and relaxation, respectively.

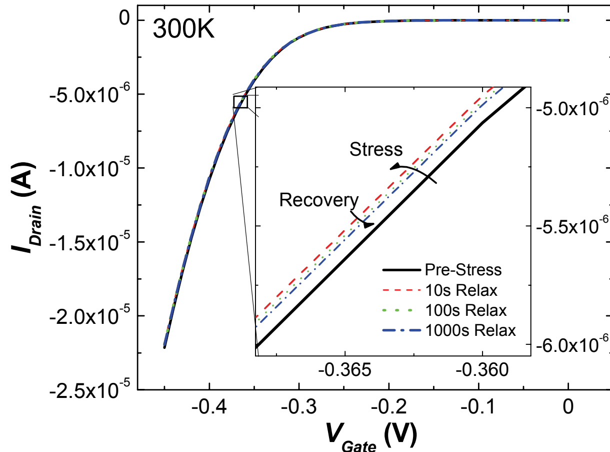

Fig. 4: I_{Drain}-V_{Gate} tests performed before stress, and after 10 s, 100 s, and 1000 s of relaxation at 300 K. The I_{Drain}-V_{Gate} curve is observed to move to the left following stress and then to the right during recovery.

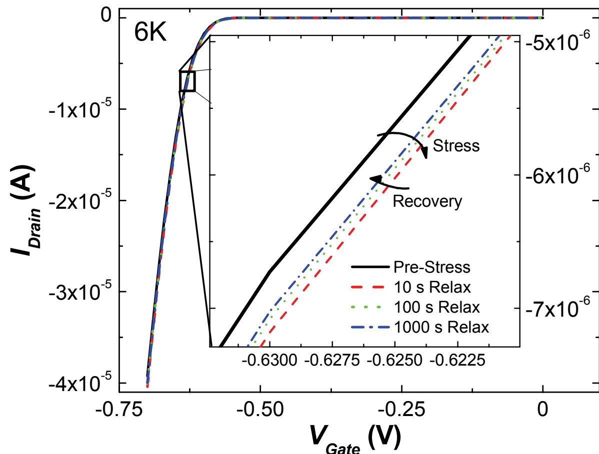

Fig. 5: I_{Drain}-V_{Gate} tests performed before stress, and after 10 s, 100 s, and 1000 s of relaxation at 6 K. The I_{Drain}-V_{Gate} curve is observed to move to the *right* following stress and then to the *left* during recovery.

Negative charge accumulation in the gate oxide (a threshold voltage shift to the right) during stress at 6 K, however, appears inconsistent with the drain current degradation during stress shown in Fig. 3a. Drain current degradation is usually an indicator of a threshold voltage shift to the left not right in pMOSFETs. An I_{Drain}-V_{Gate} measurement to the stress voltage (Table I test 13) is shown in Fig. 6 for temperatures ranging from 6 K to 300 K. Examining the drain current trends as a function of gate voltage near V_{Stress} (-1.8 V in this case) at 300 K in Fig. 6 indicates, that a pure threshold voltage shift to the left (a horizontal movement of the curve to the left) would result in a decrease in the drain current magnitude during stress. Examining the drain current as a function of gate voltage at the stress voltage for 6 K reveals a trend with negative slope. This implies that, for the drain current to degrade during stress at 6 K (Fig. 3a), a threshold voltage shift to the right is occurring. A threshold voltage shift to the right during stress is consistent with Fig. 5 and implies negative charge accumulation during stress at 6 K. It is important to note that, for a wide range of temperatures at V_{Stress}, Fig. 6 shows a slope nearly zero. Determining whether positive or negative charge accumulation is occurring in the gate oxide during stress from shifts in the drain current measured during stress are therefore difficult to determine in these temperature ranges. This difficulty is further complicated if considering transconductance degradation in addition to V_{th} shifts.

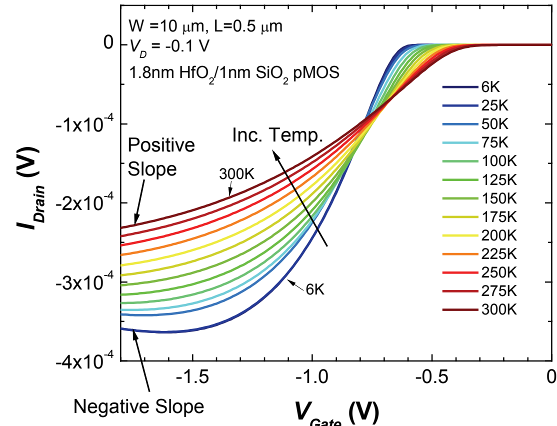

Fig. 6: I_D-V_G sweeps from 6 K to 300 K from V_{Stress} to 0 V. The slope of the I_{Drain} is negative for T < ~50 K for V_{Stress} = -1.8 V and negative for T < ~150 K for V_{Stress} = -2 V (not shown).

Self-Heating?

While the data indicates that negative charge accumulation is occurring in the oxide during stress and removed during relaxation at 6 K, it is important to ask if temperature transients from self-heating also explain the data. Large shifts in the drain current can occur with slight changes in the temperature as was indicated with the discussion of Fig. 1. Using the I_{Drain}-V_{Gate} measurements collected over the entire temperature range investigated, the sensitivity of I_{Drain} vs. temperature can be determined for any particular gate bias. Fig. 7 shows the drain current as a function temperature for a gate bias near V_{th} (at 100 K), as indicated by the open square in the figure. The corresponding stability (Table I test 2) and relaxation tests (Table I tests 6, 8, and 10) to the device in Fig. 7 are shown in Fig. 8.

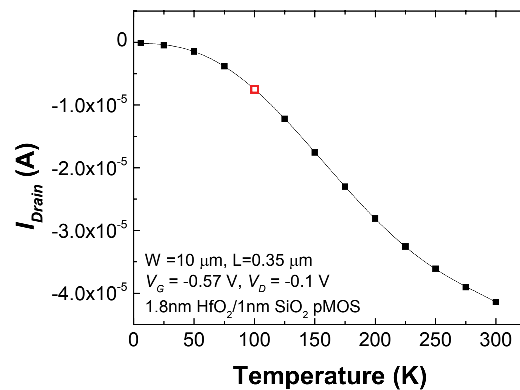

Fig. 7: Drain current as a function temperature for V_{Gate} near V_{th} when at 100 K. This figure corresponds to the stability measurement and relaxation measurement shown in Fig. 8.

Fig. 8 shows a slight increase in the magnitude of the drain current during the stability measurement while significant current decrease is observed after stress. Using the data from Fig. 7, only an increase of 0.4 K is needed to increase the drain current by the amount shown during the stability measurement. If the device is self-heated during stress (a drain bias of -0.1 V is used in this device during stress to monitor the drain current, corresponding to I_{Drain} = 326 μA), the relaxation curve would correspond to a 3.7 K decrease in temperature. While temperature monitor records of the cryostat show temperature control to within 0.01 K at the chuck during measurement, local heating in the device is possible.

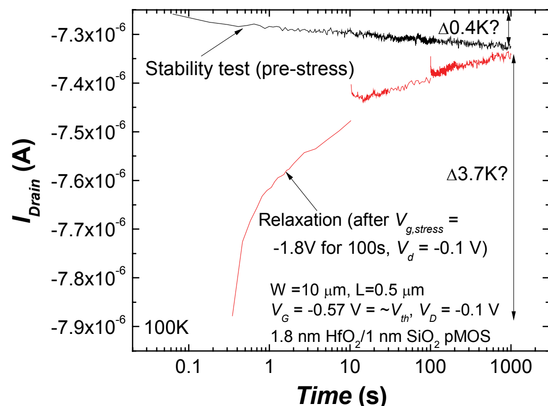

Fig. 8: Drain current as a function of time taken before stress (stability test) and after stress (relaxation) at 100 K. Calculated changes in temperature (from Fig. 7) are shown, indicating the level of self-heating required to account for changes in I_{Drain}.

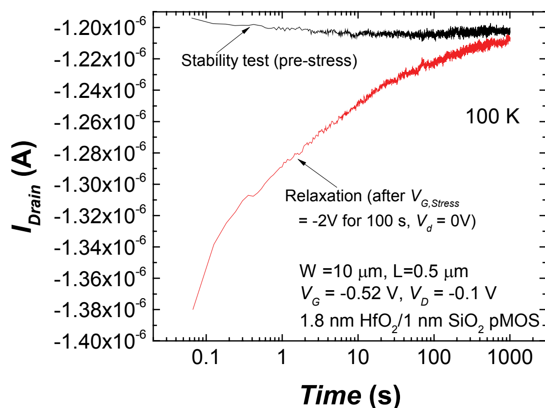

Fig. 9: Drain current as a function of time; measured before stress (stability test) and after stress (relaxation) at 100 K. The drain bias for stress was set to zero volts to eliminate the possibility of self-heating occurring during stress. The increase in the drain current magnitude following stress is therefore not due to self heating but negative charge accumulation during stress.

Self heating is a product of electron energy transferred to the lattice due to scattering. In general, increasing current increases the energy is transferred to the lattice. To determine whether significant self-heating is occurring in the pMOSFET during stress, the experiment was repeated at 6 K and 100K with the drain bias at zero volts during stress (reducing the drain current to zero to eliminate self-heating during stress) and without interrupting the relaxation test. Results for the 100 K experiment are shown in Fig. 9 (similar results, not shown, were also obtained for the 6 K experiment). With the drain bias set to zero during stress, a significant increase in the drain current magnitude is observed in Fig. 9. This increase *cannot be explained by self-heating* and therefore indicates negative charge accumulation during stress, causing a threshold voltage shift to the right to occur, followed by negative charge removal during relaxation.

Boundary Between Negative and Positive Charge Recovery

The discussion so far has focused on validating the presence of negative charge accumulation during stress and removed during relaxation at cryogenic temperatures in these high-k pMOSFETs. The transition between negative and positive net charge recovery as a function of temperature is examined next. Before doing so, a few interesting observations are made.

First, the stability measurement (Table I, test 2) at cryogenic temperatures (e.g. Fig. 8 and Fig. 9), show the drain current increasing in magnitude as a function of time (this is not observed at room temperature), an indication that negative charge is accumulating in the gate oxide. This charge accumulation is occurring at a gate voltage typically thought to show negligible transients (which it does at room temperature). While this may be the result of relaxation from incomplete relaxation from previous stress tests occurring in the device, it has also been observed on non-stressed devices as well.

A second interesting observation of the cryogenic data is found by examining the drain current during relaxation after being interrupted to perform I_{Drain}-V_{Gate} measurements (e.g., Fig. 3 and Fig. 8 after 10 s and 100 s). The first relaxation measurement point after interruption shows a lower $|I_{Drain}|$ current, indicating that V_{th} shifted to the left due to the I_{Drain}-V_{Gate} measurement which took place during interruption. However, this is followed by an increase in $|I_{Drain}|$ before decreasing again. From this observation two competing mechanisms are easily identified. Further work is necessary to better understand what is occurring.

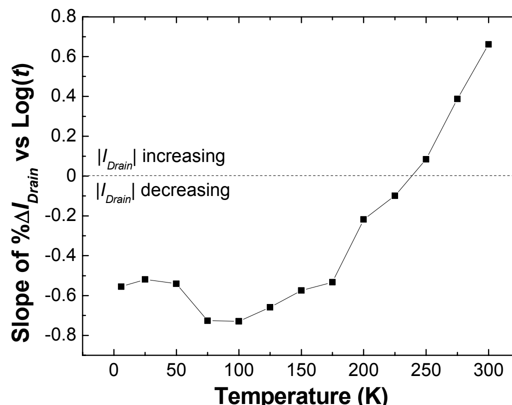

Fig. 10: Plot of the slope of $\%\Delta I_{Drain}$ (normalized to the first recovery point) during the first 10 s of relaxation versus temperature. The drain current increases following stress at temperatures above 240 K.

The stability measurement and recovery trends discussed above suggest that bidirectional charge transfer is taking place in the gate oxide. To analyze the temperature dependence of net negative or positive charge accumulation during stress, we therefore focus on the slope trends of the first 10 s of relaxation data (before interruption). Calculation of the relative change in I_{Drain} during relaxation was made using (1) where t_0 is the first measurement point during relaxation. A least squares linear fit to $\%\Delta I_{Drain}$ (on a log x-scale) is made to extract the slope. A plot of the slope of $\%\Delta I_{Drain}$ versus

temperature is shown in Fig. 10. Fig. 10 suggests the border between negative and positive net charge recovery occurs near 240 K.

$$\%\Delta I_{Drain} = \frac{I_{Drain} - I_{Drain}(t_0)}{I_{Drain}(t_0)}100 \quad (1)$$

CONCLUSIONS

The experimental data we have provided demonstrates temperature dependence for charge mechanisms in NBTI. It is evident that, by reducing the temperature at which threshold voltage and drain current measurements are monitored from room temperature to 6 K, recovery changes from a positive charge dominated scheme (consistent with hole trapping during stress and de-trapping during relaxation) to a negative charge dominated scheme (suggesting electron trapping during stress and de-trapping during relaxation). Special care was taken to promote thermal stability of the device and additional experiments show these trends are not the result of self-heating. The presence of negative charge kinetics, evident at cryogenic temperatures, may have implications for long term reliability and influence models for high-k reliability projections.

ACKNOWLEDGEMTENTS

The authors would like to thank imec’s p-line in Leuven, Belgium for providing the devices. Special thanks to Dr. Amy Moll (BSU) for partial support of this work, and the Nanoscale Materials & Device Group (nano.boisestate.edu). RGS would like to thank the NRC Research Associateship Program.

REFERENCES

[1] S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, A. Jain, and M. A. Alam, "A critical re-evaluation of the usefulness of R-D framework in predicting NBTI stress and recovery," in *IEEE International Reliability Physics Symposium*, 2011, pp. 6A.3.1-6A.3.10.

[2] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *IEEE International Reliability Physics Symposium*, 2009, pp. 33-44.

[3] T. Grasser, H. Reisinger, P. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *IEEE International Reliability Physics Symposium*, 2010, pp. 16-25.

[4] V. Huard, "Two independent components modeling for Negative Bias Temperature Instability," in *IEEE International Reliability Physics Symposium*, 2010, pp. 33-42.

[5] H. Reisinger, T. Grasser, W. Gustin, Schlu, x, and C. nder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress," in *IEEE International Reliability Physics Symposium*, 2010, pp. 7-15.

[6] R. G. Southwick, W. B. Knowlton, B. Kaczer, and T. Grasser, "On the thermal activation of negative bias temperature instability," in *IEEE International Integrated Reliability Workshop Final Report*, 2009, pp. 36-41.

[7] A. Kerber, K. Maitra, A. Majumdar, M. Hargrove, R. J. Carter, and E. A. Cartier, "Characterization of Fast Relaxation During BTI Stress in Conventional and Advanced CMOS Devices With HfO_2/TiN Gate Stacks," *IEEE Transactions on Electron Devices,* vol. 55, pp. 3175-3183, 2008.

[8] B. Kaczer, T. Grasser, P. J. Roussel, J. Martin-Martinez, R. O'Connor, B. J. O'Sullivan, and G. Groeseneken, "Ubiquitous relaxation in BTI stressing - New evaluation and insights," in *IEEE International Reliability Physics Symposium*, 2008, pp. 20-27.

Questions and Answers

Q1: Inelastic vs elastic tunneling, is it even possible to have elastic tunneling?

A1. Elastic tunneling is possible at cyrogenic temperatures. We have seen direct experimental evidence for this at 6K when performing single pulse charge trapping in nMOS high-k which shows a hysteresis in V_{th}.

Q2: If elastic why wouldn't you see abnormal NBTI at room temp?

A2. Abnormal NBTI might not be observed at room temperature due to the strong influence of classical NBTI on device characteristics.

Q3: Why is there a negative slope in the I_{Drain}-V_{Gate} characteristics at 6K, isn't that self heating?

A3: While the negative slope maybe self-heating, we believe the negative slope is due to degradation in the mobility at strong vertical fields. The experiments discussed earlier to address self-heating issues indicates that self heating plays a negligible role at these bias conditions in our devices. We feel this also indicates that the negative slope seen in the I_{Drain}-V_{Gate} characteristics is not due to self-heating. Further experiments are necessary to determine for certain however.

Q4: Could you get self heating during the measurement itself that is not shown by the measurement with 0V on the drain?

A4: Without a current flowing through the channel, self-heating would have to arise from current flowing through the gate. The gate leakage current however is too small for this to be reasonable.

Q5: Could Pb centers be responsible for the abnormal trends you are showing?

A5: We have a poster here that shows differences between SiO_2 and HfO_2 at these temperatures. The data collected so far indicates that abnormal NBTI is significantly higher in high-k (with a SiO_2 interface layer) than pure SiO_2. This would seem to indicate that this abnormal NBTI process does not occur with defects at the SiO_2/Si interface.