# TCAD Simulations of Statistical Process Variations for High-Voltage LDMOS Transistors

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***Abstract*—In this work the development of statistical models for the design of high-voltage devices considering process variations is shown. Critical process variables which are responsible for the electrical parameter shift were chosen from in-line data analysis. Based on their parameter fluctuation ranges statistical full process and device TCAD simulations were performed for high-voltage n- and p-channel LDMOS transistors implemented in 0.35 µm high-voltage CMOS technology. Measurement techniques from device production had been adapted to the device simulations to achieve proper device characterisations. Finally, the resulting parameters had been analytically modelled for comparison with measurements and development of statistical SPICE models. For process and device simulation commercial software as well as academically available software had been used.**

***Index Terms*—LDMOS, Process Variation, TCAD, Statistical Modelling, Monte Carlo**

## I. Introduction

In integrated circuit development the reliability and performance of the advanced devices is a main goal. Process variations directly affect the device characteristics. Fundamentally, the dependencies of process parameters to desired device properties have to be studied [1], [2]. Even produced corner lots also should fulfil desired criteria. In this work, obtained from site measurements, the variations of key parameters and their impact on the output characteristics are analysed by TCAD simulations. To reduce the time consumption arising with simulation of multiple parameter variations a method of central composite face-centred design and a following modelling of the resulting dependencies was selected. An already established high-voltage LDMOS process has been chosen to compare the validity of achieved results. For process simulation the commercial process simulator SPROCESS [3] has been used. To compare the simulation with measurement exactly the same methodology which is used in fabrication for parameter measurement has been adapted to the device simulations. Because of flexibility the device simulator MINIMOS-NT [4] was selected. Based on these results, the influences of parameter fluctuations on the characteristics can be studied and extended to future device developments.

## II. Process Variation Aware TCAD Simulation

The simulation flow can be split into several independent modular parts, which is shown in Figure 1. For each parameter set a process simulation, the device simulations for each output key parameter, and a following extraction of this parameter has to be performed. With this set of values the parameter dependency is analytically modelled and applied to a statistical parameter variation. These results can be compared with measurements and studied for further use.

The input parameters are selected by the engineers as seven key parameters, which have high impact on the manufactured devices (confer Table I).

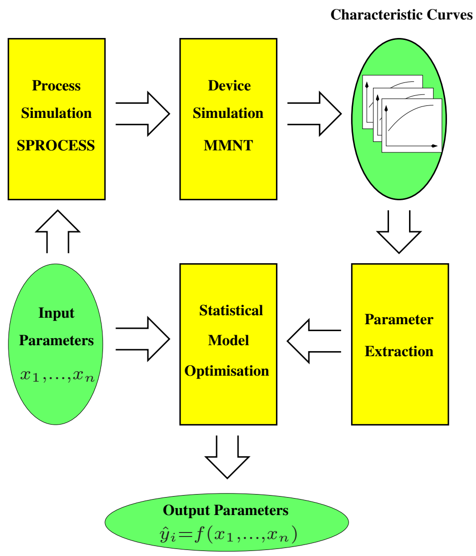


Fig. 1. Simulation flow for the generation of statistical device models.

## III. Simulation Design

Virtual statistics generation does only make sense if its results are more rapidly available than the real measurement

| Parameter | Unit | Min. | Mean | Max. |
|---|---|---|---|---|
| Substrate resistivity | $\Omega$ cm | 18 | 20 | 22 |
| HV-NWell dose | $10^{12}$ cm$^{-2}$ | 4.05 | 4.10 | 4.15 |
| HV-PWell mismatch | nm | -0.1 | 0 | 0.1 |
| Shallow NWell mism. | nm | -0.1 | 0 | 0.1 |
| Screening Oxide mism. | Å | 190 -10 | 190 | 190 +10 |
| Vt implant (BF2) | $10^{12}$ cm$^{-2}$ | 2.65 | 2.70 | 2.75 |
| Oxide thickness variation | Å | 70 -2 | 70 | 70 +2 |

TABLE I
INPUT PARAMETERS FOR PROCESS SIMULATION (P-CHANNEL LDMOS TRANSISTOR). THE MEAN VALUE AND VARIATION RANGES ARE ACHIEVED FROM MEASUREMENTS AND CAN BE INTERPRETED AS THE $\pm 3\sigma$ RANGE OF THE PARAMETERS.

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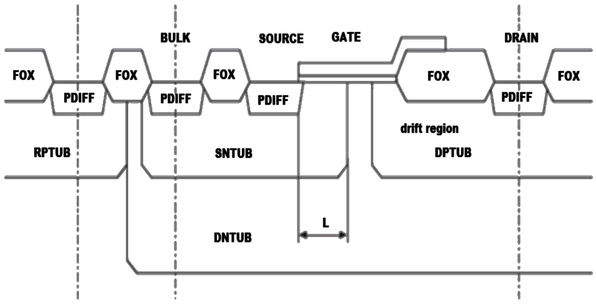


Fig. 2. Schematic lateral view of the simulated p-channel high-voltage LDMOS transistor.

data. Therefore, the process and device simulations were based on a minimum set of required input parameters and geometries together with efficient DOE (design of experiments) to overcome the huge amount of simulation time.

Here, two geometries have been used, a short channel device (gate length 0.6 µm) and a long channel device (10 µm). For the case of p-channel LDMOS transistor (HV-PMOS), a set of 7 critical parameters have been chosen to regard process variations as input parameters $x_i$ to the system. The selected parameters can be seen in Table I. Hereby the used mean value and variation range of the parameters is shown as well. The values are chosen as typical values of the parameters applied from independent measurements. The variation range describes minimum and maximum values of the parameters and can be interpreted as $3\,\sigma$ ranges of the distribution of the process parameters. The lateral cut through the used transistor is depicted in Figure 2.

In the simulations 3 levels of the parameters, which are the mean value, the minimum, and the maximum value have been investigated. To overcome the time consuming method of $3^7 = 2187$ full factorial combinations a Central Composite Face-centred (CCF) design was chosen [5]. For $n$ parameters this method consists of $2^n$ full factorial simulations of the min/max combinations, $2\,n$ axial points of the screening analysis, and one simulation for the center point. In sum this leads to 143 variations in 7 parameters.

The output parameters $y_i$ are chosen as the representatives of the investigated HV-PMOS, which are the threshold voltage (in the linear region) $V_{\mathrm{thlin}}$, the on-resistance $R_{\mathrm{on}}$, the saturation current $I_{\mathrm{Dsat}}$, the conductivity $\gamma$, the leakage current $S_{\mathrm{leak}}$, and the fitting parameter $\eta$ which, together with a second device calculation, yields to the effective gate length $L_{\mathrm{eff}}$. To achieve competitive results the extraction method for these parameters has been overtaken from the commonly used measurement strategy at austriamicrosystems. For example the extraction method for $V_{\mathrm{thlin}}$ can be seen in Figure 3. Source, bulk, and substrate are connected to 0 V, drain to -0.1 V, and the gate is swept starting from 0 V. In the $I_{\mathrm{DS}}$ curve the maximum slope is detected. An extension of the linear approximation at this bias point delivers the threshold voltage $V_{\mathrm{thlin}}$ of this device.

The 143 process simulations have been set up in Sentaurus Workbench (SWB) of the TCAD simulation package of SYNOPSYS [3]. Here the parameter variations can be set up automatically by overlay variables in the specified process flows of the device. The different simulations had been spawned on the TCAD cluster at the Institute for Microelectronic (IuE) using the interface of SWB for Sun Grid Engine.

The device simulations were performed in MINIMOS-NT [4]. For each parameter extraction either gate voltage sweeps with fixed drain voltage or with $V_{\mathrm{DS}} = V_{\mathrm{GS}}$ have to be performed. For performing the device simulations and extraction of the parameters a Python interface has been developed, which also spawns the jobs by Sun Grid Engine.

The process and device simulations were computed on the TCAD cluster at IuE, which consists of 250 AMD Opteron Cores operating at 2.7 GHz. For comparison one simulation of the full process flow took around 4 days. All required device simulations for parameter extraction took around 1 day, performing on all available cores.

## IV. Comparison

After extraction of the parameters a direct influence of the varied input parameters on the output can be studied. Comparing the output parameters and their dependency on input variables can give hints of possible limits in the structures. For comparison with measurement the view will be different. By measurement only output variables can be observed and the originated input parameters are not viewable. A discussion can only be done by comparison of different output characteristics.

The resulting dependency of $V_{\mathrm{thlin}}$ versus $R_{\mathrm{on}}$ for the device simulations can be seen in Figure 4. The input parameters were selected by CCF design in the ranges depicted in Table I. For comparison, measured devices from production show a distribution which can be seen in Figure 5. Unfortunately, during the face centred simulation the output values will not show the expected distribution. Because of the minimum number of input parameter permutations only three discrete variations of the input values are performed (see Figure 6). These variations result in unrealistic large variation ranges, standard deviations or multiple distributions of the output parameters. However, the inputs show a natural distribution and as a consequence the output shows the result of these

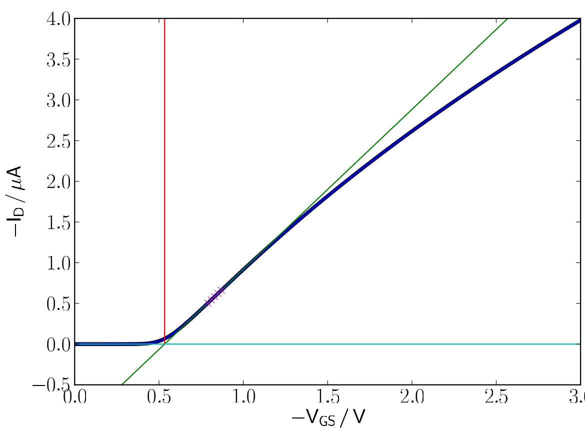


Fig. 3. Extraction methodology for $V_{\mathrm{thlin}}$. Source and bulk are connected to 0 V, drain to -0.1 V, and $V_{\mathrm{GS}}$ is varied. An expansion of the maximum slope to $I_{\mathrm{D}} = 0$ delivers the threshold voltage $V_{\mathrm{thlin}}$.

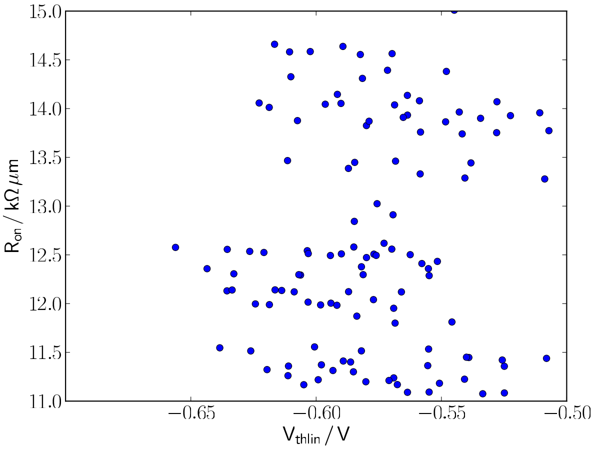


Fig. 4. Dependency of $R_{\mathrm{on}}$ versus $V_{\mathrm{thlin}}$ for the simulated devices.

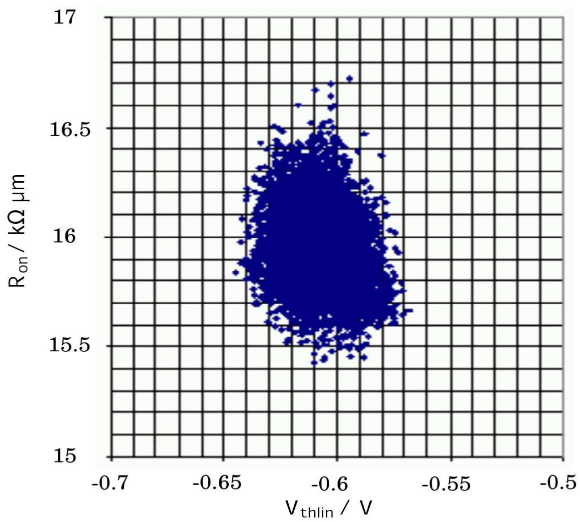


Fig. 5. Measured view of $R_{\mathrm{on}}$ versus $V_{\mathrm{thlin}}$ for produced transistors.

distributions. Therefore, the methodology of comparison is chosen in a different way:

The simulated output is chosen as a mathematical approximation of the input variables. With the CCF design each electrical output parameter $\hat{y}$ is modelled as a quadratic function

$$\hat{y} = \mathbf{x}^{\mathrm{T}}\mathbf{A}\mathbf{x} + \mathbf{b}^{\mathrm{T}}\mathbf{x} + c \tag{1}$$

of the based input parameters $\mathbf{x}$ by a least square fit of $\mathbf{A}$, $\mathbf{b}$, and $c$ for all design points $i$

$$\sum_i ||y_i - \mathbf{x}_i^{\mathrm{T}}\mathbf{A}\mathbf{x}_i + \mathbf{b}^{\mathrm{T}}\mathbf{x}_i + c|| \rightarrow \min \tag{2}$$

of their simulated output parameters $y_i$.

Afterwards the input variables are chosen normally distributed according to the measurements of characteristic values of the input (confer Figure 7) and are applied to the mathematical approximation. This leads to an output, in dependence of the natural distribution of input variables.

After this methodology the output variables show the correct distribution, compared to measurements, which is shown in

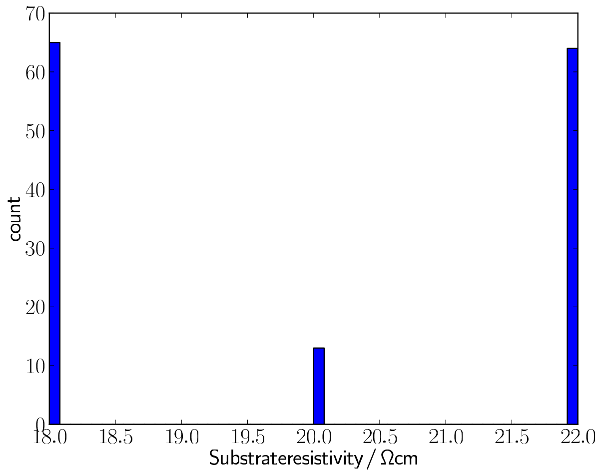


Fig. 6. Originated input parameter distribution used in the CCF design for process simulation. The CCF methodology results in $2^{n-1}+1$ simulations for the minimum and maximum values each and $2\,n-1$ simulations for the center value.

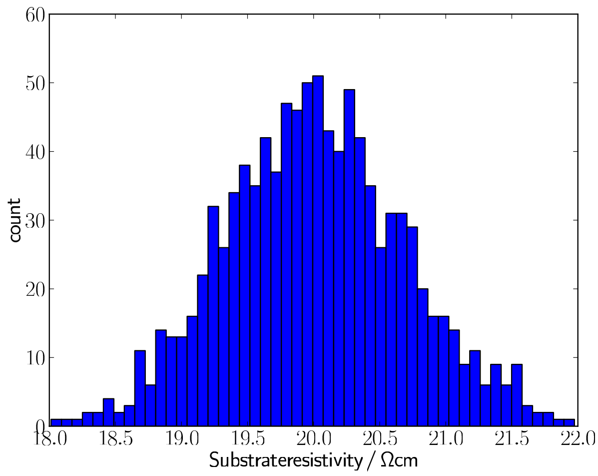


Fig. 7. Randomly normally distributed input variation. The mean value and standard deviation is achieved from measurements.

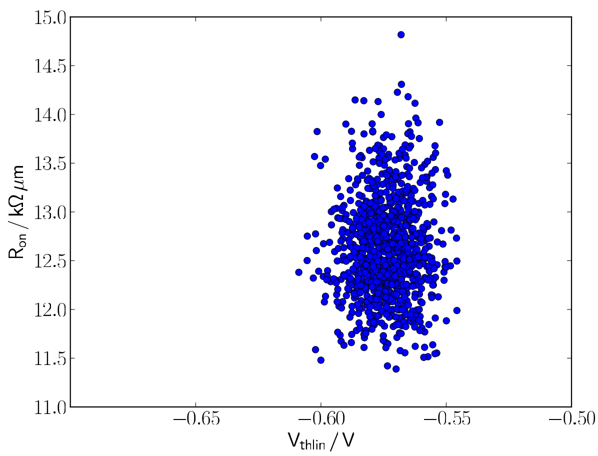


Fig. 8. Dependency of the modelled parameters $R_{\mathrm{on}}$ versus $V_{\mathrm{thlin}}$ after applying normally distributed input parameters.

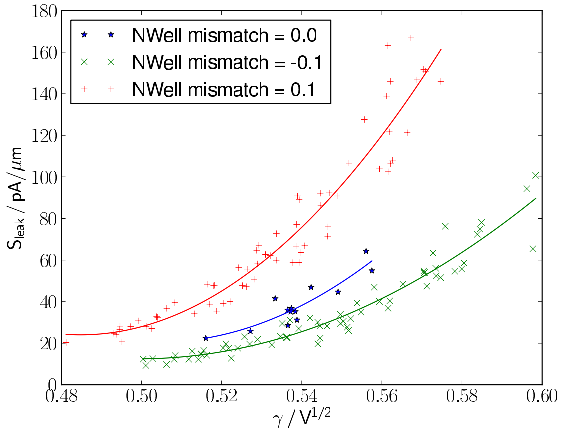


Fig. 9. Dependency of $\gamma$ versus $S_{\text{leak}}$ for the simulated devices. Different symbols show the parameter sets for the shallow NWell mismatch. Here a major dependency of the output parameters on the shallow NWell mismatch can be determined.

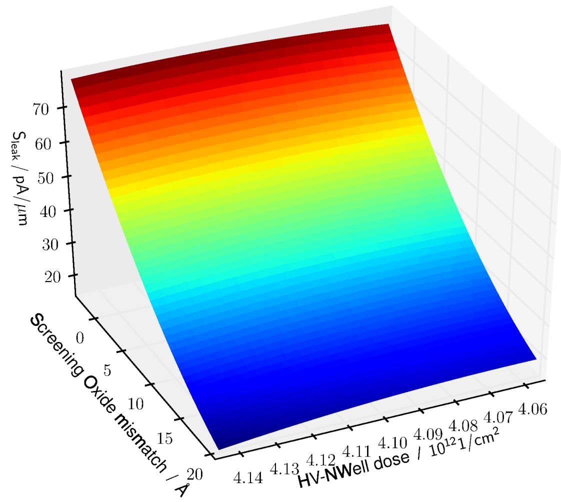


Fig. 10. Evaluation of the relatively high impact of the screening oxide mismatch and low impact of the HV-NWell dose on the leakage current $S_{\text{leak}}$.

Figure 8. Now an analysis of output parameters can be performed.

This optimization and extraction was implemented in Python using the scientific modules SciPy and NumPy. These modules expand Python by a functionality and even syntax similar to Matlab.

## V. Discussion

After finished parameter extraction and final model evaluation different sets of inputs and their influence on the outputs can be analysed. The application on the model (1) computes really fast and a variety of comparison of different sketches of outputs with their input parameters can be performed. Moreover, at different stages in simulation different statements can be observed.

A view of the dependency of $\gamma$ versus $S_{\text{leak}}$ after the CCF simulations can be seen in Figure 9. Here clearly three generations of point sets can be observed. A comparison of different parameter sets applied to the analytical model detects the shallow NWell mismatch as the parameter for the three generations in this figure. The colouring of the simulation points is in dependence of the used shallow NWell mismatch. Continuative analysis detects the Screening Oxide mismatch as the major influencing parameter, whereas other parameters show nearly no influence on these output variables. Applying the mathematical model (1) to $S_{\text{leak}}$ with only varying Screening Oxide mismatch and HV NWell dose is depicted in Figure 10.

A sketch of the dependencies of input to output variables can be seen in Table II. Each input variable $x_i$ is varied in a $1\,\sigma_i$ range and the achieved output variation in percent relatively to the nominal value is calculated. The largest variations for each output parameter are emphasized.

| variation range | $R_{\text{on}}$ | $V_{\text{thlin}}$ | $S_{\text{leak}}$ | $\gamma$ | $\eta$ |
|---|---|---|---|---|---|
| Substrate resistivity | 0.120 | 0.188 | 1.354 | 0.022 | 0.021 |
| HV-NWell dose | 0.459 | 0.004 | 0.839 | 0.027 | 0.261 |
| HV-PWell mism. | **3.582** | 0.479 | 1.413 | 0.100 | **3.092** |
| Shallow NWell mism. | 1.462 | 0.607 | 16.43 | 0.427 | 2.774 |
| Screening Oxide mism. | 0.129 | **1.365** | **21.64** | **1.312** | 0.379 |
| Vt implant (BF2) | 0.019 | 0.831 | 13.01 | 0.723 | 0.305 |
| Oxide thickness var. | 0.203 | 0.499 | 6.721 | 0.268 | 0.220 |
| Nominal value | 12.55 $\text{k}\Omega\mu\text{m}$ | 0.573 V | 37.14 $\text{pA}/\mu\text{m}$ | 0.539 $\text{V}^{1/2}$ | $8.5\cdot10^{-5}$ $\text{A}/\text{V}^2$ |

TABLE II

Variation ranges of the output parameters in % of their nominal value in dependence of a $1\,\sigma$ input variation. The last line shows the nominal values of the output parameters.

## VI. Conclusion

In this paper we present statistical models based on process variation-aware TCAD simulations. The process variation of n- and p-channel LDMOS transistors has been investigated by means of simulations. Process and device simulations were performed by the SYNOPSYS tools and MINIMOS-NT, respectively. With the use of analytic modelling and a suitable CCF design the number of simulation experiments could be minimized. Achieved results can for instance be applied to SPICE models for further device and circuit analysis.

## Acknowledgement

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