# The Relevance of Deeply-Scaled FET Threshold Voltage Shifts for Operation Lifetimes

B. Kaczer[1,*], J. Franco[1,2], M. Toledano-Luque[1], Ph. J. Roussel[1], M. F. Bukhori[3], A. Asenov[4,5], B. Schwarz[6], M. Bina[6], T. Grasser[6], G. Groeseneken[1,2]

[1]imec, Kapeldreef 75, B-3001 Leuven, Belgium
[2]KU Leuven, Belgium
[3]UKM, Malaysia
[4]University of Glasgow, UK
[5]Gold Standard Simulations, UK
[6]TU Wien, Austria
[*]phone: +32 16-281-557, e-mail: kaczer@imec.be

***Abstract*— In nm-sized FET devices with just a few gate oxide defects, the typically measured threshold voltage shifts are not obviously correlated with the device behavior at high gate bias. The largest shifts observed at the threshold voltage after the capture of a single carrier are reduced at higher gate biases. This degradation-mitigating effect is further shown to be amplified at lower channel doping. The understanding gained from 3D numerical simulations is captured in a simple analytic description of a single trapped-charge impact on the FET characteristics in the entire gate bias range. Potential use is illustrated in an improved lifetime projection and in circuit simulations of time-dependent variability.**

***Time-dependent variability, single-carrier effects, circuit simulations, lifetime projections***

## I. INTRODUCTION

The reduction of FET device dimensions to nanometer scales implies that literally only a handful of defects are present in each device, while each defect has a substantial impact on the device operation. The resulting significant increase in both *time-zero and time-dependent variability of many degradation mechanisms is thus best understood in terms of the impact of individual (charged) defects.* This "bottom-up" approach to device reliability is already being advocated by several groups [1-6].

Historically the common wisdom has been to measure and describe the degradation, such as Bias Temperature Instability (BTI) or Random Telegraph Noise (RTN), in terms of the threshold voltage $V_{th}$ shift [7, 8]. Here we show that in nm-sized devices, with just a few gate oxide defects, the *typically measured $V_{th0}$ shift is not obviously correlated with device behavior at high gate bias* $|V_G|$. The latter is representative of the impact on the drain current during typical device operation. We further show that the huge, "killer" $V_{th}$ shifts at the tail of the $\Delta V_{th}$ *exponential* distribution observed around $V_{th0}$ [9] are reduced at higher $|V_G|$'s. An example of the resulting more benign distribution of degradation impacting device operation lifetime is demonstrated. This mitigating effect is further shown to be amplified at lower channel doping. The presented learning from measurements and full scale 3D 'atomistic' simulations is captured in a simple, compact-model pluggable, analytic description of a single trapped-charge impact on the FET characteristics in the entire $V_G$ range. Such description is essential for e.g. SRAM cell stability simulations [10].

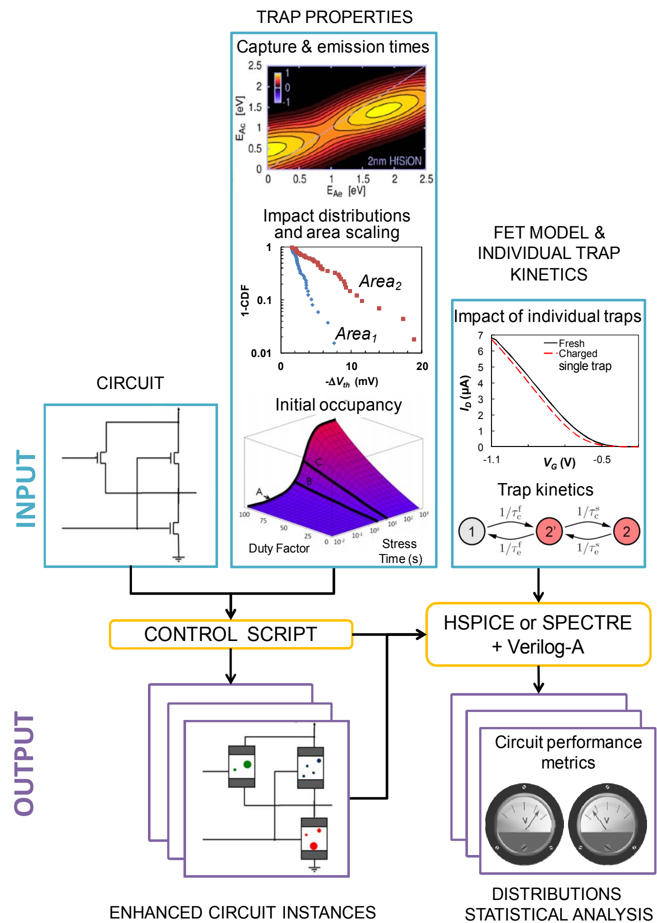


Figure 1. Simulation setup for studying time-dependent variability of circuits based on industry-standard tools [3].

## II. BACKGROUND

Our "atomistic" simulation framework proposed previously [3] is shown in Fig. 1. It allows simulating the impact of *workload*-dependent variability on circuits (i.e., "reliability *distributions* under operating conditions"). The framework accepts the studied circuit in the form of a standard netlist. All or selected FET devices of the input circuit are annotated (i.e., "instantiated" or "enhanced") with unique defect properties randomly selected from distributions obtained previously on the simulated technology. These distributions include the (voltage and temperature dependent) capture and emission times [11] and the impact of individual defects on the FET properties (e.g., the threshold voltage $V_{th}$ shift) [3, 12]. The latter, as well as the number of defects in each simulated FET device is adjusted to the device gate area. The occupancy of each defect is also determined based on its averaged workload prior to simulated interval in the circuit lifetime [3, 13].

Based on this information the control script generates multiple random instances of enhanced circuits and submits them to the HSPICE or SPECTRE solvers. The other crucial component of the framework is the Verilog-A-based BSIM4 FET model augmented to simulate the impact of individual defects on the FET's behavior. It is also capable of following the occupancy of each defect ("defect kinetics") depending on the applied voltages, thus naturally incorporating workload dependence [2,3]. The resulting circuit parameters from all instances are output and subsequently statistically analyzed.

The correctness of the used methodology is ensured by basing it on our previously-acquired detailed understanding of microscopic ("atomistic") physical mechanisms [2,11]. At the same time, by using observable defect properties it remains sufficiently agnostic to allow the simulation of a wide variety of degradation effects. The inclusion of Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI) has been already demonstrated [3,14]. Other mechanisms, such as Hot Carrier Injection (HCI) can be added by incorporating pertinent defect generation rates, kinetics, and impact on FET parameters. The framework can be similarly expanded to gate terminal-related mechanisms, such as gate current RTN [15], Stress Induced Leakage Current (SILC) and Time-Dependent Dielectric Breakdown (TDDB). The natural inclusion of workload dependence then allows simulating not only long-time aging, but also short-term, cycle-to-cycle variations in circuit parameters (at an arbitrary age point of the circuit) such as delay jitter [14, 16].

The impact of an elementary trapped charge on FET characteristics is in the current version of the framework limited to shifting the threshold voltage. The purpose of this work is then to improve our understanding of this impact.

## III. EXPERIMENTAL

This work builds on the experimentally very demanding measurements of $I_D$-$V_G$ curves of very small ($L \times W$ = 35×90 nm$^2$, EOT ≈ 1.8nm) pFETs *before and after a capture of a single hole* in the gate oxide. The details are described in [12]. A typical example is shown in Fig. 2. The impact on the original ("before" or "fresh") $I_D$-$V_G$ can be reduced to $V_G$-dependent $\Delta V_{th}(V_G)$ (note the definition in Fig. 2a). The data are plotted hereafter versus the standard initial threshold voltage $V_{th0}$ *before capture* of each FET. Although this work is, for the sake of brevity, limited to low drain voltage $V_D$, our simulations show the presented analysis is valid at and can be extended to the entire $V_D$ range.

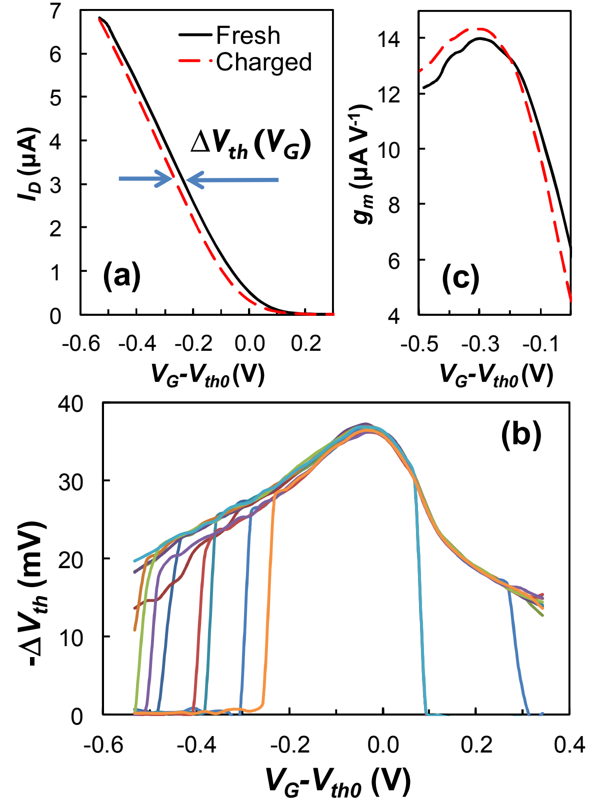


Figure 2. (a) $I_D$-$V_G$ curves measured at $V_D$ = -0.1 V on a $L \times W$ = 35×90 nm$^2$ pFET *with a single oxide defect uncharged and charged* [12]. (b) The corresponding $\Delta V_{th}(V_G)$ is defined as a simple "geometrical" horizontal distance of the two curves at a given $V_G$ (multiple measurements). (c) For the large $\Delta V_{th}$ in (a) and (b) the apparent transconducance $g_m$ *increases* after a single hole trapping.

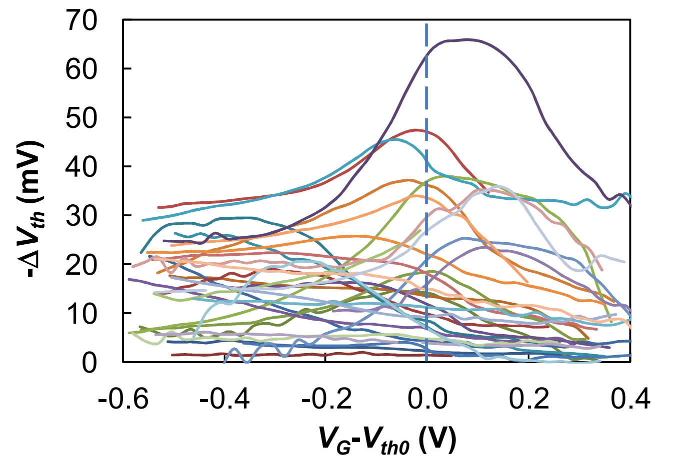


Figure 3. Widely different $\Delta V_{th}(V_G)$ characteristics are found on 30 nominally identical devices before and after the capture of a single hole. The devices were chosen for the significant impact of a single charged gate oxide defect.

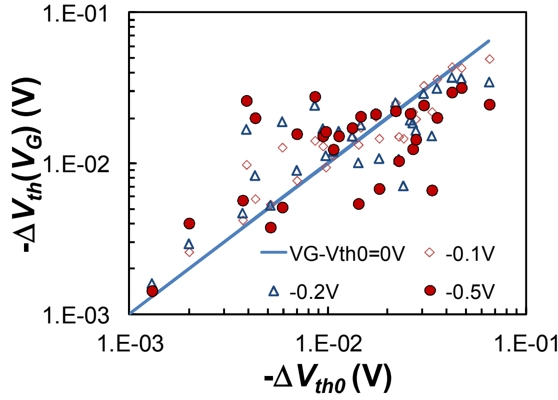


Figure 4. The loss of correlation between shift in the typically measured (low $|V_G|$) $V_{th0}$ ($\equiv\Delta V_{th0}$) and $\Delta V_{th}$ at higher $|V_G|$ [$\equiv\Delta V_{th}(V_G)$], already apparent in Fig. 3, is further documented.

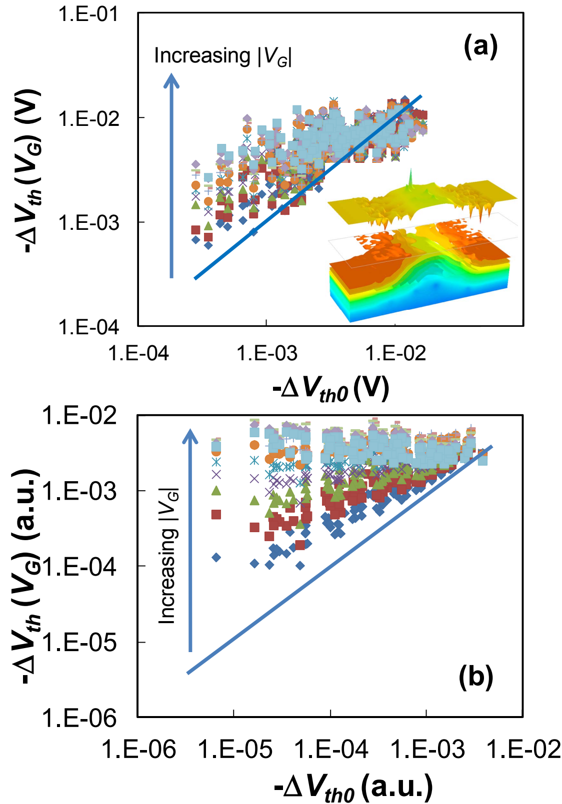


Figure 5. The loss of correlation between $\Delta V_{th0}$ and $\Delta V_{th}(V_G)$ at high $|V_G|$ is corroborated by an atomistic 3D device simulation (illustrated in the inset). (b) The same qualitative trend is obtained from channel-percolation simulation, performed in SPICE by varying $V_{th}$'s of the "atomistic" FET's, emulating random dopant distribution (see Fig. 6a).

## IV. Results and Discussion

Fig. 3 shows the $\Delta V_{th}(V_G)$ characteristics due to the capture of a single hole measured on 30 different devices. It is clear that $\Delta V_{th}(V_G)$ is not constant but changes with $V_G$ in an apparently random manner. The loss of correlation between the typically extracted $\Delta V_{th0}$ (i.e., the $\Delta V_{th}(V_G)$ extracted at $V_{th0}$, demarcated by the dashed line in Fig. 3) and the $\Delta V_{th}$ at higher $|V_G|$ is further documented in Fig. 4. This implies that in nm-sized FETs *the impact on drain current at high* $|V_G|$ *cannot be simply extrapolated from* $\Delta V_{th0}$*, the shift in the commonly understood FET parameter*. The same loss of correlation is observable in the 3D device simulation with the 'atomistic' device simulator GARAND (Fig. 5a) [17] and appears to be a fundamental property of the channel current percolation *electrostatics* (i.e., not transport mechanisms), since the same qualitative trend (Fig. 5b) can be observed with the simplified channel-percolation model (Fig. 6a) [9].

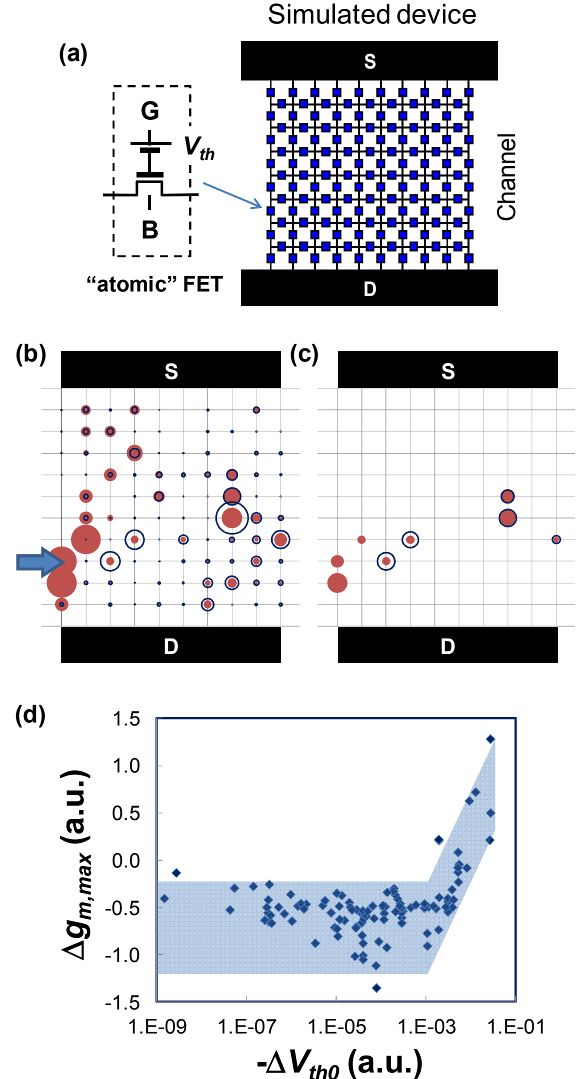


Figure 6. (a) Schematic illustration of the simplified channel-percolation simulation, performed in SPICE by varying $V_{th}$'s of the "atomistic" FET's, emulating random dopant distribution in the simulated device [9]. (b) A 10×10 mesh channel-percolation simulation shows that the largest $\Delta V_{th0}$ shifts due to a single charge defect placed successively in all mesh points (solid bubbles) are generally associated with (c) apparent increases in $g_{m,max}$ (only $g_{m,max} > 0$ shown). (d) $\Delta g_{m,max}$ plotted vs. $\Delta V_{th0}$ reveals that the largest $\Delta V_{th0}$ shifts are generally associated with apparent transconductance $g_m$ increases. Atomistic device simulation yields the same trend (not shown). Redistribution of (b) the channel potential (~$\Delta V_{th0}$) and (c) $g_{m,max}$ (open bubbles) after a single charge trapped at a critical spot (arrow). The next trapped charge is affected by the resulting potential—the impact of multiple trapped charges is, to the first order, simply cumulative.

The simplified model moreover reveals that *the largest $\Delta V_{th0}$ shifts are generally associated with apparent transconductance $g_m$ increases*, as discussed in Fig. 6d. An experimental observation of this effect is documented in Fig. 2c. Such behavior effectively means that *the largest $V_{th}$ shifts at the tail of the single-trapped-charge $\Delta V_{th}$ exponential distribution observed around $V_{th0}$ are reduced at higher $|V_G$'s$|$* where the FETs are typically operated. The resulting $\Delta V_{th}$ distributions are consequently narrower, as documented by measurements (Fig. 7a), the atomistic device simulation (Figs. 7b), and also qualitatively by the simplified model (Fig. 7c). To allow further analytical treatment and a lifetime extrapolation discussed below in Fig. 11, the behavior is approximately described by a Weibull distribution with a $V_G$-dependent shape factor (not shown).

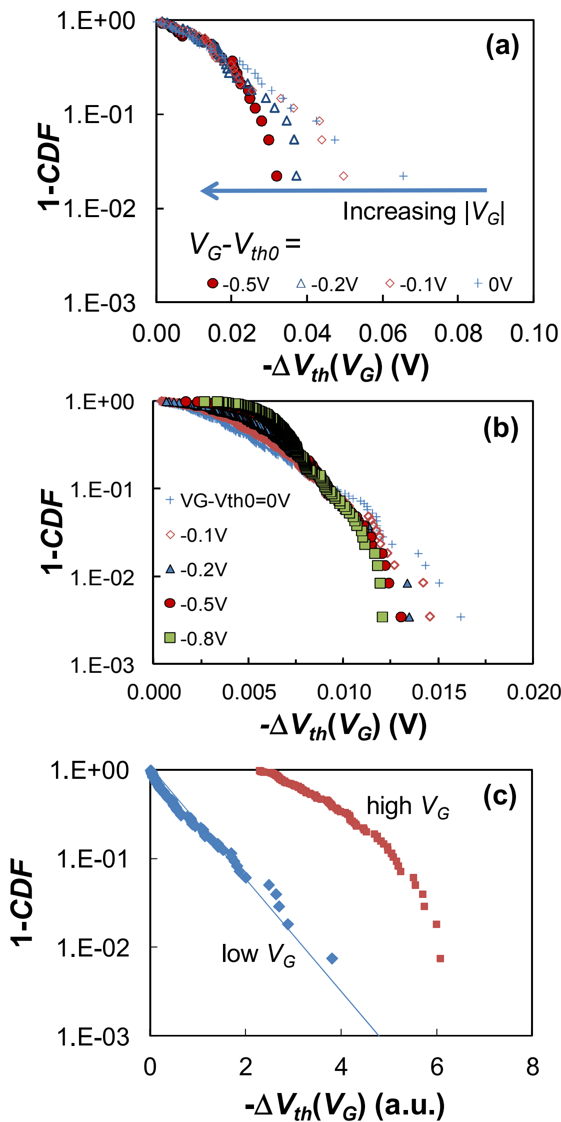


Figure 7. (a) The reduction of the measured $\Delta V_{th}(V_G)$ distribution width (variance) at higher $|V_G|$ is readily reproduced by the atomistic device simulation (b). (c) The same *qualitative* effect on the distribution shape is reproduced by the simplified channel-percolation simulation (Fig. 6a).

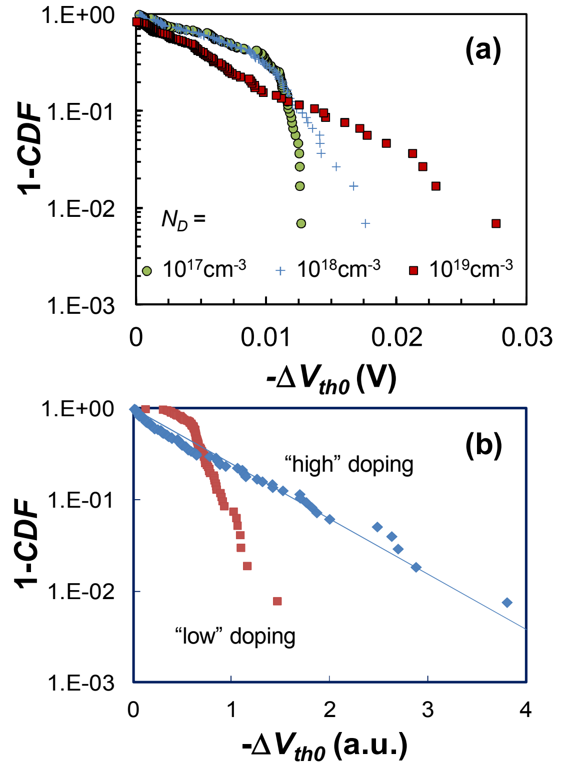


Figure 8. (a) Atomistic device simulations show single-trapped-charge $\Delta V_{th0}$ variation decreases with decreasing substrate doping. (b) The same trend is qualitatively reproduced with channel-percolation simulation (Fig. 6a), assuming only a fraction of the atomistic FETs' $V_{th}$'s are modified (corresponding to fewer dopants).

Apart from $V_G$, the width of the distribution is also affected by substrate doping [18], as documented by simulations in Figs. 8a and 8b. This behavior further emphasizes the industry's need to move to lightly doped channels. We also note that the substrate doping and the $V_G$ dependences could be the source of disagreement about the exact shape of the $\Delta V_{th}$ distribution (e.g., exponential vs. lognormal, etc.) in the RTN and BTI literature [8,9,19].

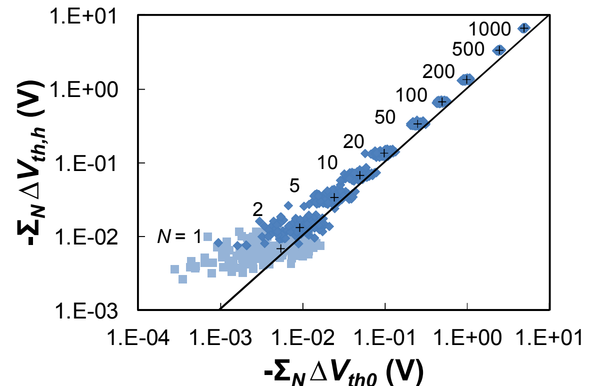


Figure 9. Illustration of constructing $\Delta V_{th0}$ and $\Delta V_{th,h}$ (i.e., at high $|V_G|$) distributions in larger devices. The *relative* variability is decreasing with increasing device area proportional to the number of defects $N$. Data for $N$=1 are taken from Fig. 5a (highest $|\Delta V_{th}(V_G)|$, boxes). Distributions for higher $N$ values (diamonds) are constructed by summing randomly-picked values from the $N$=1 distribution. $\Delta V_{th}$ values are not normalized by $N$ for better visibility. Note $\langle\Delta V_{th,h}\rangle > \langle\Delta V_{th0}\rangle$ (crosses), corresponding to mobility degradation.

Fig. 9 illustrates how the single-charged-trap $\Delta V_{th}$ distributions will scale for larger devices with a higher number of active defects. As expected, the relative variability in large devices will decrease, corresponding to all large devices behaving identically under stress. The correlation between $\Delta V_{th}$ an $\Delta V_{th}(V_G)$ at higher $|V_G|$—the assumption of the "classical" reliability projections—is thus reestablished [20]. Fig. 9 also shows that $\langle \Delta V_{th,h} \rangle > \langle \Delta V_{th0} \rangle$, corresponding to the widely-reported mobility degradation [21].

Based on the atomistic device simulations it has been proposed that the shape of $\Delta V_{th}(V_G)$ is controlled by the distance $r$ of the trapped charge from the critical (i.e., the "narrowest") point in the channel current percolation path (Fig. 10a) [12]. This shape can be parameterized with a simple formula

$$\Delta V_{th}(V_G) = \frac{\Delta V_{th,h} v^2 + \Delta V_{th0}}{v^2 + 1}, \qquad (1)$$

where

$$v \equiv \frac{|V_G - V_{th0}|}{V_0}. \qquad (2)$$

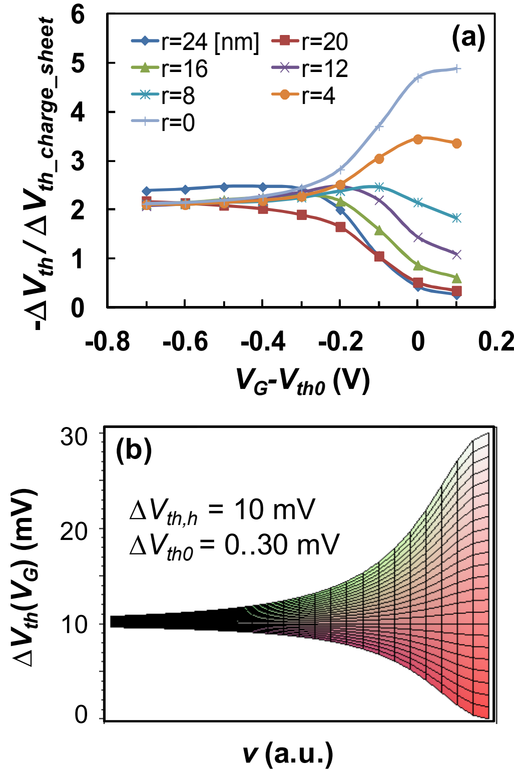


Figure 10. (a) From atomistic 3D device simulations, different $\Delta V_{th}(V_G)$ characteristics are expected as a function of $r$: the maximum $\Delta V_{th0}$ (i.e., at $V_G \approx V_{th0}$) is observed for a charged trap located directly above the critical spot ($r = 0$ nm), while a small but increasing $\Delta V_{th}$ with increasing $|V_G|$ is expected for a trap located further away. (b) The impact of a single trapped charge in (a) can parametrized for use in a degradation-enabled compact model. Note that only $\Delta V_{th0}$ is distributed here. Assuming both $\Delta V_{th0}$ and $\Delta V_{th,h}$ Weibull-distributed will result in a plot akin to Fig. 3.

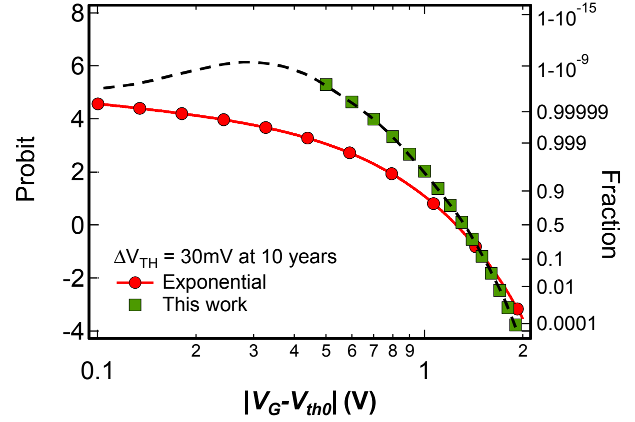


Figure 11. Predicted 10-year lifetime cumulative distribution of pFET *total* $\Delta V_{th}(V_G)$ at $t_{relax} \sim 1$ ms assuming $V_G$-independent *exponential* distribution of single-trapped-charge $\Delta V_{th}$ (circles, presented in [20]) and the $\Delta V_{th}(V_G)$ distribution in Fig. 7a (squares). An improvement is observed at intermediate $V_G$'s due to the reduced variance of the single-trapped-charge distribution.

Here, $V_0$ is a scaling parameter and $\Delta V_{th0}$ and $\Delta V_{th,h}$ are $\Delta V_{th}$ *distributions* at $V_{th0}$ and high $|V_G|$, respectively. Eq. 1, illustrated in Fig. 10b, thus provides physically-based connection between the $\Delta V_{th}(V_G)$ distributions at $V_{th0}$ and high $|V_{G,h}|$ shown in Fig. 7. To the first order (no cross-talk between individual traps), this formula can be invoked repeatedly to calculate the characteristics of individual FETs with multiple defects becoming charged during the circuit simulation (cf. open bubbles, Figs. 6b and 6c).

Finally, the learning presented heretofore is demonstrated on the relaxation of the projected lifetime distribution. Fig. 11 shows the projected device reliability using previously assumed $V_G$-independent (i.e., correlated), exponentially distributed $V_{th}$ shift [20]. A significant improvement in the projected reliability is obtained at medium $V_G$'s when the narrower $\Delta V_{th}$ distributions at higher $|V_G|$ are considered.

## V. CONCLUSIONS

Degradation in nm-sized FETs is understood in terms of impact of individual traps. In such devices with only a handful of defects the typically measured $V_{th}$ shift has no correlation with device behavior at high gate bias. A simple analytic description is proposed to describe the single-trapped-charge impact. The formula is directly pluggable into circuit simulators, such as described here, enabling simulations of time-dependent variability. Large $V_{th}$ shifts at the tail of the typically measured $\Delta V_{th}$ distribution observed around $V_{th0}$ are reduced at higher $|V_G|$'s. This effectively relaxes the impact on the projected device reliability.

## VI. ACKNOWLEDGEMENTS

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