New Trends in Microelectronics: Towards an Ultimate Memory Concept

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Memory is an indispensible component of any modern integrated circuit. While MOSFET scaling has advanced tremendously, traditional DRAM cell scaling is hampered by the presence of a capacitor which is difficult to reduce in size. Recently, an interesting concept of a DRAM memory cell based on a transistor alone was introduced. The ultimate advantage of this new concept is that it does not require a capacitor, and, in contrast to traditional 1T/1C DRAM cells, it represents a 1T/0C cell named Z(for zero)-RAM. The advanced Z-RAM bitcells built on a multiple-gate MOSFET (MuGFET) utilizes the bipolar transistor usually considered as parasitic [1]. The advantage is that the current flows through the body of the structure. The majority carriers are generated by impact ionization and stored under the gates. The charge stored opens the bipolar transistor guaranteeing high current (state 1). The stored charge can be flashed out by applying the voltage pulse to the gates returning the bipolar transistor into the low current state 0. The stored charge for the bipolar transistor in the high current and low current states is shown in Fig.1. The results [2] of current calculations as function of the gate voltage for a double-gate structure with 10nm thin body are shown in Fig.2. In a forward scan direction of the gate voltage, the current stays low until a certain critical value is reached. After that the source-drain current rapidly increases by several orders of magnitude. In a reverse gate voltage scan, the current first slowly decreases, however, due to the charge stored under the gates, the relatively large current value is maintained down to the negative gate voltages, where it abruptly decreases by several orders of magnitude completing the hysteresis loop [2]. The use of vertical gate-all around transistors extends the Z-RAM roadmap to future generations. One disadvantage of the Z-RAM cell is the relatively high operating voltage needed to ignite impact ionization. To reduce the operating voltage, a new concept of a 1T/0C cell was recently proposed [3].

Charge-based memories including flash are, however, gradually approaching the physical limits of scalability, and the search for a new universal memory concept has accelerated. A new type of universal memory has to be nonvolatile and must exhibit low operating voltage, low power consumption, high operation speed, long retention time, high endurance, simple structure, and small size.

One of the promising candidates for future universal memory is the resistive random access memory (RRAM). It is based on new materials, such as metal oxides and perovskite oxides. This type of memory is characterized by high density, excellent scalability, low operating voltages (<2V), fast switching times (<10ns), and long retention time. We developed a stochastic model of the bipolar resistive switching mechanism based on electron hopping between the oxygen vacancies along the conductive filament (CF) in an oxide layer. The CF is formed by localized oxygen vacancies (V_o) [4] or domains of V_o (Fig. 3). Formation and rupture of a CF is due to a redox reaction in the oxide layer under a voltage bias. The hysteresis cycles modeled [5] is shown in Fig.4.

The spin transfer torque random access memory (STTRAM) is another promising candidate for future universal memory. The reduction of the current density required for switching and the increase of the switching speed are among the most important challenges in this area. A decrease in the critical current density for the penta-layer magnetic tunnel junction was reported in [6]. By numerically investigating the dynamics of the switching process illustrated in Fig.5 in a junction composed of five layers we demonstrate [7] that the switching time can be significantly decreased (Fig.6) by the removal of the switching bottleneck due to the central region of the free layer and by tilting the magnetization of the end domains in the magnetostatic field of the uncompensated pinned layers.

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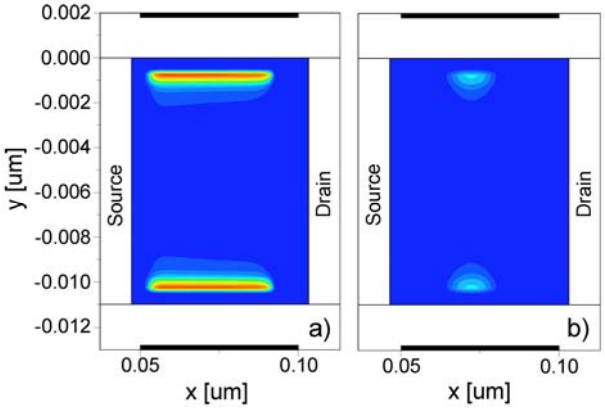

Fig. 1. Simulated hole concentration along the fin in states "1" (a) and "0" (b) for a 50-nm Z-RAM device.

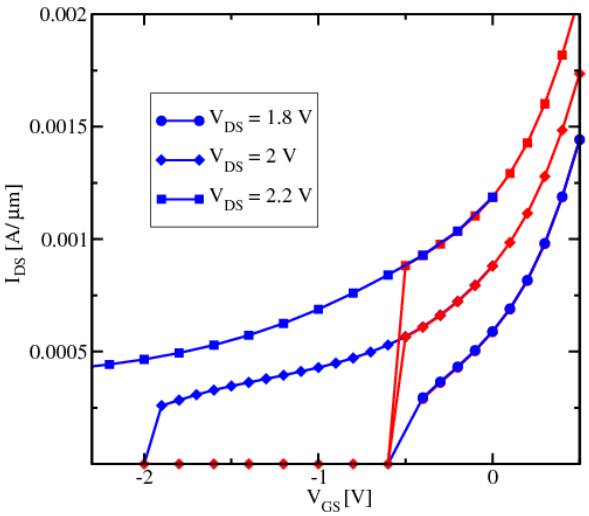

Fig. 2. Simulated hysteresis for a 50-nm Z-RAM device.

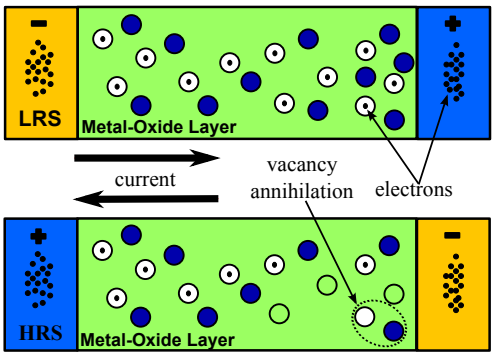

Fig. 3. Schematic illustration of the conducting filament in the low resistance state (top) and the high resistance state (bottom).

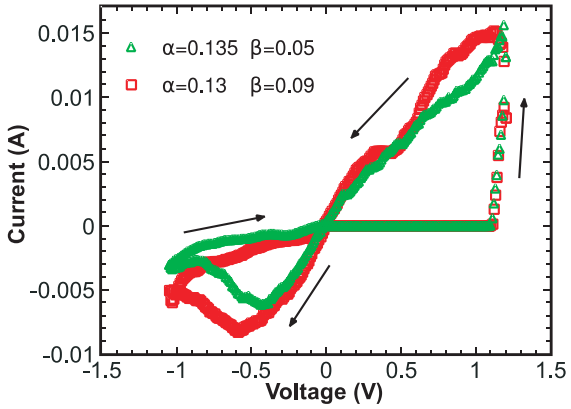

Fig. 4. *I-V* characteristics showing the hysteresis cycle obtained from the stochastic model, for two sets of parameters.

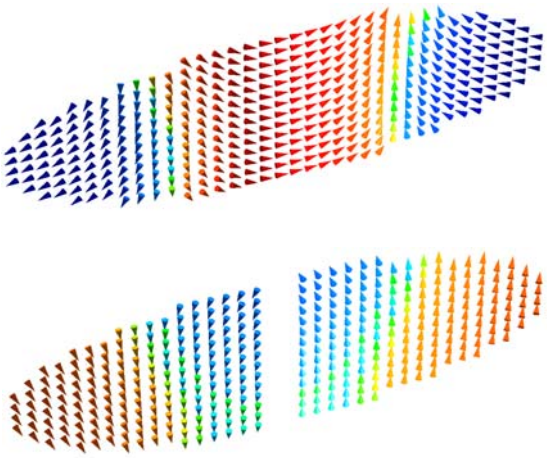

Fig. 5. Snapshots of the switching process for the monolithic (top) and composite (bottom) free magnetic layer.

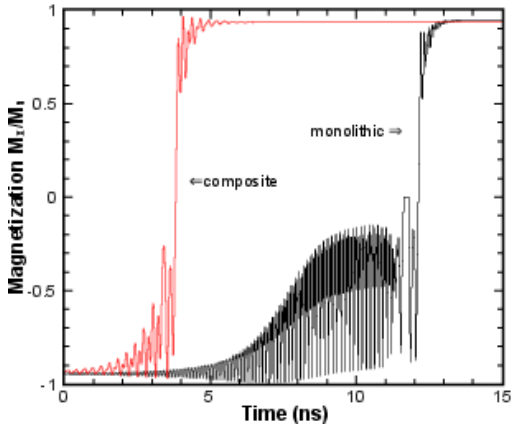

Fig. 6. Magnetization evolution in the free magnetic layer. Faster switching is predicted for the composite layer.