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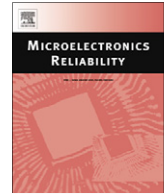

Impact of gate poly doping and oxide thickness on the N- and PBTI in MOSFETs

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ABSTRACT

We study n- and pMOS devices with 3.2–30 nm thick SiON or SiO_2 gate dielectrics and n^{++} or p^{++} doped polysilicon gates to identify the type and energetic location of defects created through bias temperature stress. The results clearly indicate a dependence of the type of BTS induced defects on the stress polarity and the gate poly doping. If holes are provided from the p^{++} poly gate and the gate dielectric is sufficiently thin, NBTI-type donor-like defects may occur even under positive bias stress conditions. For devices with sufficiently thick dielectrics or n^{++} poly gated devices, holes are absent during PBTI stress and acceptor-like defects are created.

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1. Introduction

When subjecting p- and n-channel MOSFETs to positive and negative bias temperature stress (BTS), the instability of pMOS device parameters following *negative* BTS was found to be the most severe degradation mode and has become a major reliability concern in the last years [1]. Several physical models have been proposed to explain the microscopic origin of the build-up of electrically active defects during NBTS on pMOS devices [2–5]. Although the degradation following positive BTS is less severe [1,4,6] and thus of smaller importance for device manufacturers, more insight into this less studied PBTI will be an invaluable probe for existing theories.

Most physical models for the NBTI regard cold holes at the silicon–dielectric interface as the trigger for defect creation, such as a silicon dangling bond [7] or the E'_γ center [5,8]. During negative bias temperature stress in any MOS device, a large number of cold holes are available at the silicon–dielectric interface and may be captured into a defect precursor. By inverting the polarity of the stress bias, thus applying positive BTS, holes are repelled from the silicon–dielectric interface. Contrary to expectations, recent investigations showed a resulting build-up of donor-like charges, similar to, but smaller than that after negative BTS [9–11]. Existing studies on the PBTI were mostly made on devices of CMOS technology, where pMOS transistors are equipped with a p^{++} doped polycrystalline silicon (poly) gate and nMOS transistors with a n^{++} poly gate. Even though first observations of the PBTI on p^{++} gated pMOS devices were attributed to mobile oxide charges [12], the degradation effect was recently suggested to be similar to the NBTI but with holes provided by tunneling from the p^{++} poly gate [4,6]. This idea is supported by the fact that holes tunneling from the p^{++} poly gate towards the silicon substrate are the main contributors to the tunneling current in p^{++}/pMOS devices at low positive gate bias [13].

We show that the PBTI is indeed related to holes tunneling from the p^{++} poly gate for thin gate dielectric devices, but that an additional acceptor-like defect is created during PBTS independent of holes. We demonstrate this by studying the oxide thickness dependence of the degradation following PBTS on p^{++} and n^{++} gated pMOS devices. While the degradation following PBTS is independent of the oxide thickness for n^{++} gated pMOS devices, a strong oxide thickness dependence is observed for p^{++} gated devices. Furthermore we observe the creation of acceptor-like defects within the silicon band gap following PBTS in the absence of holes. The density of holes at the Si–SiO_2 interface is negligible for PTBS conditions in either n^{++} gated devices or devices with a sufficiently thick gate dielectric (cf. also Fig. 1).

2. Experimental setup

We used two sets of n- and pMOS devices with different types of gate poly doping of different technologies. The first set of devices were of a CMOS technology (p^{++} gated pMOS and n^{++} gated nMOS) with three differently thick SiON gate dielectrics. Their corresponding equivalent SiO_2 oxide thicknesses (EOTs) from capacitance voltage (CV) measurements, which include the quantum mechanical shift in substrate peak inversion layer density [6], were found to be 3.2 nm, 6.0 nm and 26.0 nm, respectively.

The second set of devices consisted of n- and pMOS devices with n^{++} poly gates and three differently thick pure SiO_2 gate

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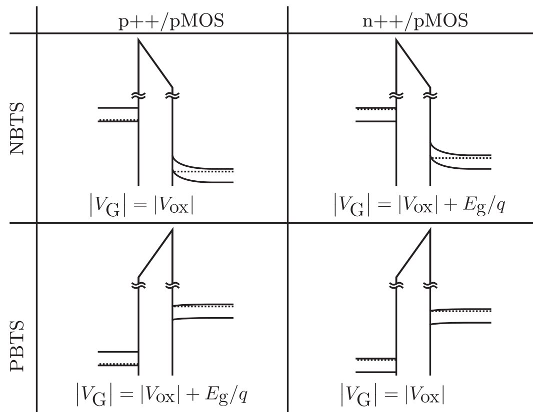

Fig. 1. Band structure and voltage drop for strong inversion or accumulation in p^{++}/pMOS and n^{++}/pMOS devices. The voltage V_G applied to the gate is either the voltage drop across the oxide V_{ox} or V_{ox} and the band gap of silicon E_g. A possible voltage drop due to the depletion of the gate poly is neglected.

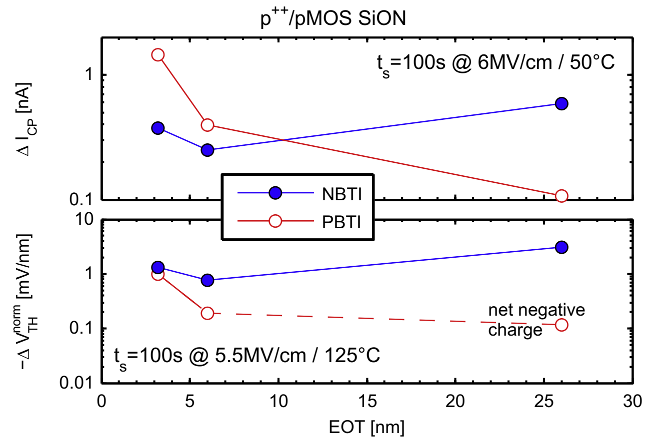

Fig. 2. Change of the maximum charge pumping current ΔI_{CP} (top, ≈40 ms post stress) and change of the normalized V_{TH} shift $\Delta V_{TH}^{norm} = \Delta V_{TH}/EOT$ (bottom, ≈10 ms post stress) over equivalent oxide thickness for p^{++}/pMOS devices after N- and PBTS. An increase of degradation (ΔI_{CP}) following PBTS with decreasing oxide thickness suggests that holes tunneling from the p^{++} poly gate may contribute to the degradation in thin dielectric p^{++} gated devices.

oxides with thicknesses 5.6 nm, 13.8 nm, and 29.1 nm, respectively. In Fig. 1 a sketch of the band structures of the p^{++}/pMOS and n^{++}/pMOS devices during N- and PBTS conditions and the corresponding voltage drop approximations for strong accumulation or inversion are depicted. A possible poly depletion voltage drop was neglected.

In order to monitor the stress induced degradation we performed two different measurements on separate devices directly after termination of stress. In the first experiment we switched the gate voltage from stress level to V_{TH} as determined by a current criterion and converted the difference in the drain current to a corresponding ΔV_{TH} with the help of the virgin $I_D V_G$ characteristic [14] after roughly 10 ms delay. In another experiment we started a charge pumping (CP) measurement with 1 MHz frequency directly after termination of stress and obtained the first maximum charge pumping current value after 41 ms of delay. Fast measurement of I_{CP} after stress is essential because ΔI_{CP} undergoes a significant recovery during the CP measurement itself, which may be attributed to detrapping of positive charges from defect sites [15]. We remark that the ΔI_{CP} may reflect the overall degradation of the device following BTS because the CP current is not only composed of contributions of the average density of interface traps but also of the density of border traps [16] near the Si–SiO_2 interface [17,18] which may be involved in the microscopic BTI mechanism [5,4,15]. To address different V_{FB} and V_{TH} for the different equivalent oxide thicknesses we adapted the high and low voltage levels of the CP pulse in order to measure the maximum charge pumping current, while keeping the slope of the pulses and thus the scanned energy interval the same for all devices [19].

3. Experimental results

In Figs. 2 and 3 the equivalent oxide thickness normalized V_{TH} shift and the change of the I_{CP} after BTS as a function of the EOT are depicted for the p^{++} gated and n^{++} gated pMOS devices, respectively. The NBTI in either p^{++} or n^{++} poly gated devices is nearly independent of the equivalent oxide thickness, regarding both V_{TH} shift and I_{CP} change, consistent with earlier work [20,21]. The PBTI shows a complex picture in two regards. First, vastly different dependences on the EOT for devices with different gate poly doping are observed. While the degradation in n^{++}/pMOS devices is independent of the oxide thickness, it increases strongly with decreasing oxide thickness in p^{++}/pMOS devices. The ΔV_{TH} even changes its sign with decreasing EOT, such that a very small net negative charge is built up for the device with 26 nm equivalent

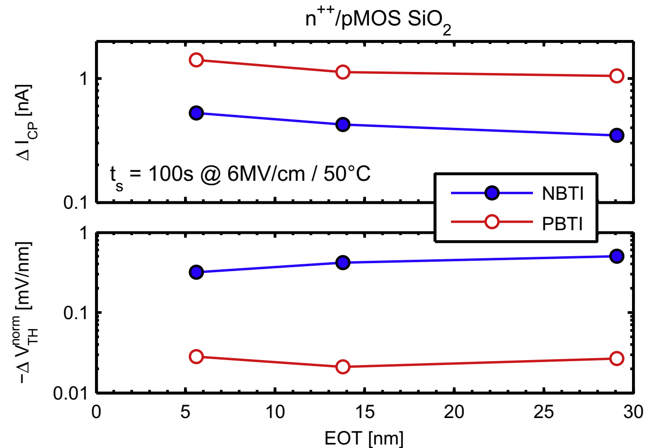

Fig. 3. The degradation following N- and PBTS for n^{++}/pMOS device is independent of the oxide thickness. This indicates that the oxide field value is the only relevant parameter for the N- and PBTI in n^{++} poly gated devices.

gate oxide thickness, and a net positive charge for devices with thinner dielectrics. Second, when comparing to NBTI, we see that even though ΔV_{TH} may be quite small, ΔI_{CP} is even higher than after NBTS for the n^{++}/pMOS (c.f. Fig. 3). In Figs. 4 and 5 the oxide field dependence of the change of the charge pumping current is depicted for the p^{++}/pMOS and the n^{++}/pMOS devices, respectively. All degradation modes except the PBTI in p^{++}/pMOS devices show a power law exponent $\Delta I_{CP} \propto E_{ox}^b$ of $b \approx 4$ [22,15]. The lower power law exponent of the PBTI on p^{++}/pMOS devices differs vastly from all other combinations which motivates further investigations on the PBTI on p^{++}/pMOS devices. We remark that the lower power law exponent of the PBTI on p^{++}/pMOS devices may occur because two separate mechanisms (carrier tunneling and BTI degradation), which are both heavily dependent on the oxide field, act together. Again, we observe that the ΔI_{CP} after PBTS is greater than the ΔI_{CP} after NBTS for all stress fields. Figs. 6 and 7 depict the ΔI_{CP} and ΔV_{TH} *recovery* traces after PBTS of pMOS and nMOS devices. The thin dielectric p^{++}/pMOS of Fig. 6 show typical NBTI-like recovery, i.e. ΔI_{CP} and negative ΔV_{TH} decrease with time (loss of net positive charge). This shows that for thin dielectrics covered by a p^{++} polygate, PBTI is essentially inverted NBTI with holes provided by

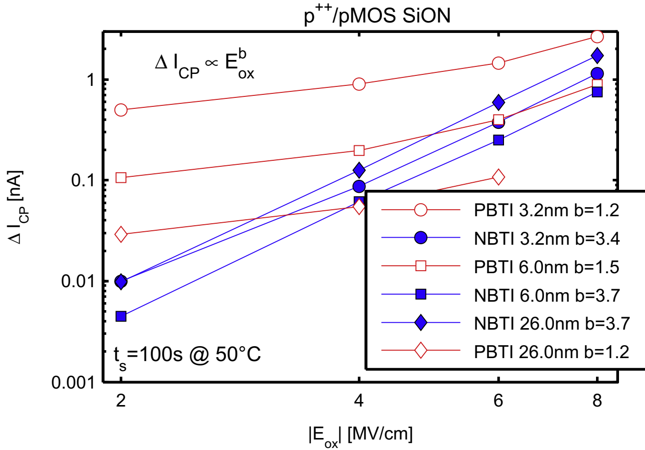

Fig. 4. CP current degradation for the p^{++}/pMOS set of devices. The vastly different power law coefficient of the PBTI degradation on the p^{++}/pMOS devices hints that the BTI degradation is not the only field dependent mechanism involved. Also holes have to be supplied by the gate, which is as well strongly oxide field dependent and thus changing the power law.

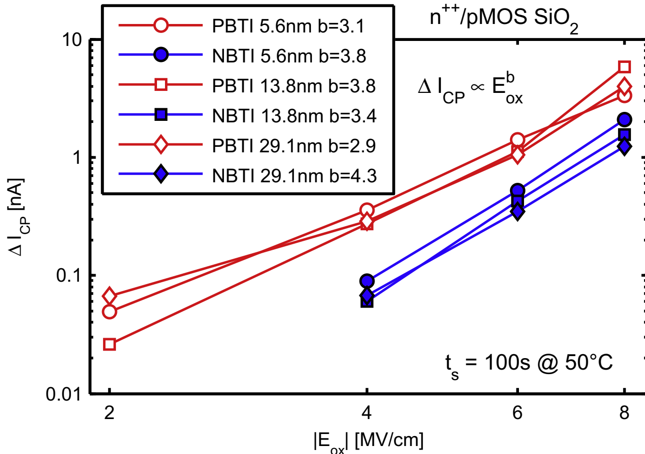

Fig. 5. The degradation following N- or PBTS for the n^{++}/pMOS devices shows a similar power law exponent indicating ordinary BTI degradation mechanisms. For the NBTI, a power law exponent of $b \approx 4$ is obtained consistent with the bulk of literature [4,15].

the gate. For the n^{++} gated nMOS after PBTS, there are no free holes and we would normally not expect any drift or recovery. However, Fig. 6 shows a substantial degradation by negative charges and recovery of negative charges, together with a recovery of ΔI_{CP}. The same holds true for thick dielectrics, as depicted in Fig. 7, with almost identical ΔI_{CP} recovery for nMOS and pMOS independent of poly doping. The same behavior is also observed for trench MOS devices (n^{++} gated nMOS) after PBTS in Fig. 8. A closer look on the results depicted in Fig. 7 reveals that defects are created through PBTS for all devices (change of the I_{CP}), while the pMOS experience virtually no V_{TH} shift. This behavior may be explained with the creation and annealing of acceptor-like defects with energy levels within the band gap of Si. The Fermi level lies close to the valence band edge of Si for a pMOS in inversion. Acceptor-like defects (neutral when unoccupied and negatively charged when occupied, 0/−) are therefore not charged at the V_{TH} of a pMOS. On the other hand, the Fermi level for an nMOS in inversion lies close to the conduction band edge and acceptor-like defects are negatively charged [23]. Therefore, after PBTS an equivalent degradation level is observed in the ΔI_{CP}, regardless of the transistor

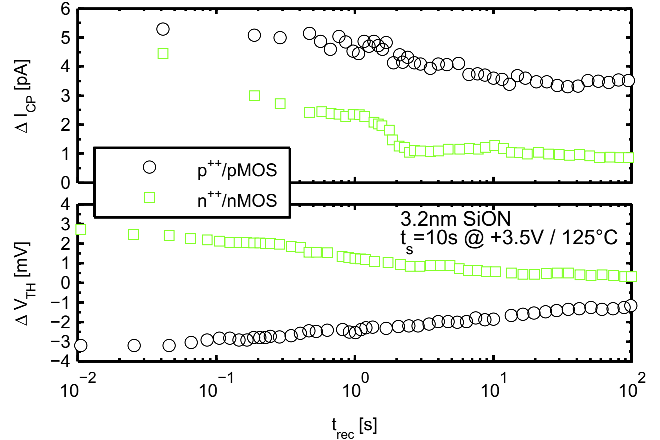

Fig. 6. For *thin* gate dielectric p^{++}/pMOS devices the degradation and recovery behavior following PBTS differs vastly from the behavior of all other devices. Rather a negative threshold voltage shift and recovery towards zero is observed, which indicates positively charged defects recovering, just as after NBTS. The thin gate dielectric n^{++}/nMOS behaves equivalently to the thick dielectric devices as depicted in Fig. 7 because the n^{++} poly gate cannot provide any holes to trigger NBTI degradation.

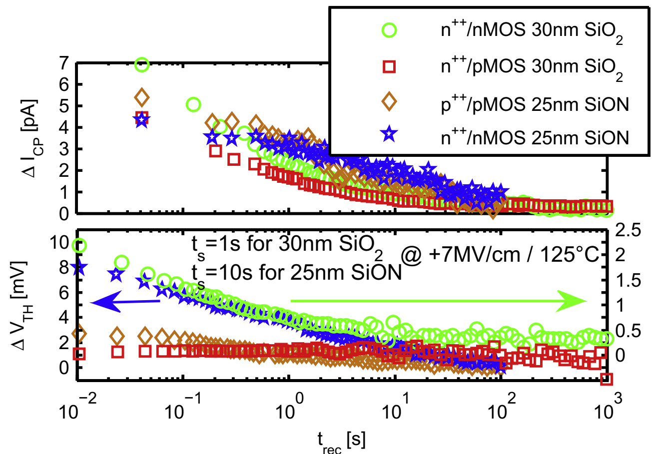

Fig. 7. For *thick* gate dielectrics, PBTS causes roughly the same degree of oxide damage (cf. ΔI_{CP}), regardless of the gate poly doping type. The defects are energetically situated within the silicon bandgap because they are visible in the ΔV_{TH} only for nMOS devices, where the Fermi level is near the conduction band edge at V_{TH} (occupied acceptor-like defects are negatively charged, causing positive ΔV_{TH}). For the pMOS the defects are unoccupied and thus neutral. Consequently the recovery of the defects is not visible in the ΔV_{TH} of a pMOS.

type, consistent with earlier work [23]. For the nMOS a positive ΔV_{TH} due to negatively charged defects is measured, whereas the acceptor-like defects give rise to ΔI_{CP} for pMOS and nMOS alike but are not ΔV_{TH} relevant for the pMOS. We remark that acceptor-like defects may be due to negatively charged E'_{γ} centers [24].

The finding that acceptor-like defects are created through PBTS is in disagreement with earlier work [25], where researchers proposed the creation of donor-like defects following PBTS on devices with thick gate oxides. The results in [25] are based on $I_D V_G$ sweeps in the linear regime of the transistor before and after stress. However, in a repetition of the experiment we found a strong dependence of the ΔV_G on the voltage applied to the drain V_D, as depicted in Fig. 9. In the linear regime of the transistor ($V_D < V_D^{sat}$) ΔV_G is largely negative above the threshold voltage of the device (ΔV_G is measured with $V_G > V_{TH}$ in [25]). This negative shift nearly vanishes when measuring the characteristic in saturation, even though the V_D should not affect the ΔV_G at all.

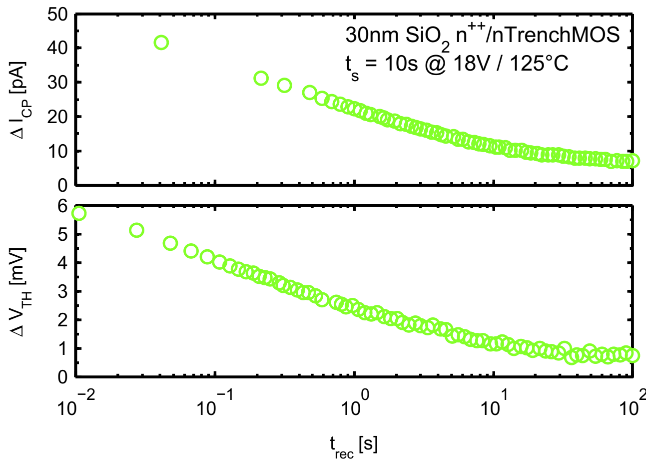

Fig. 8. The build-up of acceptor-like charges following PBTS on n++ gated devices is observed in a wide range of different technologies. Also e.g. in n-channel power transistors using an SiO_2 oxide at the vertical face of an etched trench in silicon (Trench-MOSFET) a very similar behavior to that of lateral devices is observed.

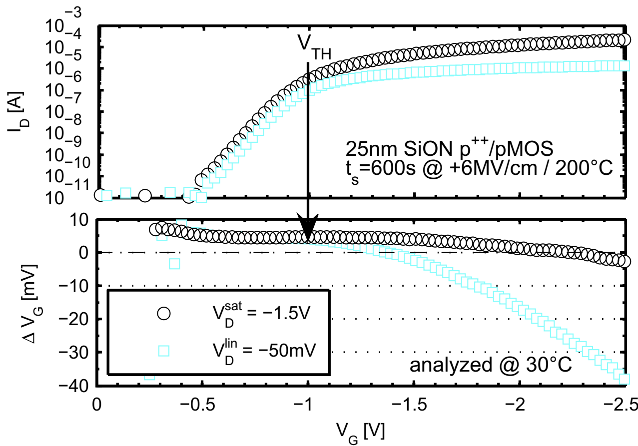

Fig. 9. A repetition of the experiment of Ref. [25] shows a strong dependence of the drift following PBTS on the drain voltage. When measuring in the linear regime ($V_D < V_D^{sat}$) the influence of the spurious ΔV_{TH} shift due to a change in effective channel mobility leads to the misinterpretation that donor-like defects are created during stress. A measurement in the saturation region ($V_D > V_D^{sat}$) decreases the parasitic effect due to mobility changes. Regardless of the operating mode the net drift at the V_{TH} of the device is slightly positive, hinting at negatively charged defects.

The strong difference in ΔV_G with different V_D occurs because changes in the effective channel mobility μ have a different impact on the measured drain current. The channel length decrease in saturation due to pinch-off reduces the impact of the channel mobility changes on the change of the drain current. This may be deduced from first order models for the drain current in the linear (lin) and saturation (sat) regime of a transistor [26]

$$I_D^{lin} = -\frac{W}{L}\mu C_{ox}\left(V_G - V_{TH} - \frac{V_D}{2}\right)V_D \tag{1}$$

$$I_D^{sat} = -\frac{1}{2}\frac{W}{L}\mu C_{ox}(V_G - V_{TH})^2, \tag{2}$$

with W the channel width, L the channel length and C_{ox} the oxide capacitance. From these formulas it follows that changes in the drain current may be due to mobility changes or shifts of the V_{TH} as [27]

$$\frac{\Delta I_D^{lin}}{I_D^{lin}} = \frac{\Delta\mu}{\mu} - \frac{\Delta V_{TH}}{V_G - V_{TH} - V_D/2} \tag{3}$$

$$\frac{\Delta I_D^{sat}}{I_D^{sat}} = \frac{\Delta\mu}{\mu} - \frac{2\Delta V_{TH}}{V_G - V_{TH}}. \tag{4}$$

For a large overdrive ($V_G - V_{TH} \gg \Delta V_{TH}$) the change in effective channel mobility μ dominates the change of I_D. When operating the transistor in the saturation regime the impact of the V_{TH} shift on the change of the drain current is roughly two times larger compared to the linear regime.

4. Conclusion

When subjecting thin gate dielectric pMOS transistors with a p++ polycrystalline silicon gate to PBTS a strong dependence of the overall degradation on the equivalent gate oxide thickness is observed. For thin gate dielectric devices the degradation after PBTS is similar to that after NBTS. This demonstrates that the PBTI in p++ gated pMOS devices can be considered as an NBTI-like degradation mechanism triggered by holes tunneling from the p++ poly gate towards the silicon–dielectric interface.

If holes are absent during stress, acceptor-like defects are created which are energetically situated within the bandgap of silicon. These defects are only charged and visible in V_{TH} shifts of nMOS transistors, where the Fermi level is near the conduction band edge of silicon during device operation. A possible source for misleading interpretation of measurement results due to mobility changes of former research was revealed and disqualified.

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