Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics

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Abstract
Quantized threshold voltage (VTH) relaxation transients are observed in nano–scaled field effect transistors (FETs) after bias temperature stress. The abrupt steps are due to trapping/detrapping of individual defects in the gate oxide and indicate their characteristic emission/capture times. Individual traps are studied in n-channel SiO2/HfSiO FETs after positive gate stress to complement previous studies performed on SiO(N). Similarly to single SiO(N) traps, strong thermal and bias dependences of the emission and capture times are demonstrated. The high-k traps have a higher density but a reduced impact on VTH due to their separation from the channel.

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1. Introduction
As the dimensions of metal oxide semiconductor field effect transistors (MOSFETs) shrink toward the nanometer scale, the discrete behavior of individual defects is revealed. Quantized threshold voltage VTH transients after bias temperature stress have been observed in deeply scaled MOSFETs due to the emission and capture of individual carriers in gate oxide traps [1–4]. This phenomenon has been explored to study the statistical properties of single traps in MOSFETs [5–7] after bias temperature stress. A new technique named time dependent defect spectroscopy (TDDS) has been developed and successfully applied on SiO(N) p-channel (pFETs) [6,7] and n-channel FET (nFETs) [5] after negative and positive gate stress, respectively.

In this work, we first present a statistical comparison of the discrete threshold voltage shifts in a larger number of SiO(N) nFETs and, technologically more relevant, SiO2/HfSiO nFETs after positive bias stress. Even though the trap density in HfSiO is larger, they have a reduced impact on the total threshold voltage shift due to their larger separation from the channel. Next, a set of individual traps in a single SiO2/HfSiO nFET is analyzed. Similarly to the SiO(N) traps, the emission and capture times of high-k traps show strong thermal and bias dependences.

2. Experimental
In our experiment a DC signal was applied to the gate of nFETs with 1.8 nm-SiO(N) or 0.8 nm-SiO2/1.8 nm-HfSiO gate dielectrics. The drawn gate dimensions for both cases were L × W = 70 × 90 nm². A stress signal VSTRESS was applied for a stress time tSTRESS. Afterward, the relaxation transient was measured at VRELAX for a relaxation time tRELAX. The drain voltage VD was 0.1 V. During this entire process the source current IS was registered and transformed into a VTH shift via a reference IS – VG curve of the device taken prior to stress [8]. The VRELAX was chosen close to the threshold voltage VTH of the device so that ΔIS varies strongly with respect to the absolute value of IS. Keithley 2602 source-measure units were used for this experiment.

3. Statistical comparison of SiO(N) and SiO2/HfSiO nFETs
Fig. 1 shows the typical relaxation transients obtained on (a) SiO(N) and (b) SiO2/HfSiO stacks under the gate oxide electric field of 13 MV/cm for 240 ms. The VTH transients show a discrete behavior due to electron emission from individual traps [2]. As opposed to the clean VTH relaxation traces obtained in SiO(N) nFETs, the high-k stacks present a higher level of noise. When the VTH step heights are displayed in a complementary cumulative plot normalized to the number of traces (see Fig. 2), it is observed that the number of steps, i.e., traps, after identical stress conditions (the
electric field and time) is larger for the HfSiO stacks than for the SiO(N) stacks. Indeed a significant number of SiO(N) devices did not show any step. The step heights for SiO(N) shown in Fig. 2a follow an exponential distribution [9] with an average value $g = 5.4$ mV and a trap density $N_T = 0.19$ trap/device. However, a clearly bimodal distribution can be observed for HfSiO. Each mode can be fitted by means of the maximum likelihood method using two exponential distributions with $g_1 = 3.7$ mV and $N_{T1} = 0.3$ trap/device and $g_2 = 0.85$ mV and $N_{T2} = 2.6$ trap/device, respectively. Fig. 3 shows the likelihood functions assuming a monomodal distribution and a bimodal distribution for the step heights detected in the high-k stack. The no overlap among the regions strengthens the bimodality assumption with a high level of significance. Distribution 1 ($g_1$) is similar to SiO(N), both in $g$ and in magnitude $N_T$. We therefore argue that this is due to defects in the SiO$_2$ layer. Since the $g$ value is related to the centroid ($x_0$ distance from the gate) of the trapped electrons in the dielectric [4,10], i.e., $g \propto x_0$, distribution 2 corresponds to the defects in the high-k dielectric ($g_2$). Also it is worth noting that the number of steps per device $N_{T2}$ is 10 times larger than $N_{T1}$. This indicates a higher density of traps in the high-k dielectric. However, the impact on the total $V_{TH}$ is reduced since $g_2$ is significantly lower. Therefore, the large density of high-k traps with a small impact on the $V_{TH}$ explains the larger noise level observed in the high-k stack (Fig. 1b).

4. Individual traps in a single SiO$_2$/HfSiO nFET

Fig. 4 shows three typical relaxation curves taken on a single SiO$_2$/HfSiO nFET. Under the conditions of the experiment, the selected device has four active traps with $V_{TH}$ step heights lower than 4 mV. From the bimodal distribution shown in Fig. 2b, the probability of observing a high-k trap with a $V_{TH}$ step height of 2 mV or lower is significantly larger than for SiO$_2$ traps. This suggests that there is a high probability that the traps observed in Fig. 4 are located in the high-k material.

As in the case of SiO(N) devices [5], every high-k trap has its characteristic emission time and $V_{TH}$ shift, which form the ‘fingerprint’ of the defect (see Fig. 5a). However, the extracted clusters are not as compact as those observed in SiO(N) due to the higher level
of noise present in the high-k stack. Note that all four clusters in Fig. 5a shift to shorter emission times with increasing temperature (Fig. 5b). Trap #1 shifts out of the experimental window, while a new trap #5 appears. Fig. 6a shows the histogram of the emission times $t_e$ of the trap #3 for two $V_{\text{STRESS}}$ values. As expected for Markov processes [7,11], the emission times can be fitted to an exponential distribution in order to obtain the characteristic emission time $\tau_e$. Similarly to SiO(N) [5], the emission time $\tau_e$ is independent of the stress time. Fig. 6b displays the Arrhenius plot of the characteristic emission time $\tau_e$. It presents a strong thermal activation with $E_A = 0.48$ eV. Fig. 7 shows that the intensity of the cluster associated with trap #3 increases with stress time up to the saturation level determined by the characteristic emission ($\tau_e$) and capture ($\tau_c$) times at $V_{\text{STRESS}}$ as shown in the equation of Fig. 7 [11]. These characteristic times are strongly temperature (Fig. 7a) and voltage (Fig. 7b) dependent. The reduction of the occupancy with temperature is related to a higher activation energy of $\tau_e$ with respect to $\tau_c$. The $P_C$ increase with $V_{\text{STRESS}}$ is due to the decrease of $\tau_c$ with increasing $V_{\text{STRESS}}$.

Interestingly, in Fig. 5b, a new trap (trap #5) that causes a negative $V_{\text{TH}}$ shift appears in the TDDS spectrum at high temperature. We hypothesize that this effect is due to electron discharge from the dielectric to the gate during stress [12]. Therefore, electron emission takes place during stress condition and electron capture occurs during relaxation. As we will see in the following, this trap follows analogous kinetics as the other four (#1–4). Fig. 8 shows the intensity of cluster #5 as a function of the stress time for different temperatures. The emission probability increases with $V_{\text{STRESS}}$ and can be described by the equation given in Fig. 7 after exchanging the capture and emission times. Again, this process is clearly thermally activated as shown in the Fig. 9. In the inset of Fig. 9, the histogram of the capture times shows that the capture process can also be described by an exponential distribution. The activation energy obtained from the fit of the data to an Arrhenius law is 0.8 eV. The activation energies found in this study are close to the values obtained in SiO(N) pFETs after negative stress [6,7], and those of SiO(N) nFETs after positive stress [5].
5. Conclusion

We have shown that SiO$_2$/HfSiO nFET traps are located both in the SiO$_2$ and in the high-k dielectric. High-k traps have a reduced impact on the $V_{TH}$ shift after stress but produce a high level of noise in the source current. We have demonstrated that the statistical properties of individual traps in SiO(N) and HfSiO dielectrics after positive stress follow analogous kinetics as described by Markov processes.

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