Microelectronic Engineering 88 (2011) 1388–1391

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

On the impact of the Si passivation layer thickness on the NBTI of nanoscaled $Si_{0.45}Ge_{0.55}$ pMOSFETs

J. Franco [a,b,*], B. Kaczer [a], M. Toledano-Luque [a,c], Ph. J. Roussel [a], P. Hehenberger [d], T. Grasser [d], J. Mitard [a], G. Eneman [a,b,e], L. Witters [a], T.Y. Hoffmann [a], G. Groeseneken [a,b]

[a] Imec, Kapeldreef 75, 3001 Leuven, Belgium
[b] ESAT, Katholieke Universiteit Leuven, Belgium
[c] Dpto. Física Aplicada III, Universitad Complutense Madrid, Spain
[d] Technische Universität Wien, Austria
[e] FWO-Vlaanderen, Belgium

ARTICLE INFO

Article history:
Available online 30 March 2011

Keywords:
NBTI
SiGe
Si
Cap
pMOSFET
Passivation
Reliability

ABSTRACT

The negative bias temperature instability (NBTI) of nanoscaled $Si_{0.45}Ge_{0.55}$ pFETs with different thicknesses of the Si passivation layer (cap) is studied. Individual discharge events are detected in the measured threshold voltage shift (ΔV_{th}) relaxation traces, with exponentially distributed step heights. The use of a thinner Si cap is shown to reduce both the average number of charge/discharge events and the average ΔV_{th} step height. To qualitatively explain the experimental observations, a simple model including a defect band in the dielectric is proposed.

1. Introduction

We have recently shown that SiGe pMOSFETs with buried channel architecture can alleviate the NBTI issue for ultra-thin EOT devices [1]. A crucial impact of the Si cap thickness was found, with thinner Si caps significantly improving the reliability, possibly by reducing the interaction between channel carriers and dielectric defects thanks to a favorable Fermi level alignment shift [2,3]. This allowed us to demonstrate 6 Å EOT $Si_{0.45}Ge_{0.55}$ pFETs with a 10 year lifetime at operating V_{DD} of 1 V [2]. However, those studies were performed on large area test devices, as customary for standard NBTI studies. Recent works have shown that as device geometries scale toward atomistic dimensions *both* the fresh device parameters *and* the parameter *shifts* during device operation become statistically distributed. At the same time, individual charge/discharge events become visible in the V_{th} transients, providing a new way to study oxide trap properties [4–7]. For these reasons, in this work we focus on the NBTI of nanoscaled $Si_{0.45}Ge_{0.55}$ pFETs, looking in particular into the impact of different Si cap thicknesses.

2. Experimental

$Si_{0.45}Ge_{0.55}$ pFETs with metallurgic length $L \approx 35$ nm (drawn $L = 70$ nm) and width $W = 90$ nm were used in this study. The device gate stack (Fig. 1) consisted of a Si cap with three different thicknesses in the range of 0.65–2 nm (as grown), a SiO_2 interfacial layer (~0.8 nm), an HfO_2 dielectric (~1.8 nm), and a metal gate. More information on the process can be found in [8]. Up to 160 nominally identical devices were used for the statistical studies.

3. Results and discussion

A representative set of typical NBTI relaxation transients recorded with the extended measure-stress-measure (eMSM) technique [9] on nanoscaled SiGe devices is shown in Fig. 2a. As previously reported for Si devices [4,5], the total ΔV_{th} observed after the same NBTI stress strongly varies from device to device. Single discharge events are visible, and the ΔV_{th} step heights are exponentially distributed (Fig. 2b, complementary cumulative distribution function, CCDF ≡ 1-CDF) [5]. Several single discharge events are observed causing ΔV_{th} as large as 20 mV. The step heights and the trap emission times are uncorrelated (not shown), as observed in [5] for the case of RTN, confirming that charge emission does not follow a simple elastic model [10]. While for large area devices the total ΔV_{th} depends on the stress time (Fig. 3a)

* Corresponding author at: Imec, Kapeldreef 75, 3001 Leuven, Belgium.
E-mail address: jacopo.franco@imec.be (J. Franco).

0167-9317/$ - see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2011.03.065

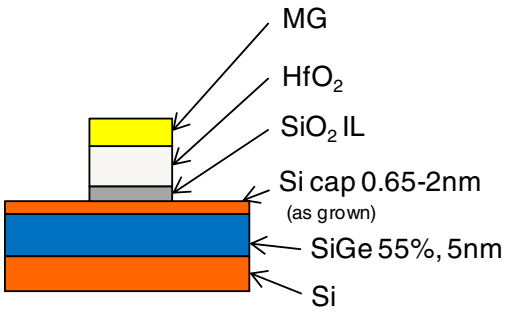

Fig. 1. Gate stack of the SiGe devices under test. Gate metallurgic length L was ~35 nm (drawn L = 70 nm), while gate width was 90 nm.

and on the stress gate overdrive voltage, for nanoscaled device the average number of discharge events per single stressed device is observed to follow similar dependences (Fig. 3b). A thinner Si cap on SiGe pFETs was found to strongly reduce the large area device ΔV_{th} at fixed stress oxide electric field (Fig. 4a). In a similar way, a thinner Si cap causes a strong reduction of the average number of ΔV_{th} steps (i.e. trapped charges) in nanoscaled devices (Fig. 4b, different stress conditions w.r.t. Fig. 4a). It is also worth noticing that the very small number of discharge events observed complicates the study, requiring large sample sets to get reliable statistics.

Moreover, the CCDFs of the step heights for different Si cap thicknesses reveal that a thinner cap causes a reduction of the average step height (η) as shown in Fig. 5 (η = 3.9 mV for a 2 nm Si cap and η = 1.8 mV for a 0.65 nm Si cap). As shown in Fig. 6, this observation is confirmed at several stress equivalent oxide electric fields (E_{ox}). Moreover, the observed η values are significantly lower w.r.t. the values previously observed for Si devices with similar gate stack (Si Ref. data from [5], η = 4.8–5.7 mV). Hence, the use of a thin Si cap on a SiGe channel reduces both the average number of steps and the average ΔV_{th} step height after NBTI stress, confirming to be extremely beneficial also for the nanoscaled device reliability.

A possible model to explain the experimental observations relies on the existence of a defect band in the dielectric at a narrow energy level, e.g. in the SiO_2 at $E_{v\_Si} - 0.4$ eV, as observed in [10]. As depicted in Fig. 7, the Fermi level in the SiGe channel determines which part of the defect band will be accessible to channel holes. I.e. for a thin Si cap only a small part of the defect band located on the gate side of the dielectric is accessible, while the larger voltage drop on a thicker Si cap lowers the Fermi level making more defects accessible to channel holes. This interpretation qualitatively agrees with the higher average number of trapped charges observed for devices with a thicker Si cap. Moreover, the additionally accessed defects, being located nearer to the channel, shift the centroid (x_t in Fig. 7) of the total trapped charge closer to the channel, explaining the observed higher η (Fig. 5) [11].

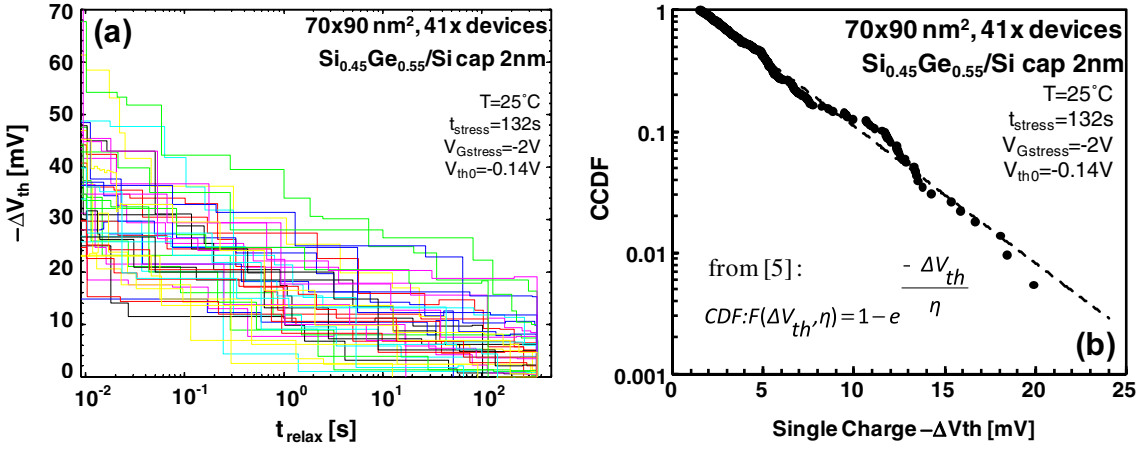

Fig. 2. (a) NBTI relaxation transients recorded on nanoscaled SiGe devices (measurement noise was filtered out), with visible single discharge events. (b) The complementary cumulative distribution function (CCDF ≡ 1-CDF) shows the ΔV_{th}s per single discharge event are exponentially distributed.

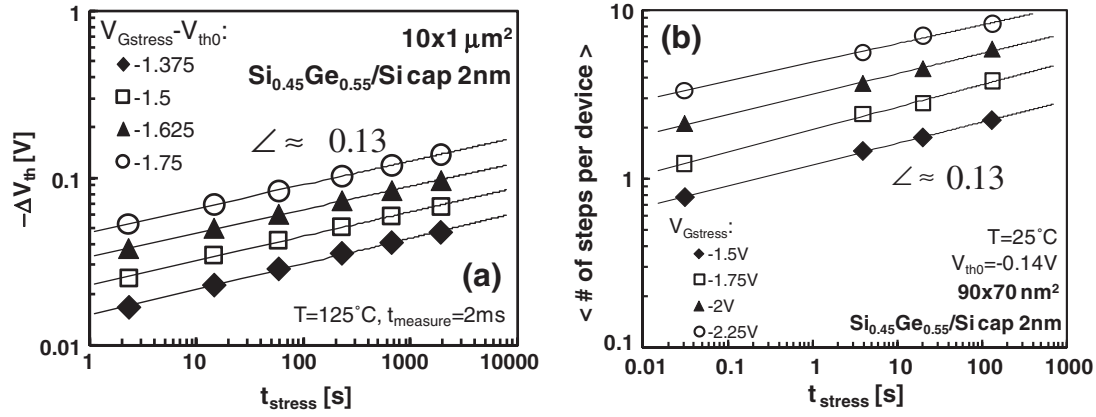

Fig. 3. (a) For large-area devices, the total ΔV_{th} depends on the stress time and voltages. (b) For nanoscaled devices, the average number of discharge events (i.e. trapped charges per device) follows similar dependences.

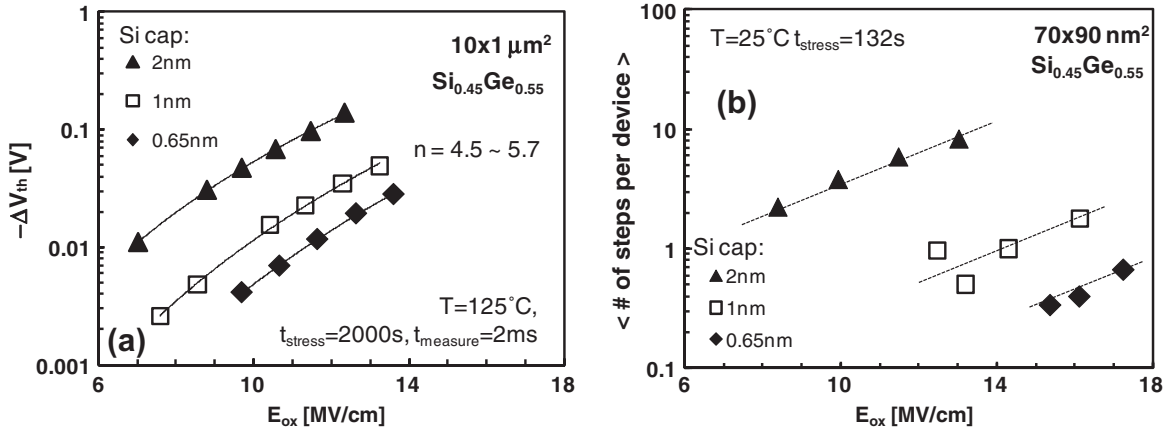

Fig. 4. (a) The use of a thinner Si cap reduces the total ΔV_{th} on a large area device (re-plotted from [1], field acceleration power-law exponents $n \approx 4.5$ for the thickest cap, while $n \approx 5.7$ for the thinnest cap) and (b) the average number of discharge events per device on nanoscaled SiGe pFETs (lines are guides to the eye here). Note: $E_{ox} \approx |V_G - V_{th0}|/T_{inv}$ here (E_{ox} estimation from capacitance–voltage measurements was not possible due to the small area devices having C_{ox} values below the detection limit of standard measurement equipment; $T_{inv} = CET(V_{th0} - 0.6\,V) \approx EOT + 4$ Å). As one can notice, very high oxide electric fields, up to ~18 MV/cm, had to be applied in order to cause trap charging in SiGe devices with thinnest Si cap. This further proves the improved NBTI reliability of this technology. Furthermore, time dependent dielectric breakdown (TDDB) did not constitute a showstopper even at such high electric fields thanks to its area scaling.

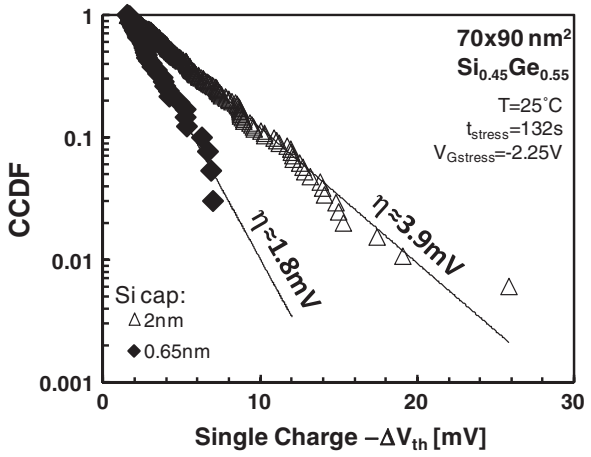

Fig. 5. The average ΔV_{th} step height (η) is reduced when using a thinner Si cap.

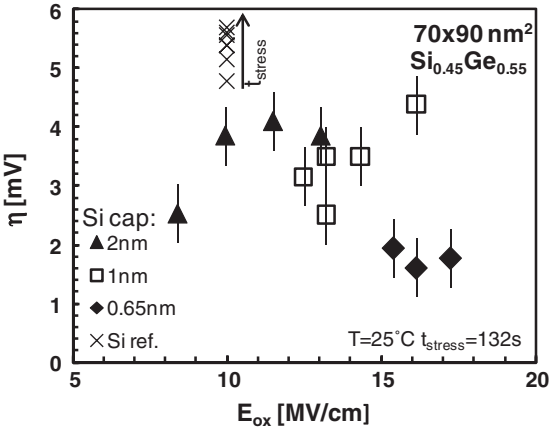

Fig. 6. Extracted average ΔV_{th} step heights (η) as a function of the stress electric field for different Si cap thicknesses. Devices with a thinner Si cap show lower η, while in general SiGe devices show lower η w.r.t. Si Ref. data from [5].

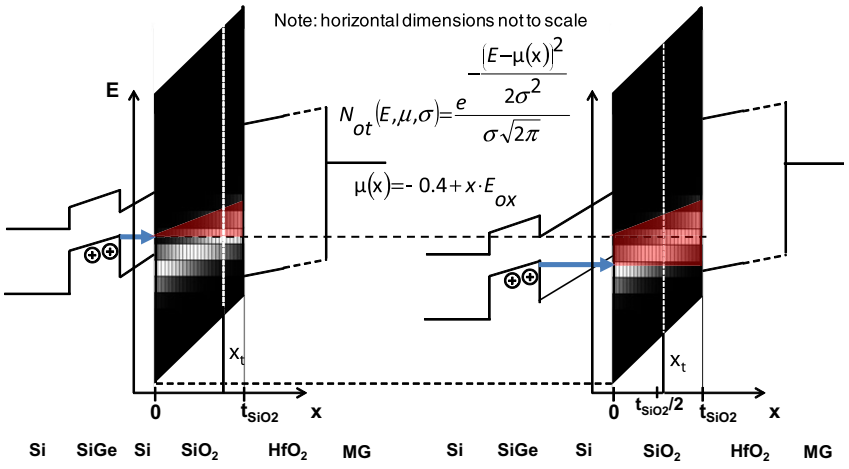

Fig. 7. Assuming the existence of a defect band (modeled as a Gaussian distribution of traps over the oxide energy bandgap) in the dielectric (e.g. in the SiO_2 as observed in [10]) can explain the experimental observations. With thinner Si cap only a small part of the defect band located on the gate side can interact with channel holes, while for a thicker cap more defects become accessible on the channel side, explaining the higher average number of trapped charges per device and the higher η [11].

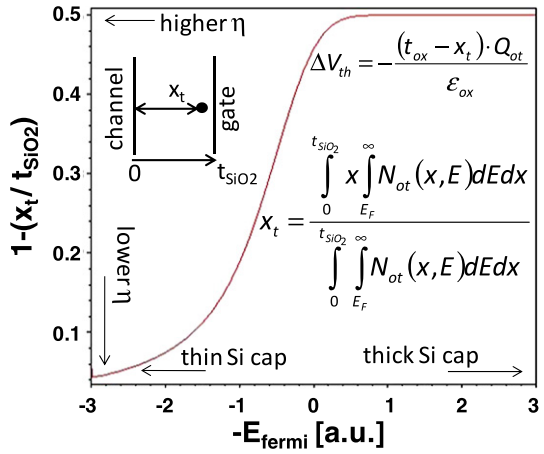

Fig. 8. Centroid of the accessible traps calculated for different values of the Fermi level in the channel. The model proposed in Fig. 7 qualitatively agrees with the experimental observation of the η dependency on the Si cap.

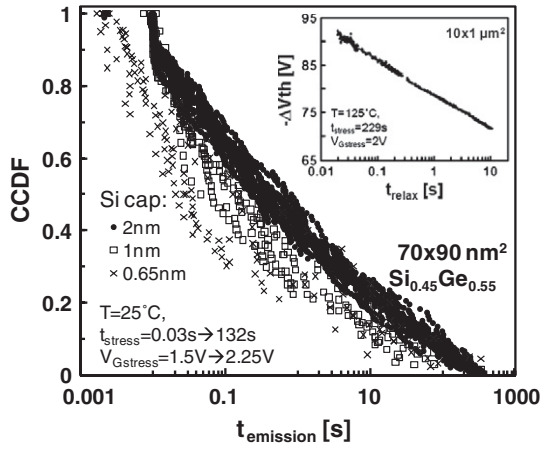

Fig. 9. The CCDF of the emission times observed for several stress times and voltages and for different Si cap thickness are reminiscent of the relaxation traces observed on large area devices. For comparison, the inset shows a typical ΔV_{th} relaxation trace for a $10 \times 1\ \mu m^2$ with a 2 nm Si cap. The emission time distributions appear to be shifted toward lower emission times for thinner Si cap, suggesting a faster discharge of the trapped charges after stress removal.

A defect band is assumed with a Gaussian density of states (see the SiO_2 layer and the Eq. in Fig. 7) with its mean value μ centered at $E = E_{v\_Si} - 0.4$ eV at the Si/SiO_2 interface and linearly changing with depth (with slope E_{ox}) to account for the voltage drop in the dielectric. The centroid of the accessible traps (assuming all traps are charged after NBTI stress) can be numerically calculated for different values of the Fermi level in the channel. As shown in Fig. 8, this simple model qualitatively agrees with the experimental observation of the η dependency on the Si cap (shown in Fig. 6).

Finally the complementary cumulative distribution of the emission times observed for several stress times and voltages are plotted in Fig. 9 for different Si cap thickness. Interestingly the emission time distributions appear to be shifted toward lower values for thinner Si cap, suggesting a faster discharge of the trapped charges after stress removal, i.e. a faster *initial* relaxation.

4. Conclusion

The NBTI reliability of nano-scaled $Si_{0.45}Ge_{0.55}$ pFETs was studied as a function of the Si cap thickness. Individual discharge events are visible in the ΔV_{th} relaxation traces, with exponentially distributed step heights. The ΔV_{th} step heights and the corresponding charge emission times were observed to be uncorrelated. The average number of discharge events follows the typical NBTI dependences on stress time and voltage observed for the total ΔV_{th} on large area devices. The use of a thinner Si cap on SiGe was found to dramatically reduce the average number of discharge events and the average ΔV_{th} step height (η), confirming this technology to be extremely promising also for nanoscaled device reliability. A simple model including a defect band in the dielectric can qualitatively explain the experimental observation, suggesting that fewer defects located on the gate side of the dielectric are accessible by the channel holes when reducing the Si cap thickness, thanks to a favorable Fermi energy alignment.

Acknowledgements

This work was carried out as part of imec's Industrial Affiliation Program funded by imec's Core Partners. The imec pilot line and Amsimec are also acknowledged for their support.

References

[1] J. Franco, B. Kaczer, M. Cho, G. Eneman, T. Grasser, G. Groeseneken, Proc. IRPS (2010) 1082–1085.
[2] J. Franco, B. Kaczer, G. Eneman, J. Mitard, A. Stesmans, V. Afanas'ev, T. Kauerauf, Ph.J. Roussel, M. Toledano-Luque, M. Cho, R. Degraeve, T. Grasser, L.-Å. Ragnarsson, L. Witters, J. Tseng, S. Takeoka, W.-E. Wang, T.Y. Hoffman, G. Groeseneken, Proc. IEDM (2010) 70–73.
[3] S.J. Mathew, G. Niu, W.B. Dubbelday, J.D. Cressler, J.A. Ott, J.O. Chu, P.M. Mooney, K.L. Kavanagh, B.S. Meyerson, I. Lagnado, Proc. IEDM (1997) 815–818.
[4] V. Huard, C. Parthasarathy, C. Guerin, T. Valentin, E. Pion, M. Mammasse, N. Planes, L. Camus, Proc. IRPS (2008) 289–300.
[5] B. Kaczer, T. Grasser, Ph.J. Roussel, J. Franco, R. Degraeve, L. -Å Ragnarsson, E. Simoen, G. Groeseneken, H. Reisinger, Proc. IRPS (2010) 26–32.
[6] T. Grasser, H. Reisinger, P. Wagner, F. Schanovsky, W. Goes, B. Kaczer, Proc. IRPS (2010) 16–25.
[7] M. Toledano-Luque, B. Kaczer, Ph.J. Roussel, M. Cho, T. Grasser, G. Groeseneken, J. Vac. Sci. Technol. B 29 (01AA04) (2011) 1–5.
[8] L. Witters, S. Takeoka, S. Yamaguchi, A. Hikavyy, D. Shamiryan, M. Cho, T. Chiarella, L.-Å. Ragnarsson, R. Loo, C. Kerner, Y. Crabbe, J. Franco, J. Tseng, W.-E. Wang, E. Rohr, T. Schram, O. Richard, H. Bender, S. Biesemans, P. Absil, T. Hoffmann, Proc. VLSI Symp. (2010) 181–182.
[9] B. Kaczer, T. Grasser, Ph.J. Roussel, J. Martin-Martinez, R. O'Connor, B.J. O'Sullivan, G. Groeseneken, Proc. IRPS (2008) 20–27.
[10] T. Nagumo, K. Takeuchi, T. Hase, Y. Hayashi, Proc. IEDM (2010) 628–631.
[11] A. Ghetti, C.M. Compagnoni, A.S. Spinelli, A. Visconti, IEEE Trans. Electron. Dev. 56 (8) (2009) 1746–1752.