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Oxide Defects: From Microscopic Physics to Compact Models

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An electronic version of this presentation containing all animations is available at
http://www.iue.tuwien.ac.at/pdf/ib_2011/SISPAD_Grasser_2011.pdf

Idealized Reliability Mechanisms

In order to characterize degradation, stress is accelerated
Idealized stress conditions are defined

Time-dependent dielectric breakdown (TDDB)

Very large gate voltages \Rightarrow oxide loses insulating property

Bias temperature instability (BTI)

S/D grounded, elevated temperature

pMOS: $-V_G \Rightarrow$ NBTI

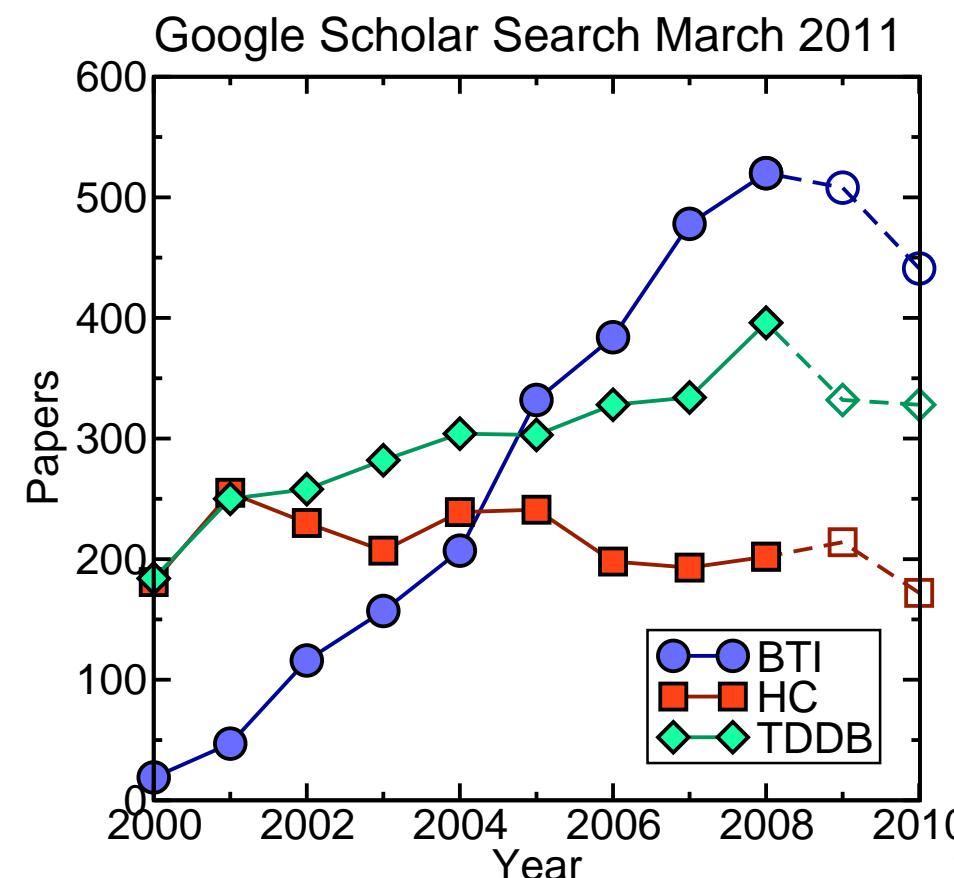
nMOS: $+V_G \Rightarrow$ PBTI (mostly high- κ)

Hot carrier (HC) degradation

Current flow between S/D

Circuit:

All of the above in a mixed form!



Time Dependent Dielectric Breakdown

Very large voltages applied to the gate

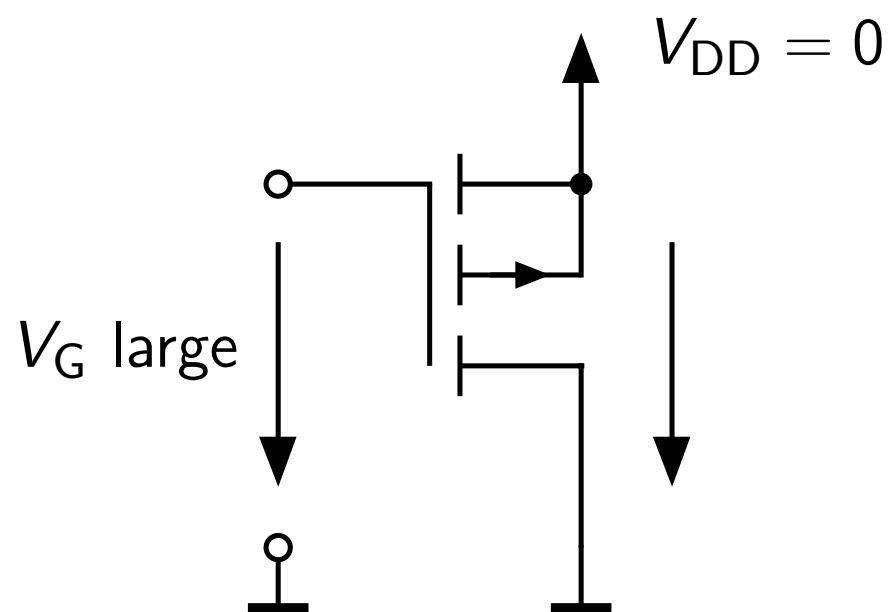
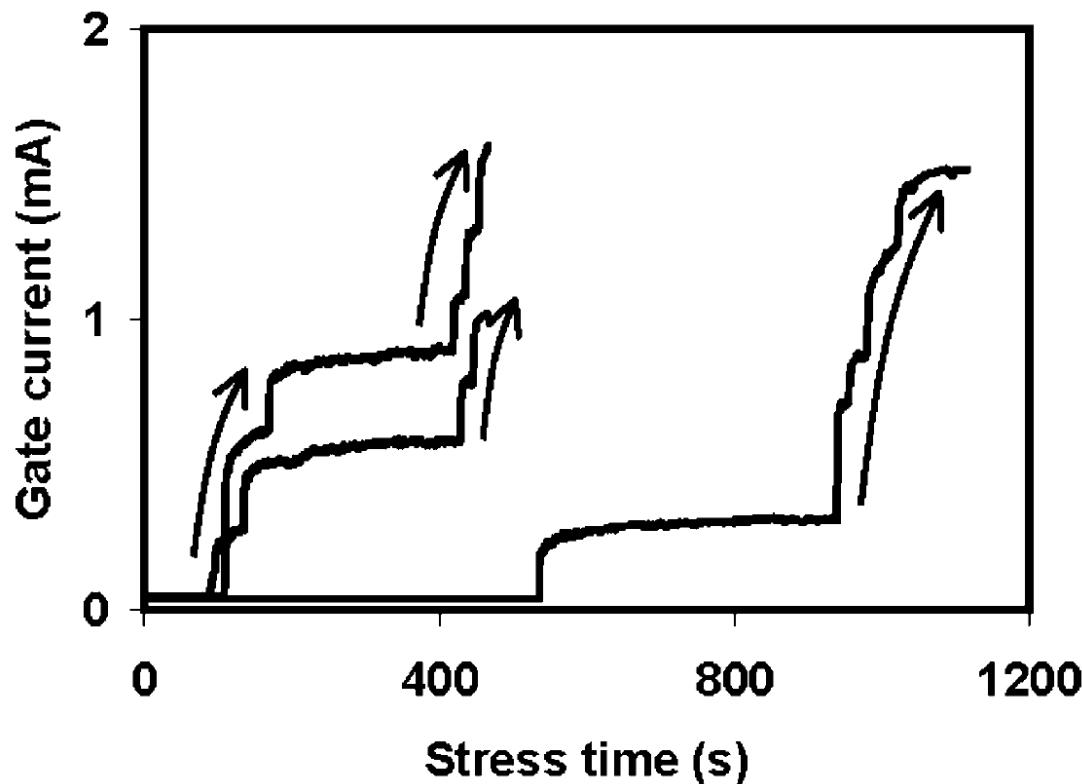
Larger than about 10 MV/cm

All other terminals grounded

Cause of degradation: creation of defects (conducting paths in the oxide)

Oxide loses insulating property

Soft and hard breakdowns



The Negative Bias Temperature Instability

Large negative voltage applied to the gate of a PMOS (NBTI)

Larger than about 4 MV/cm

All other terminals grounded

Elevated temperatures (NBTI)

Typically 125 °C

Cause of degradation: oxide charges and defects

Drift of V_{th} , g_m , etc.

Degradation occurs in all four configurations

NMOS/PMOS

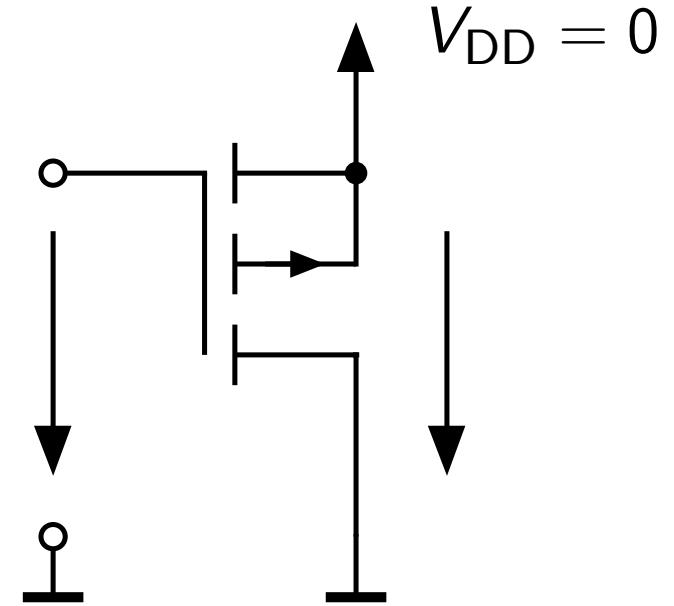
Negative and positive stress voltages

NBTI in PMOS most important

In high-k NMOSFETs, PBTI equally important

Note:

Degradation occurs also at room temperature and voltages slightly larger than V_{th}



Hot Carrier Degradation

Voltages applied to both gate and drain

Like BTI, but with current flow from S/D

Carriers become ‘hot’ as they traverse the channel

Excess energy can create defects at drain side

Cause of degradation: oxide charges and defects

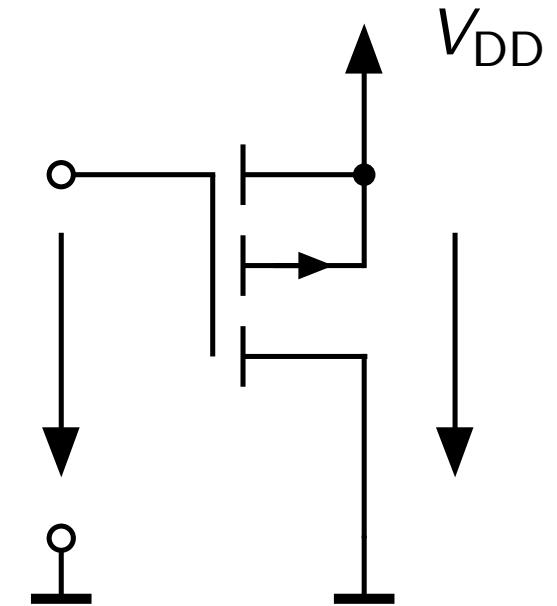
Drift of V_{th} , g_m , etc.

Very similar to BTI, except:

Inhomogeneous degradation at the drain side

Degradation does not recover that well

Degradation typ. becomes weaker with increasing T



NBTI vs. HCI Degradation

In a circuit NBTI and HCI degradation can occur simultaneously

Separation using modified ring-oscillators^[1]

Feedback interruptible by control circuitry

Allows separation of BTI and HCI

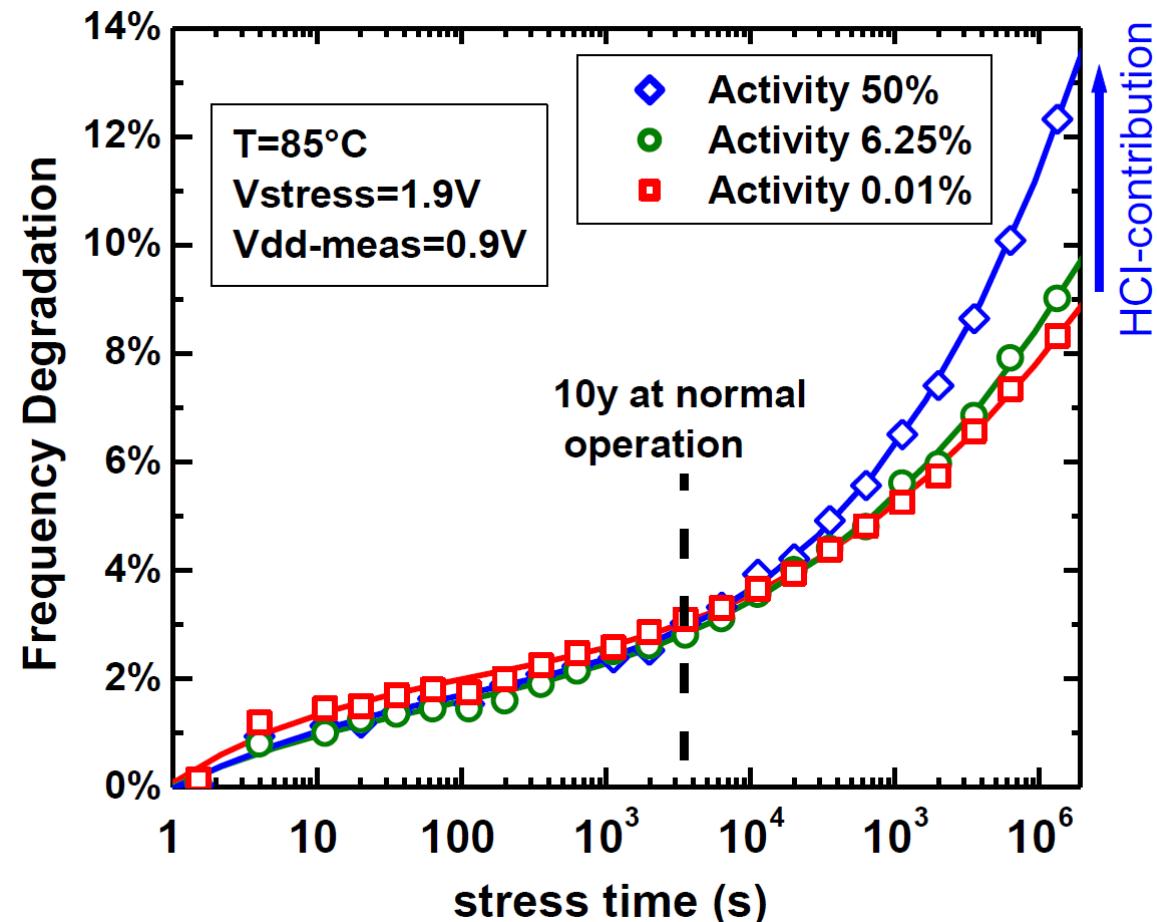
Activity 50%: BTI + HCI

Activity 0.01%: Almost static BTI

At normal operating conditions

Degradation NBTI dominated

At least for combinatorial logic



[1] Hofmann et al., VLSI Symp. '10

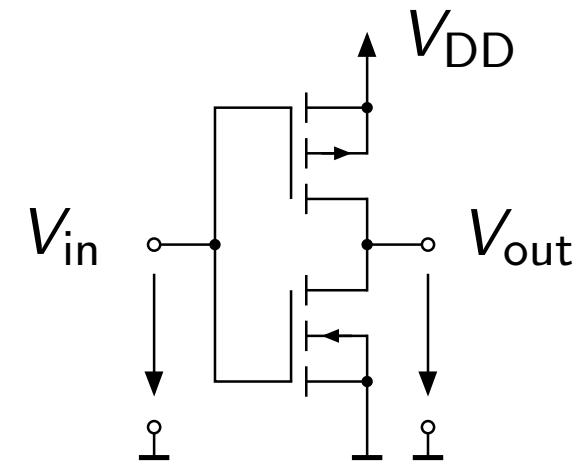
The Negative Bias Temperature Instability

When does the NBTI scenario occur?

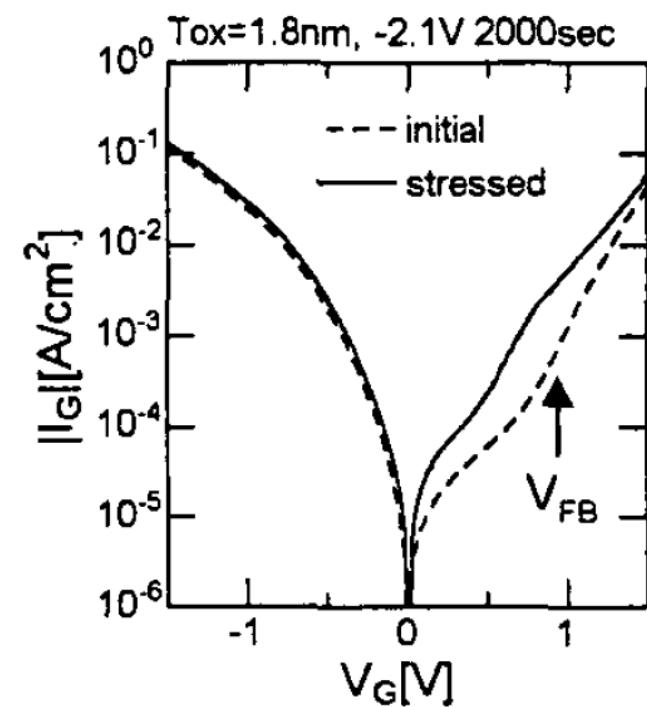
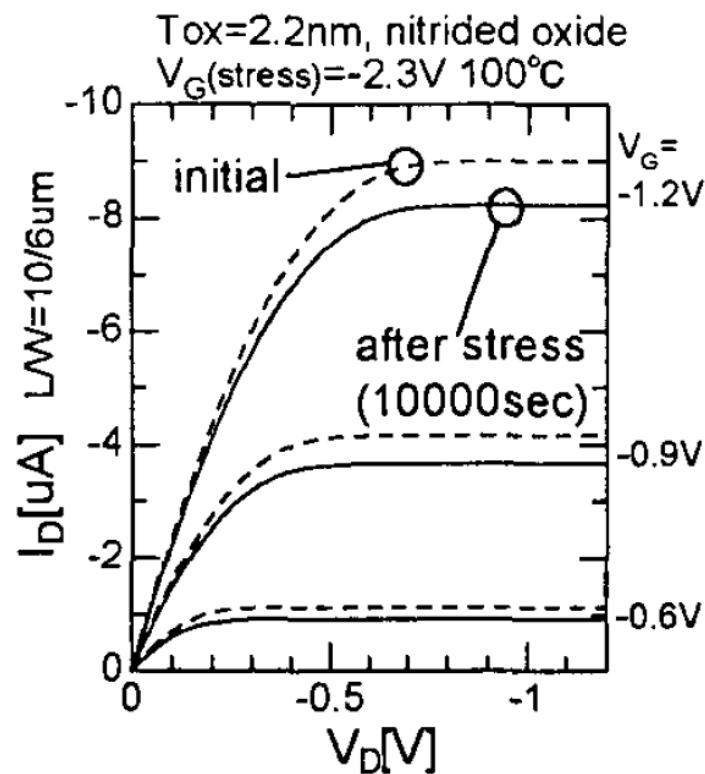
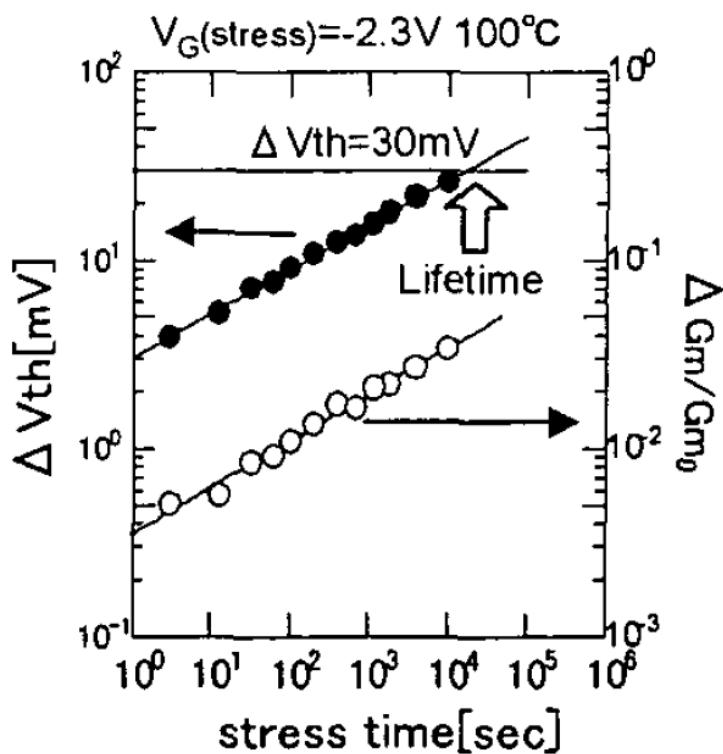
NBTI: $V_G \ll 0\text{ V}$, $V_S = V_D = 0\text{ V}$

Example: inverter with $V_{in} = 0\text{ V}$

Similar scenarios in ring-oscillators, SRAM cells, etc.



What happens to the pMOS transistor?



Introduction

Stochastic NBTI on small-area devices: link NBTI and RTN

Physical defect modeling

Temperature- and bias-dependence

Anomalous defect behavior

Time-dependent variability

Reliability make variability time-dependent

Circuit model

How to approximate the essence for circuit simulation

Experimental support

Wide distribution of capture and emission times

Conclusions

Conventional NBTI Model

Most popularized model for NBTI

Reaction-diffusion theory [1] [2] [3] [4]

Stress

Si–H breaks

Creation of Si–•

H diffuses away

2 H form H₂

H₂ diffusion controls kinetics

Recovery

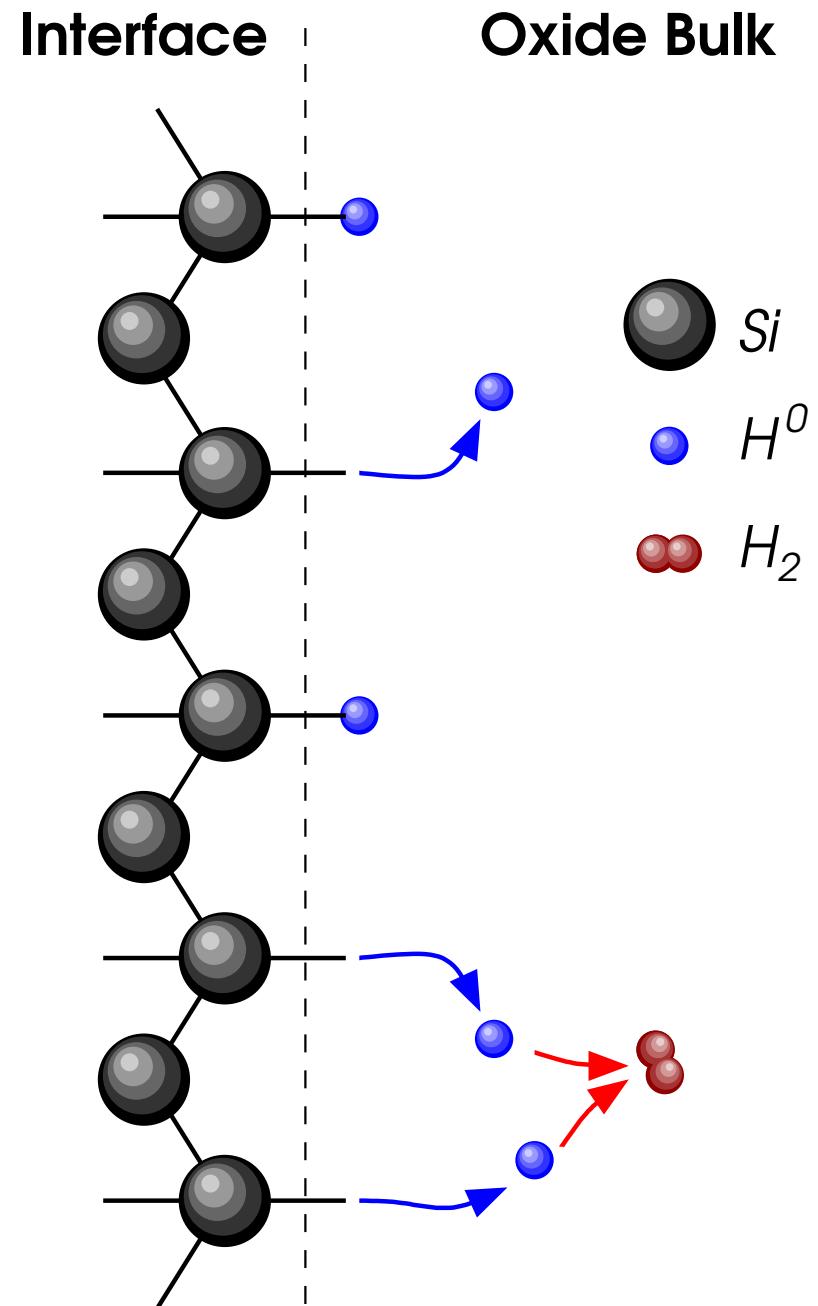
H₂ repassivates Si–•

H₂ back-diffusion controls kinetics

Hole trapping

Obscures data up to 1 s

Has to be ‘subtracted’



[1] Jeppson and Svensson, JAP '77

[2] Alam, IEDM '03

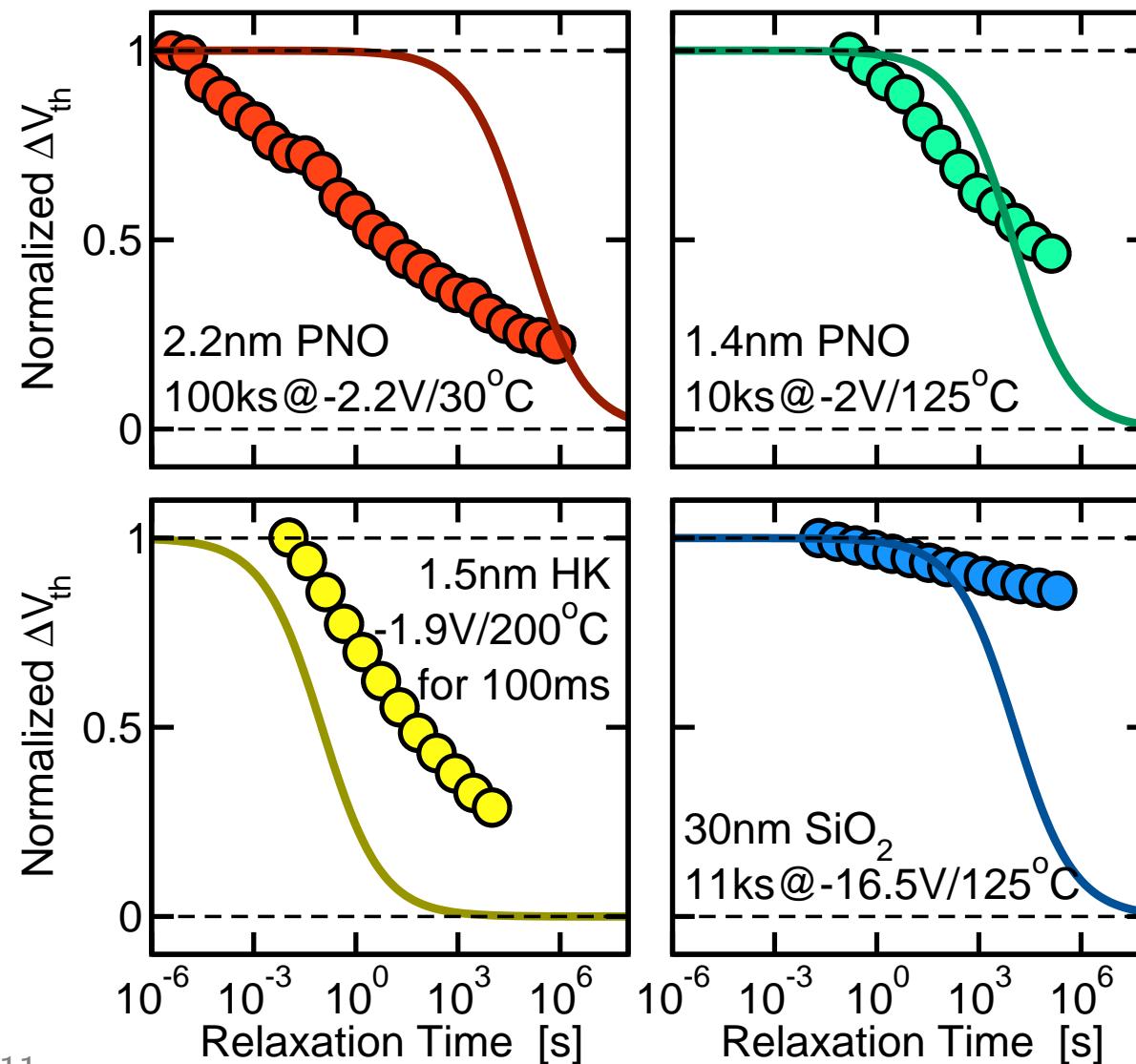
[3] Islam *et al.*, IEEE T-ED '07

[4] Grasser *et al.*, IEEE T-DMR '08

Conventional NBTI Model

Reaction-diffusion (RD) theory

Problem #1: cannot reproduce recovery [1] [2] [3] [4]



[1] Kaczer *et al.*, IRPS '05

[2] Grasser *et al.*, IRPS '07

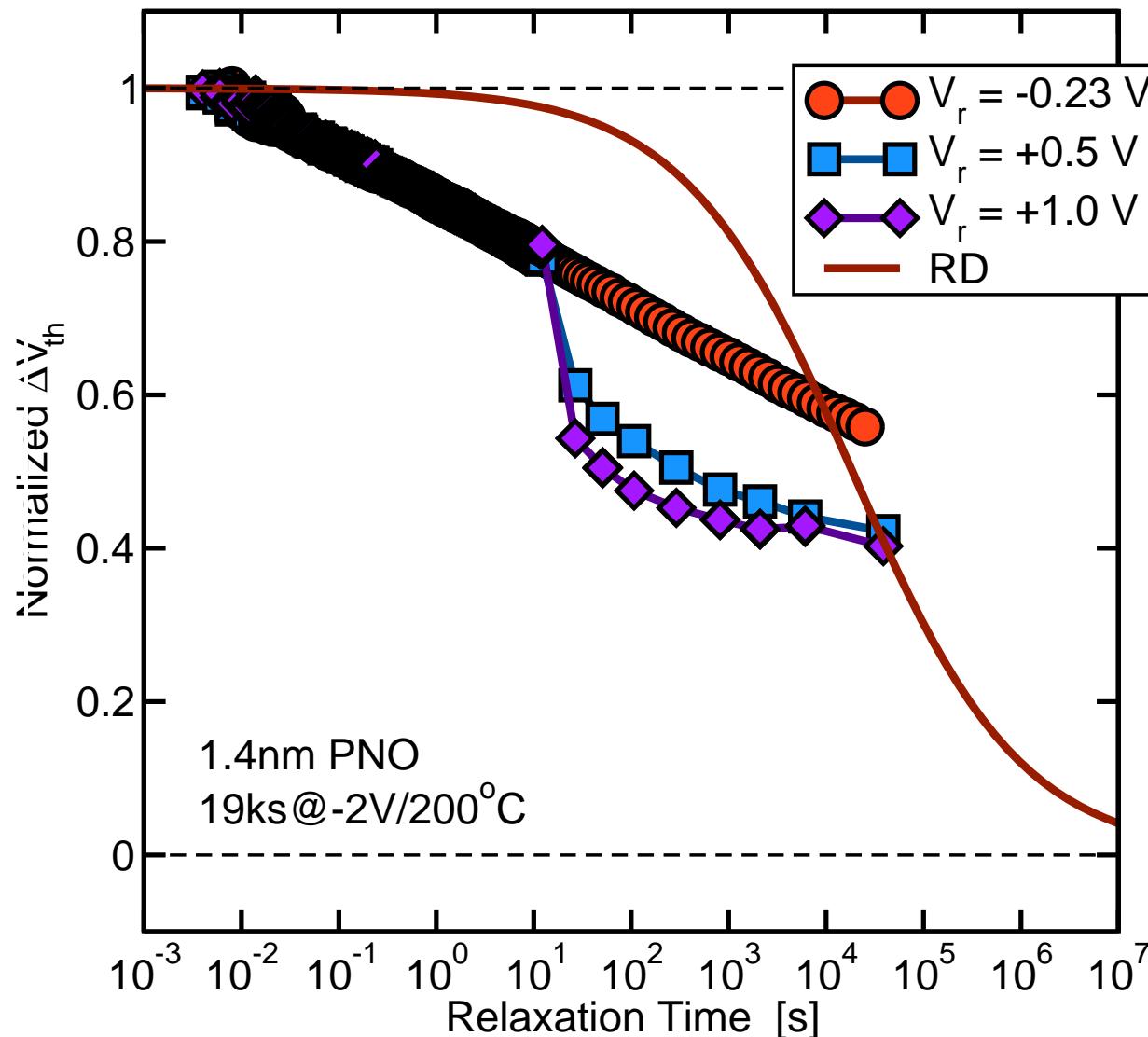
[3] Huard *et al.*, IEDM '07

[4] Grasser *et al.*, IEEE T-ED '11

Conventional NBTI Model

Reaction-diffusion (RD) theory

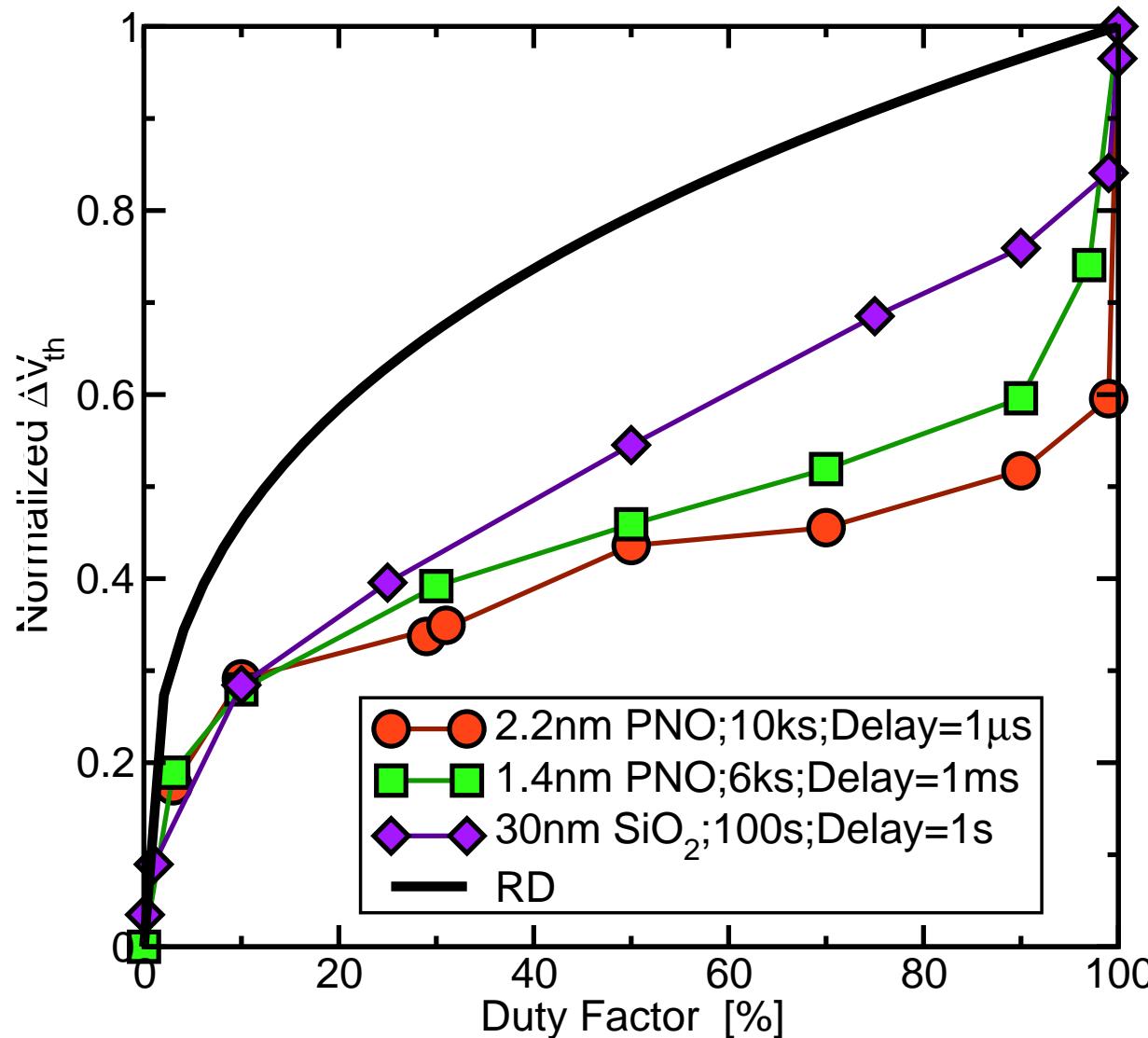
Problem #2: long-time recovery is due to back-diffusion of neutral H₂



Conventional NBTI Model

Reaction-diffusion (RD) theory

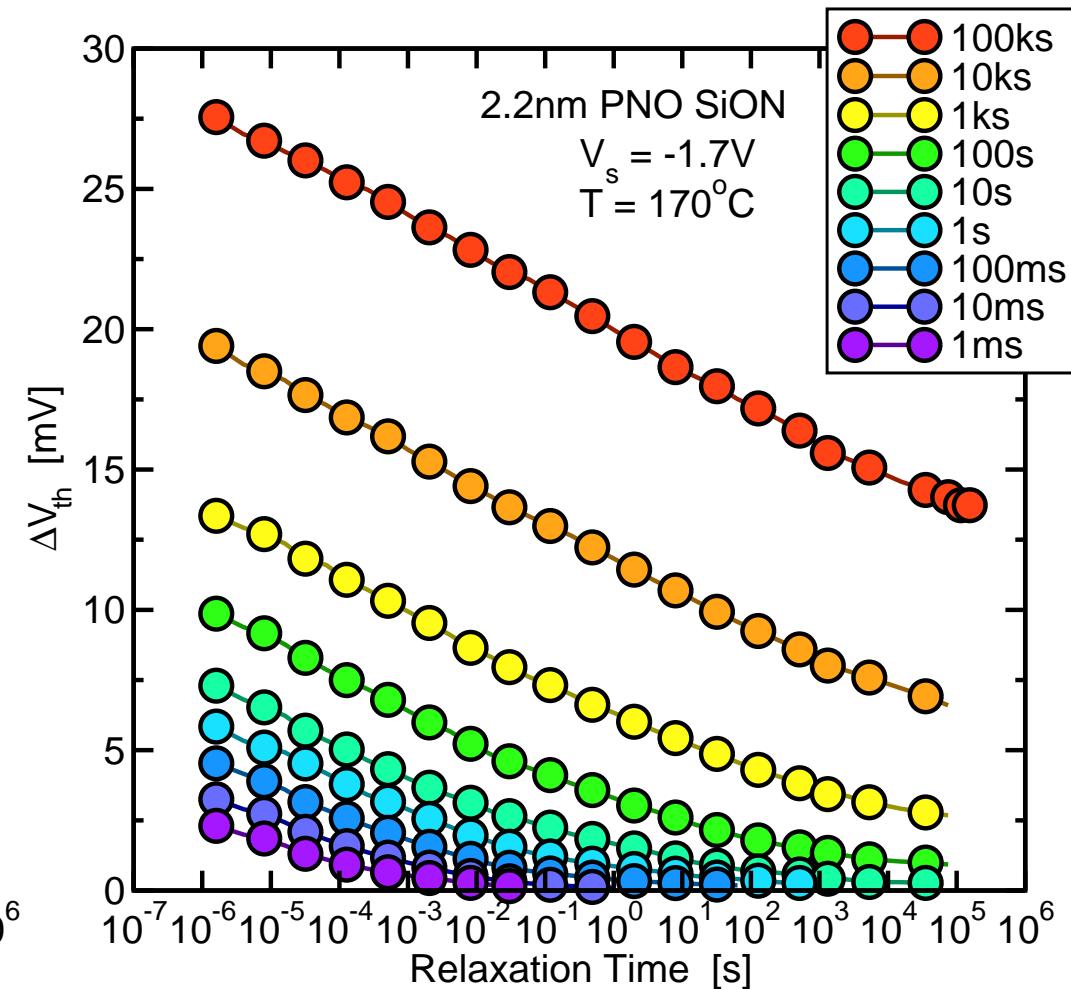
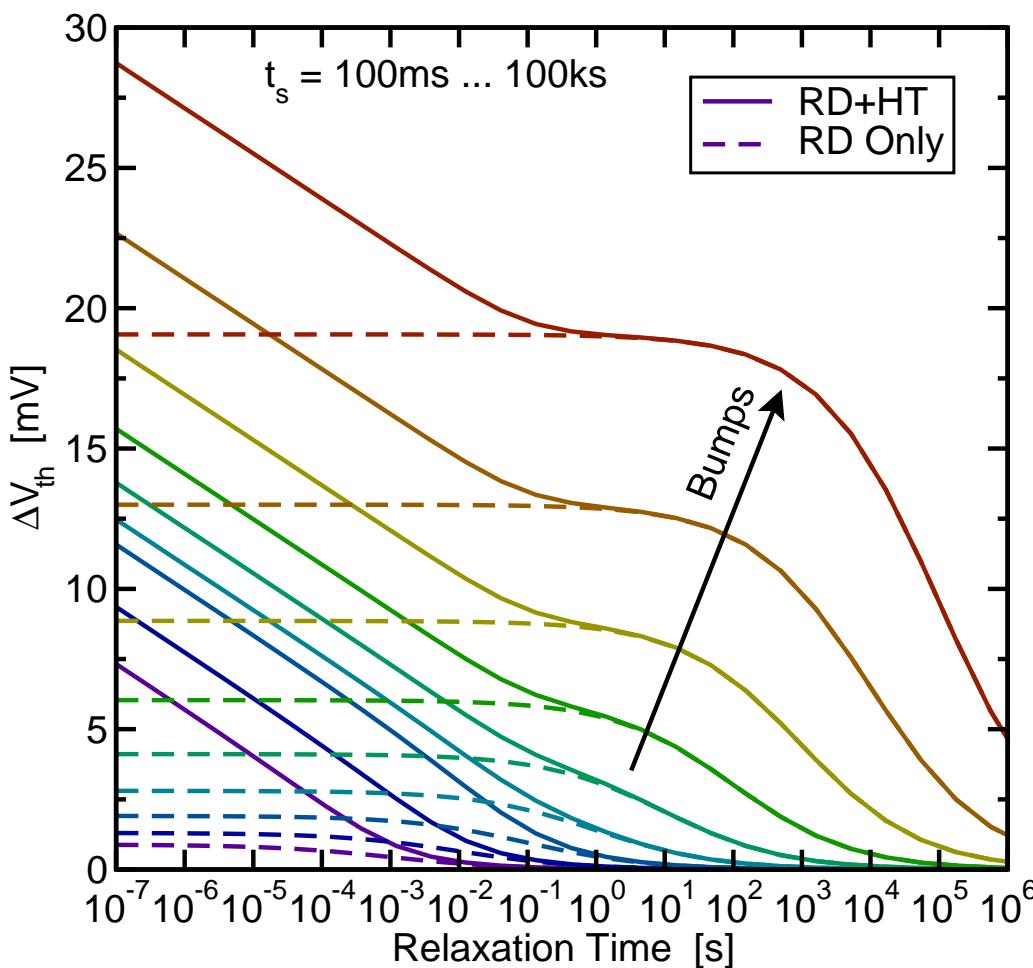
Problem #3: Duty-factor (DF) dependence nearly constant for DF $\rightarrow 100\%$



Conventional NBTI Model

Reaction-diffusion (RD) theory

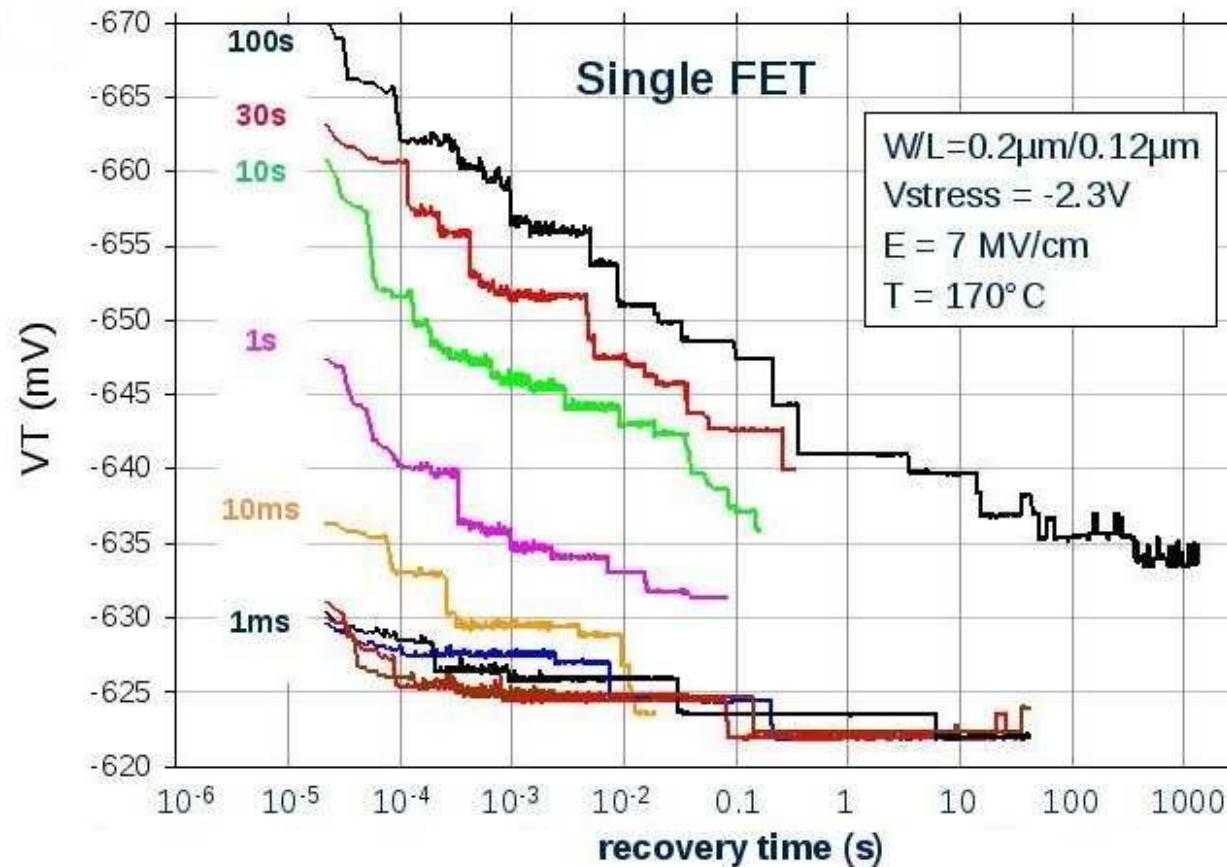
Problem #4: elastic hole trapping (HT) cannot fix recovery



What is Really Going On?

Study of NBTI recovery on small-area devices [1] [2] [3] [4] [5]

Stochastic and discrete charge emission events, no diffusion



- [1] Reisinger *et al.*, IIRW '09 [2] Grasser *et al.*, IEDM '09 [3] Kaczer *et al.*, IRPS '10 [4] Grasser *et al.*, IRPS '10
[5] Reisinger *et al.*, IRPS '10

Recoverable NBTI due to the same Defects as RTN

Quasi-equilibrium:

Some defects neutral, others positive, a few produce random telegraph noise (RTN)

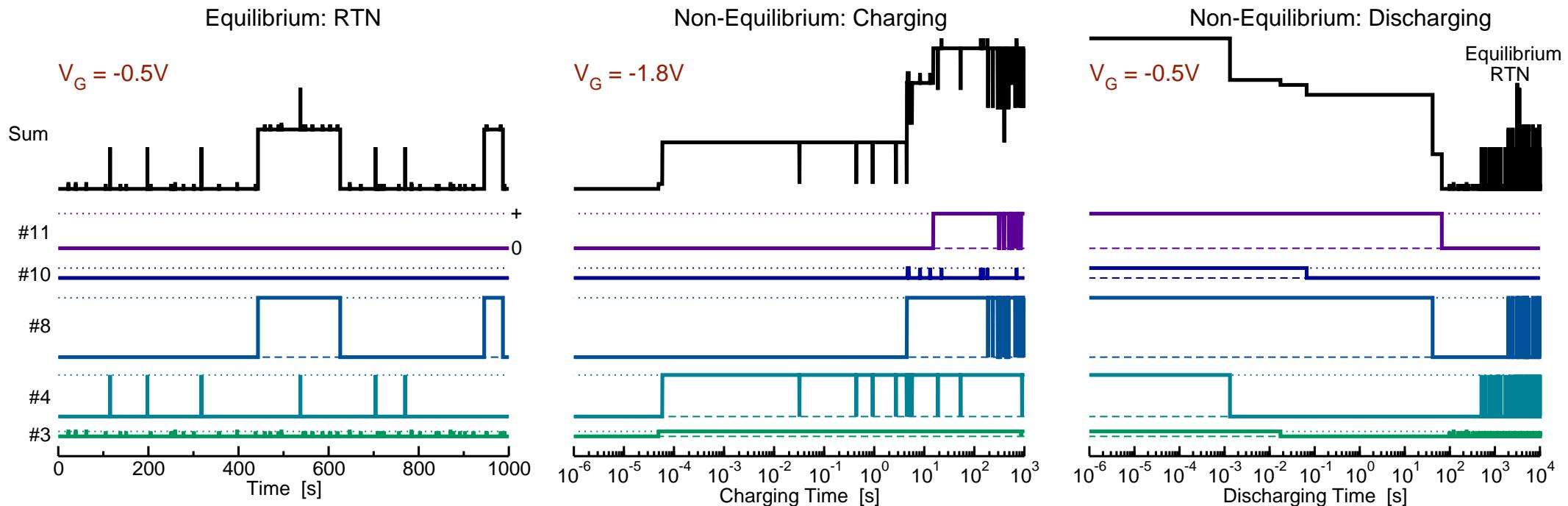
Stress:

Defects switch to new equilibrium (mostly positive), a few may produce RTN

Recovery:

Slow transition (broad distribution of timescales) to initial quasi-equilibrium

Analysis: time-dependent defect spectroscopy^{[1][2]}



[1] Grasser et al., IRPS '10

[2] Grasser et al., PRB '10

Charging of Oxide Defects

Conventional model

Elastic tunneling, results in a 'tunneling front' (1 nm in 10 ms)

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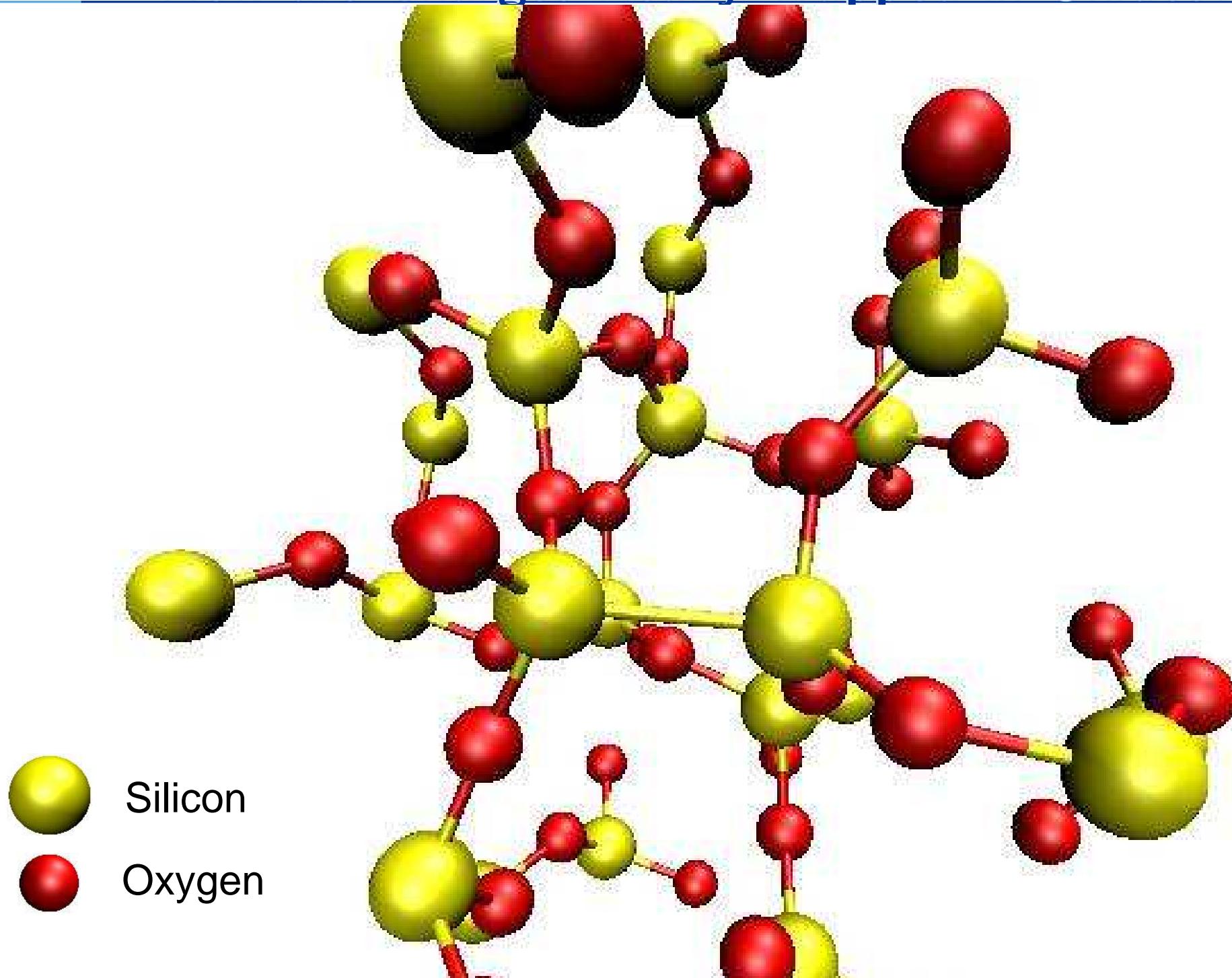
How to approximate the essence for circuit simulation

Experimental support

Wide distribution of capture and emission times

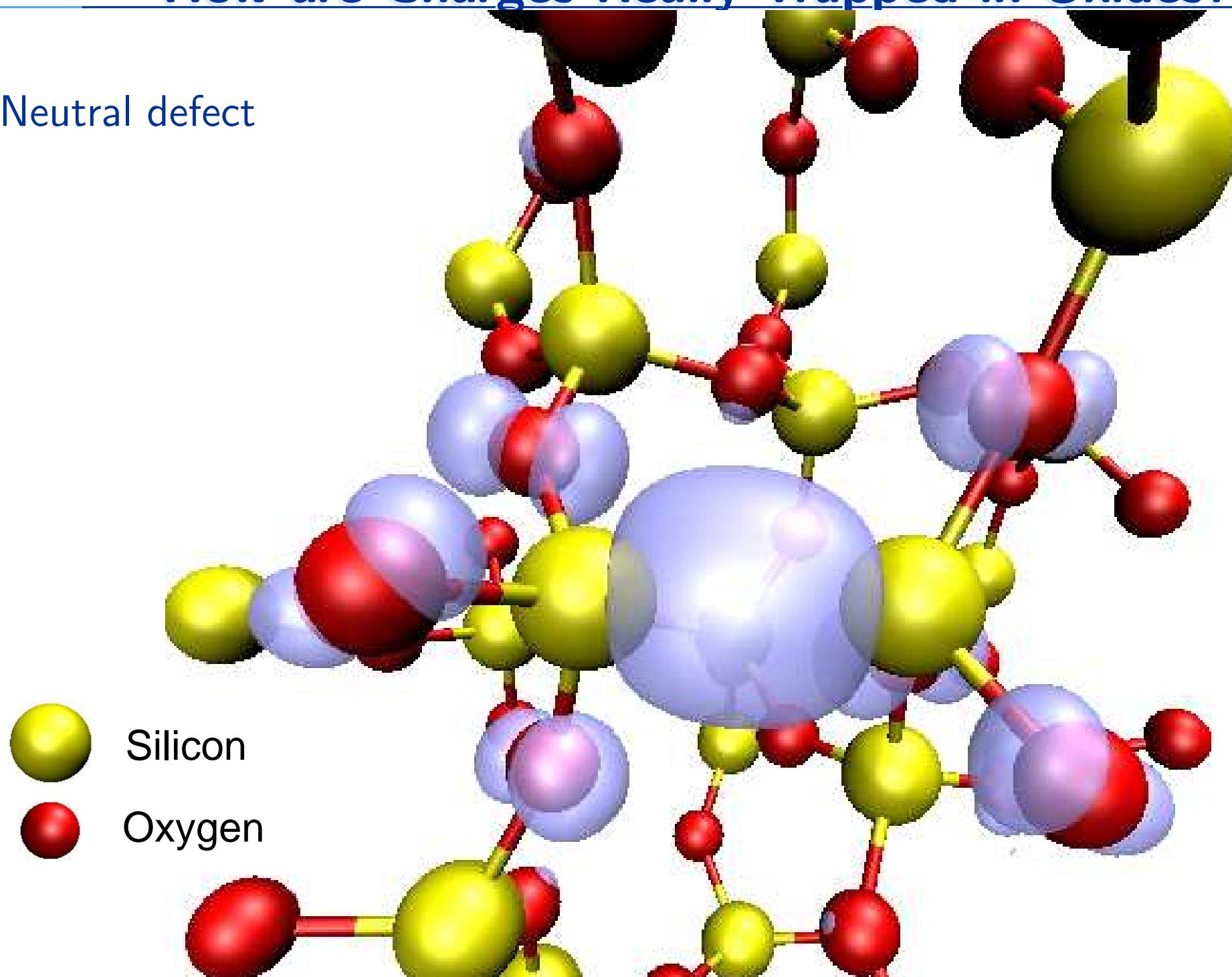
Conclusions

How are Charges Really Trapped in Oxides?



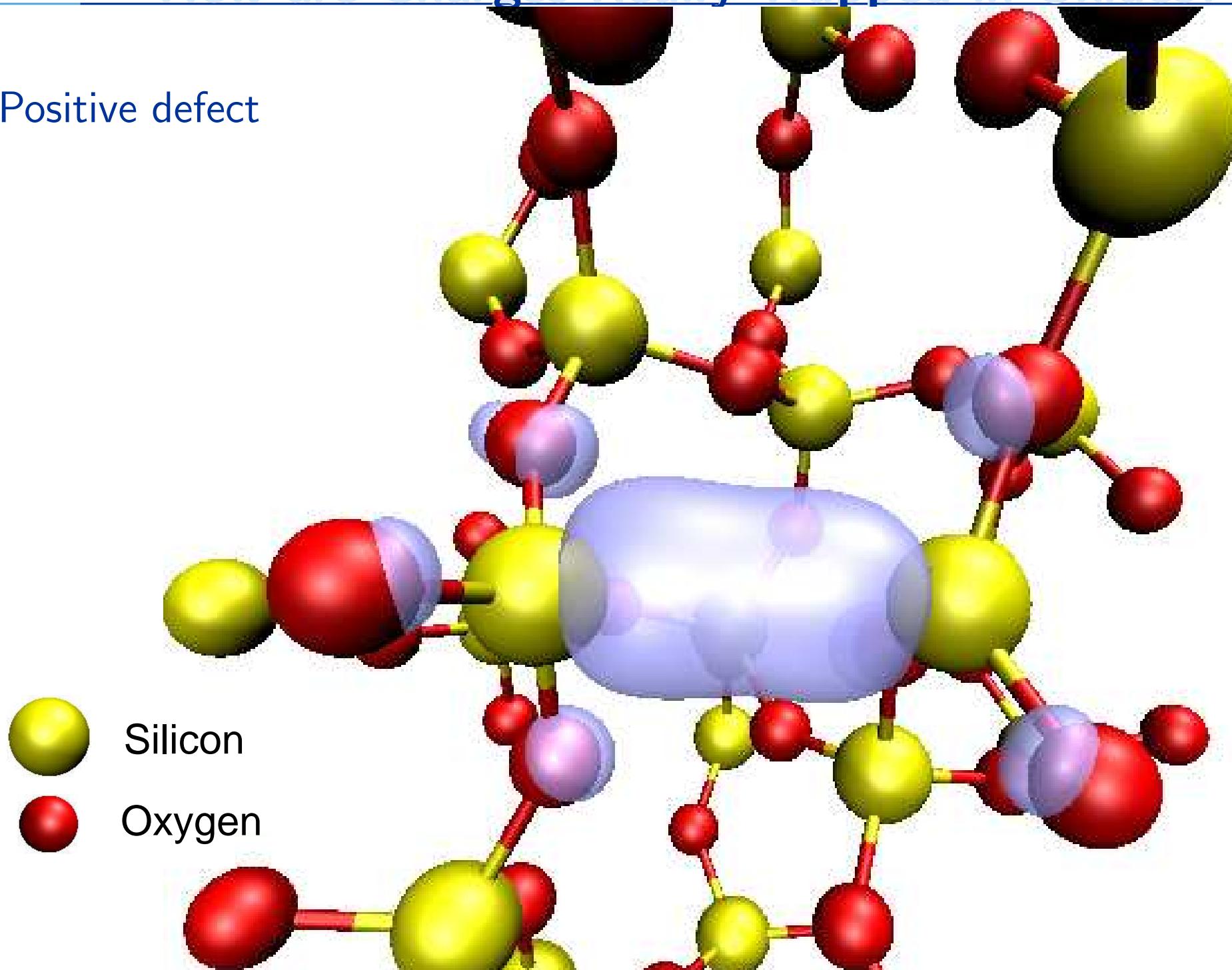
How are Charges Really Trapped in Oxides?

Neutral defect



How are Charges Really Trapped in Oxides?

Positive defect



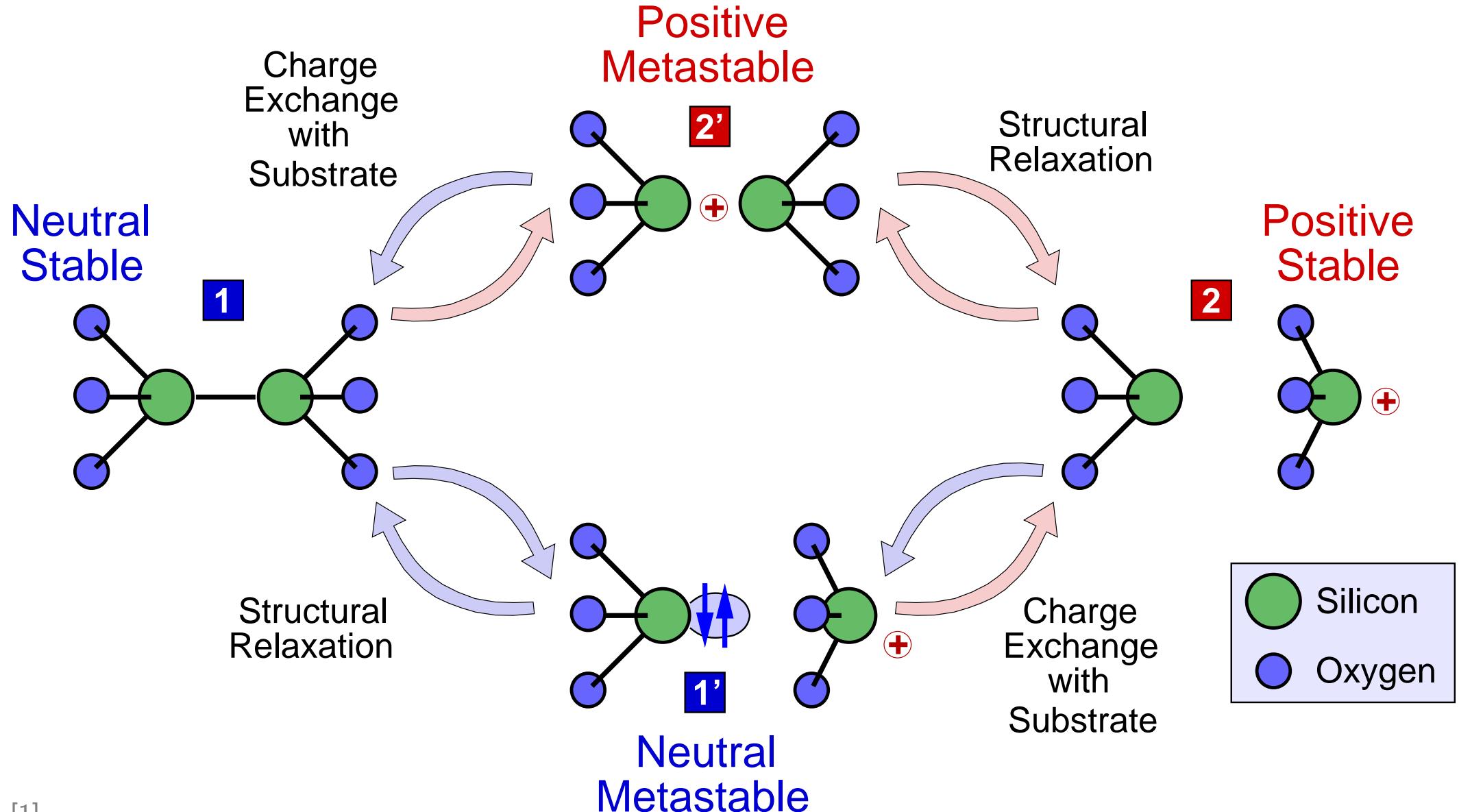
100 Femtoseconds in the Life of an E' center

Charging of an E' center

Puckering of an E' center

Detailed Defect Model Required

Defect has four states: neutral/positive, stable/metastable^[1]



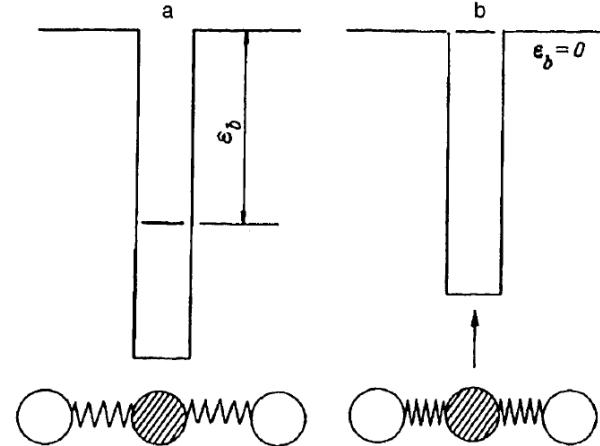
[1] Grasser et al., IRPS '10

Nonradiative Multiphonon Theory

Developed for F-centers and defects in III-V semiconductors^{[1][2]}

O in GaP, Fe and Cr in GaAs, etc.

Thermal vibrations modulate E_T



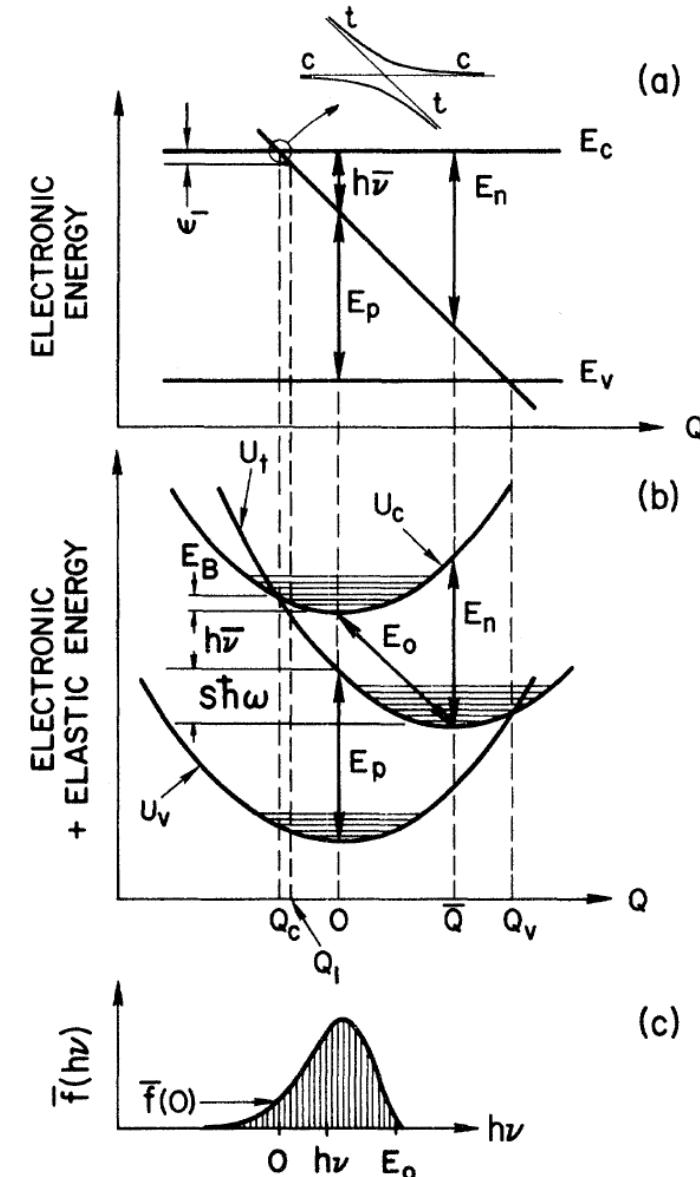
Total energy: vibrational plus electronic

Adiabatic approximation

Linear coupling: changes defect level

Quadratic coupling: changes in vibrational frequency

Explains optical energies



[1] Huang and Rhys, Proc.Roy.Soc.A 50

[2] Henry and Lang, PRB 77

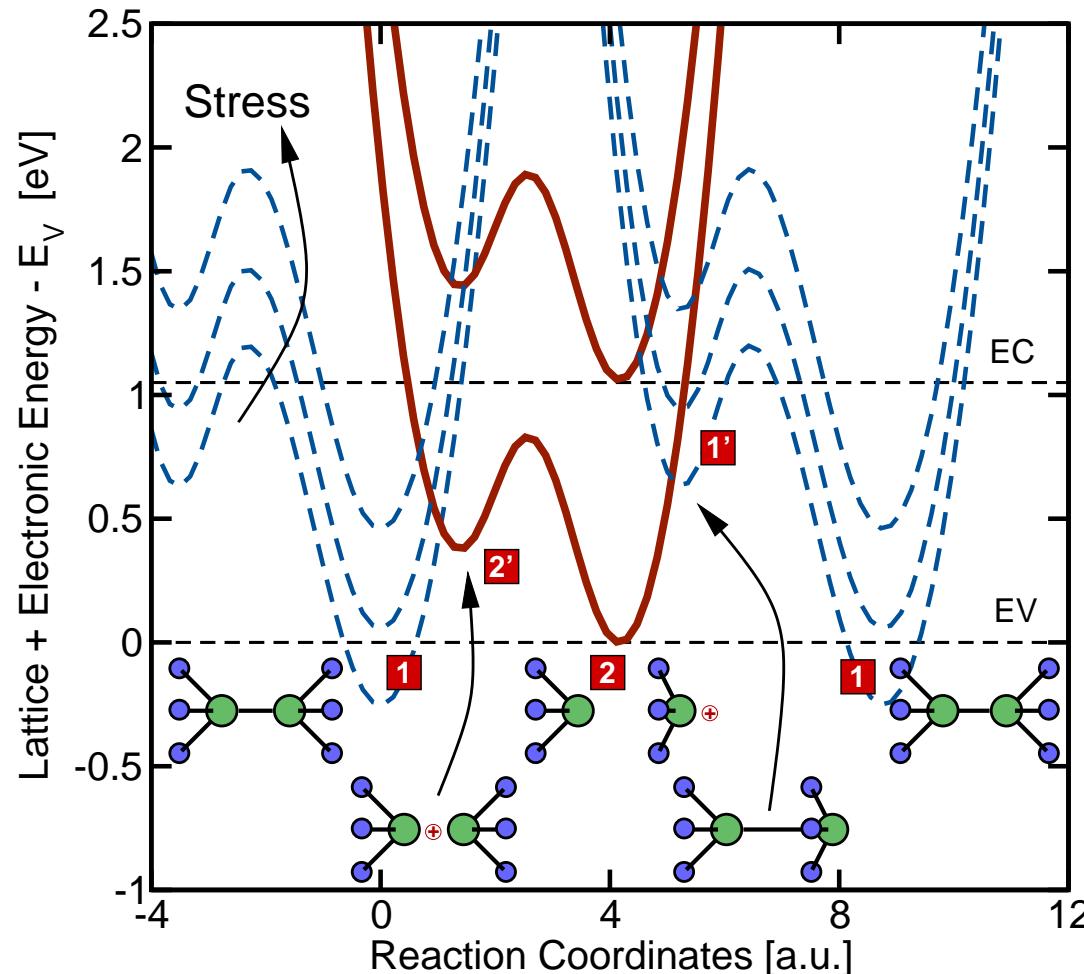
Model

Different adiabatic potentials for the neutral and positive defect

Metastable states $2'$ and $1'$ are secondary minima

Thermal transitions to ground states 1 and 2

Stochastic Markov-model for defect kinetics based on multiphonon theory



Charging of Oxide Defects

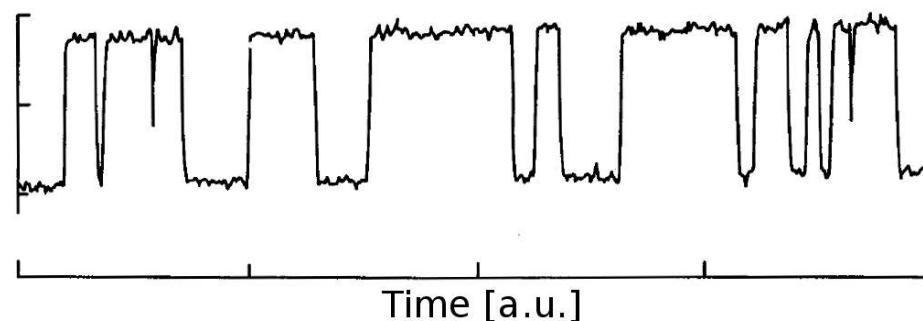
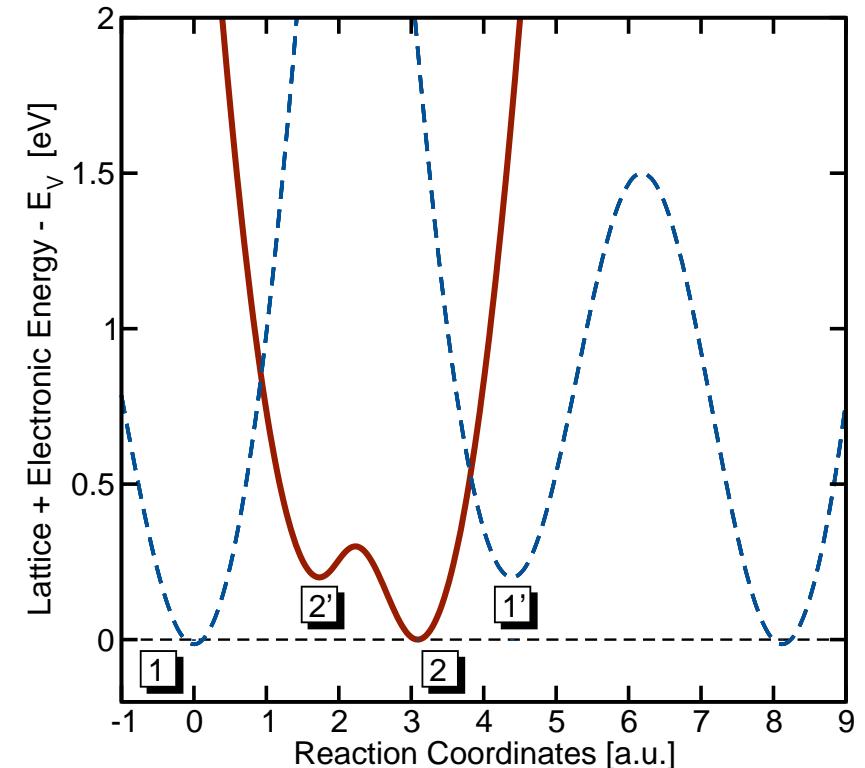
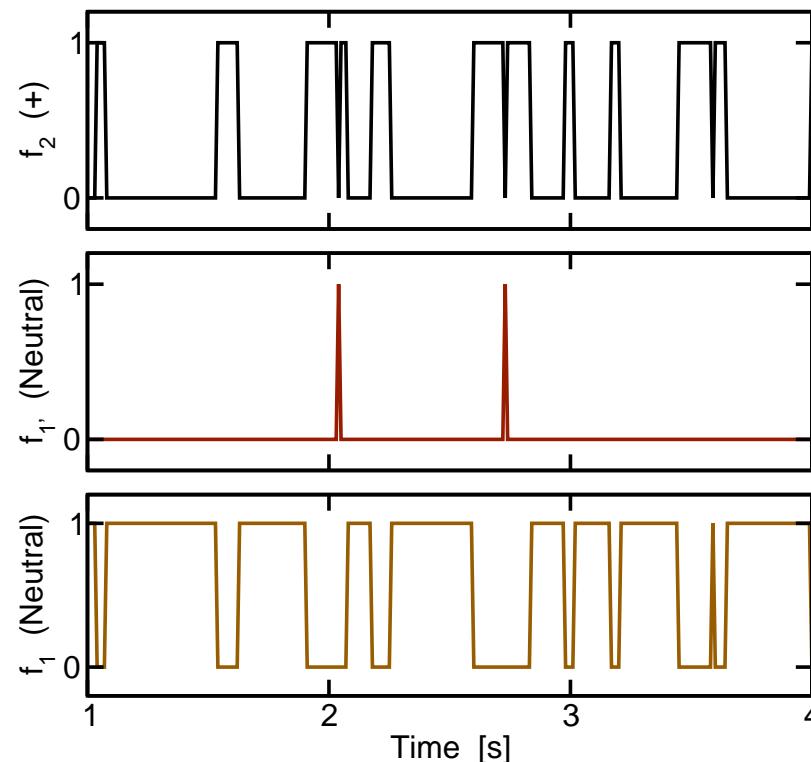
Nonradiative multiphonon model

Inelastic tunneling, no 'tunneling front'

Qualitative Model Evaluation

Normal random telegraph noise (RTN)

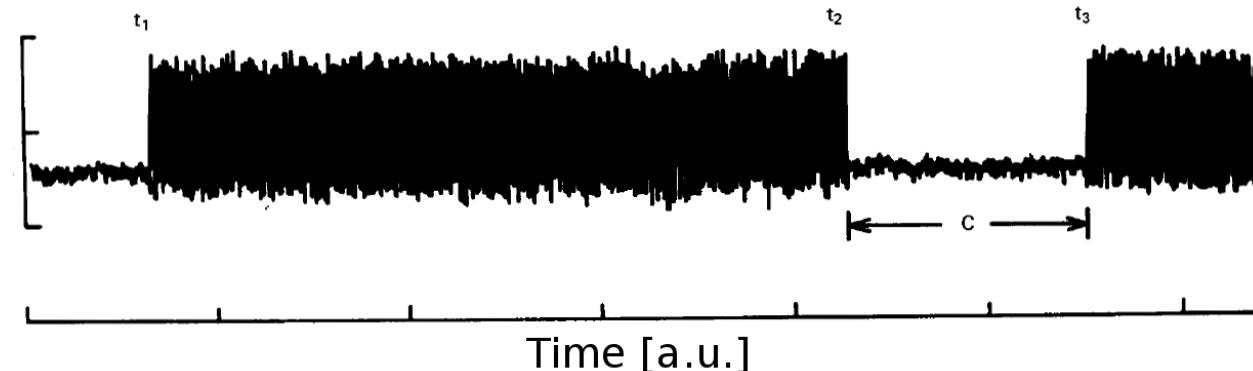
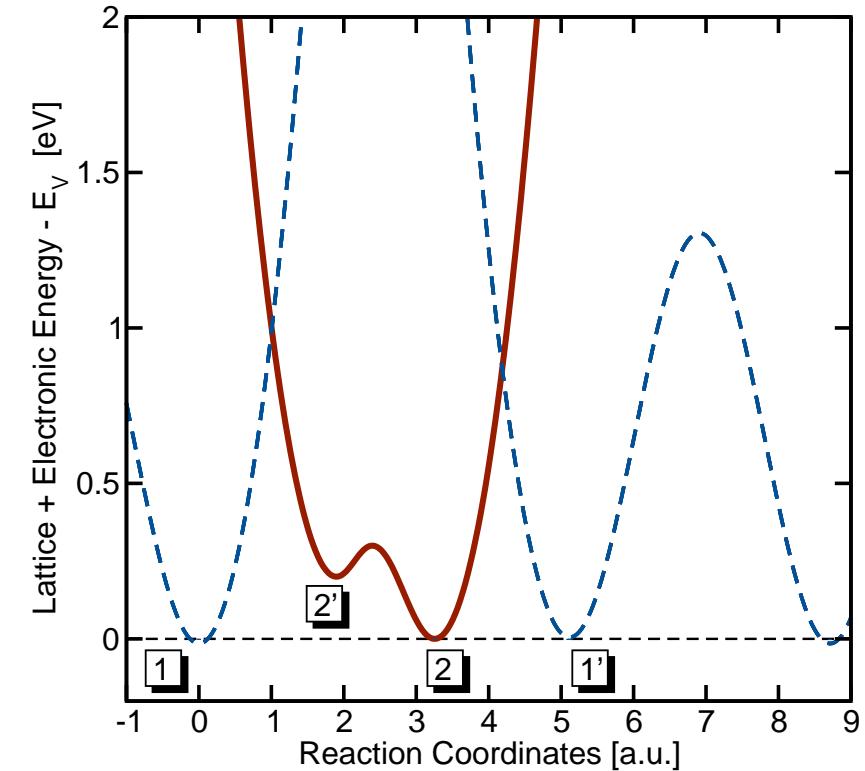
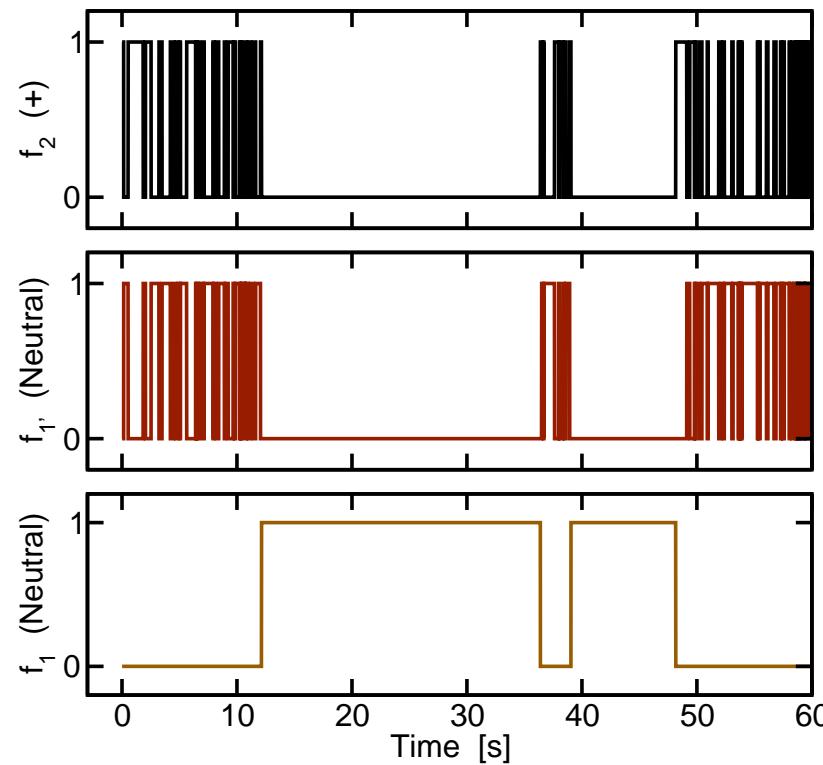
Very similar energetic position of the minimas 1 and 2



Qualitative Model Evaluation

Anomalous RTN

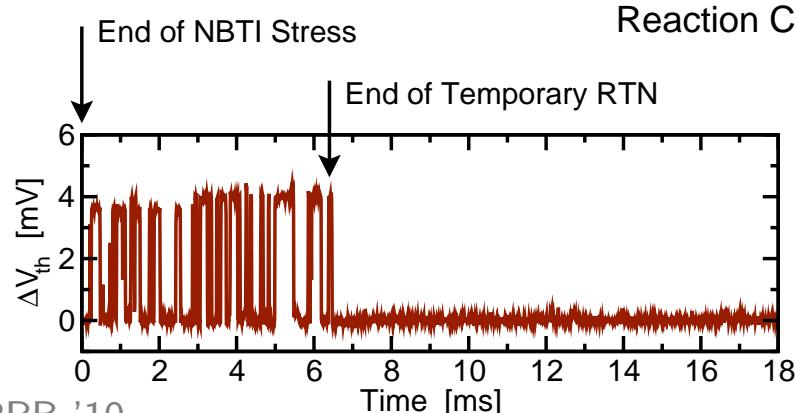
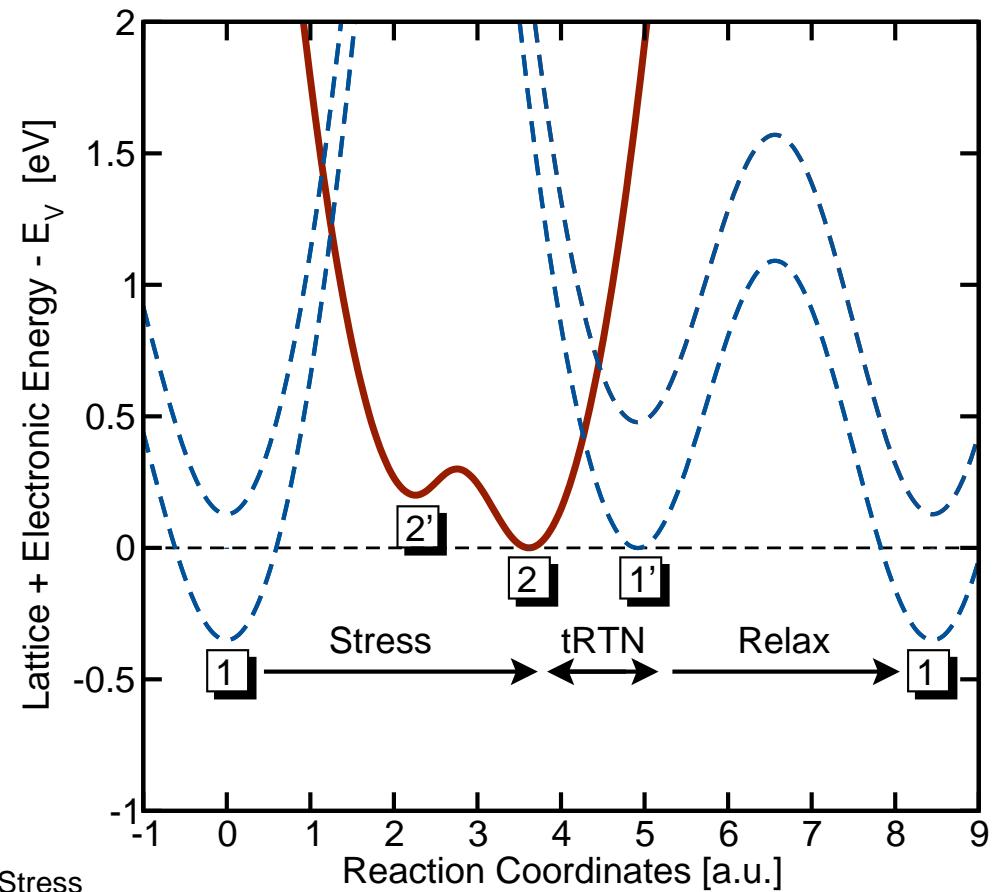
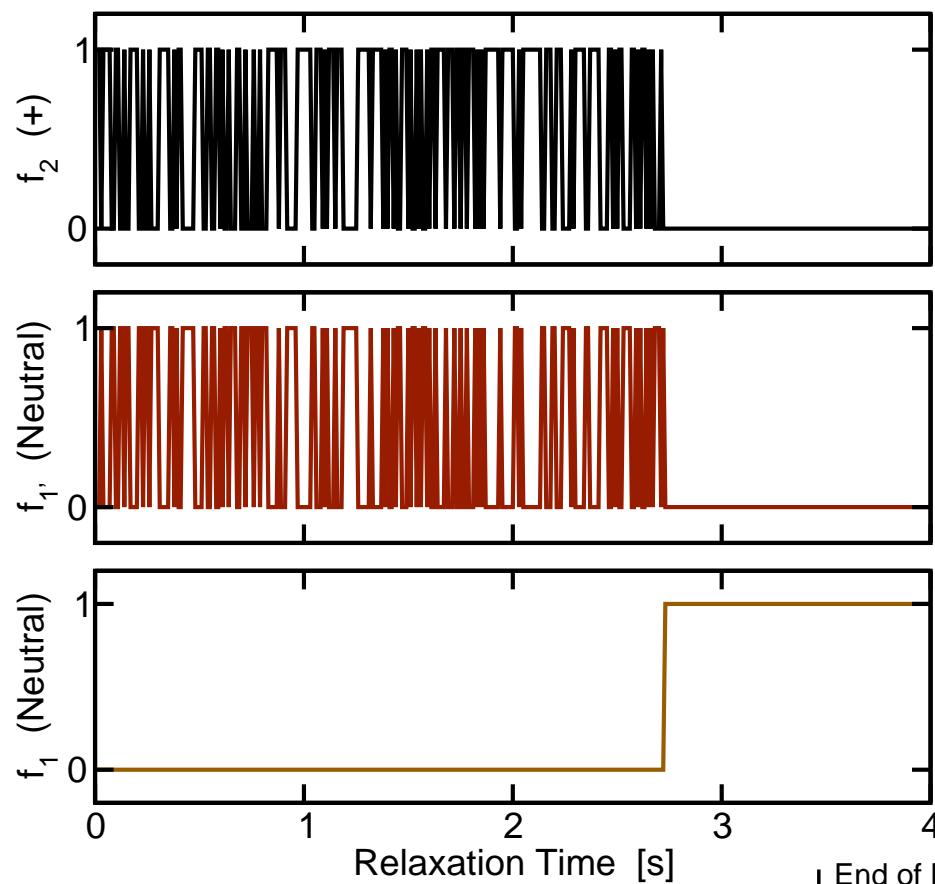
Very similar energetic position of the three minima 1, 2, and 1'



Uren et al., PRB '88

Qualitative Model Evaluation

Temporary random telegraph noise (tRTN)^{[1][2]}



Quantitative Model Evaluation

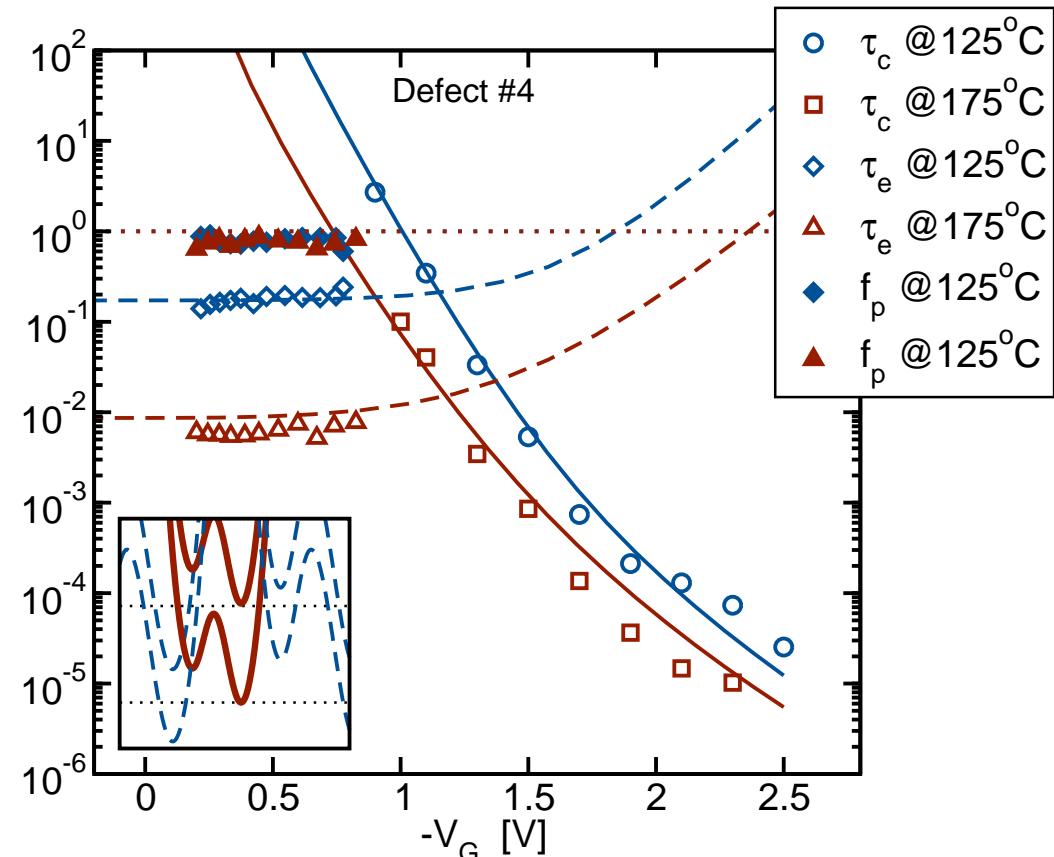
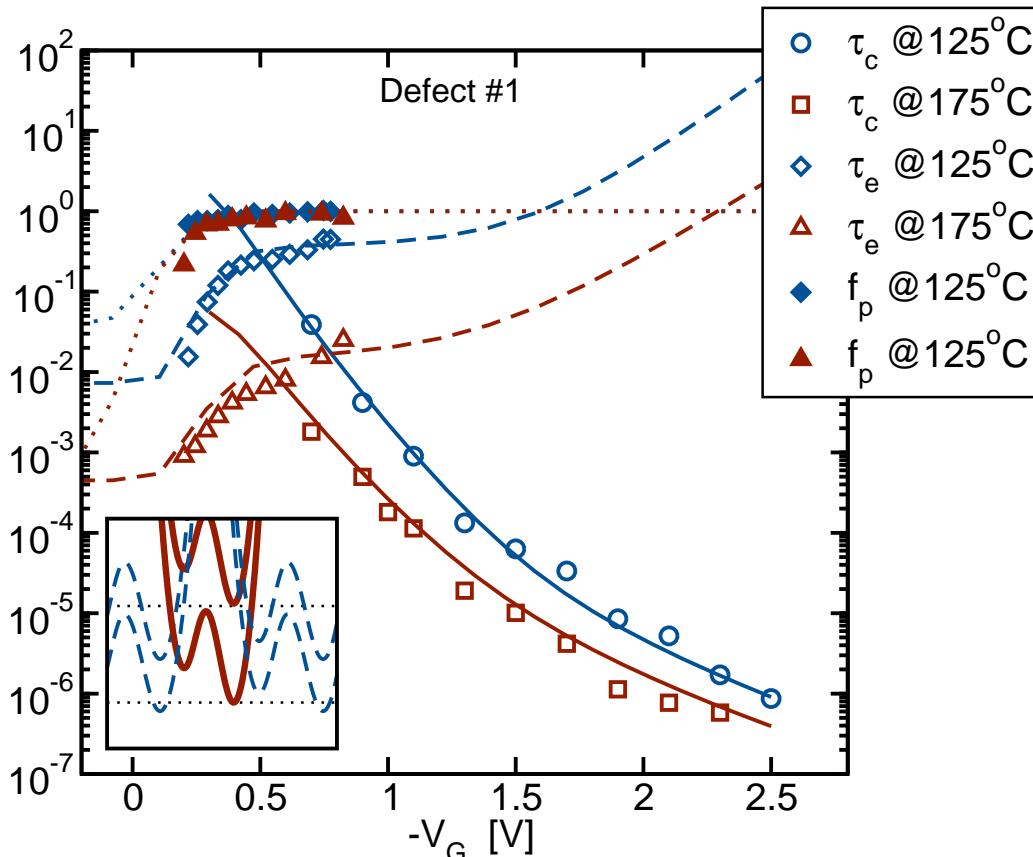
Excellent agreement for both capture and emission time constants

Experimentally extracted using the time-dependent defect spectroscopy (TDDS)^{[1][2]}

TDDS works over wide operation regime of the transistor

Does the defect act like a switching trap?

Depends on the defect configuration



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Wide distribution of capture and emission times

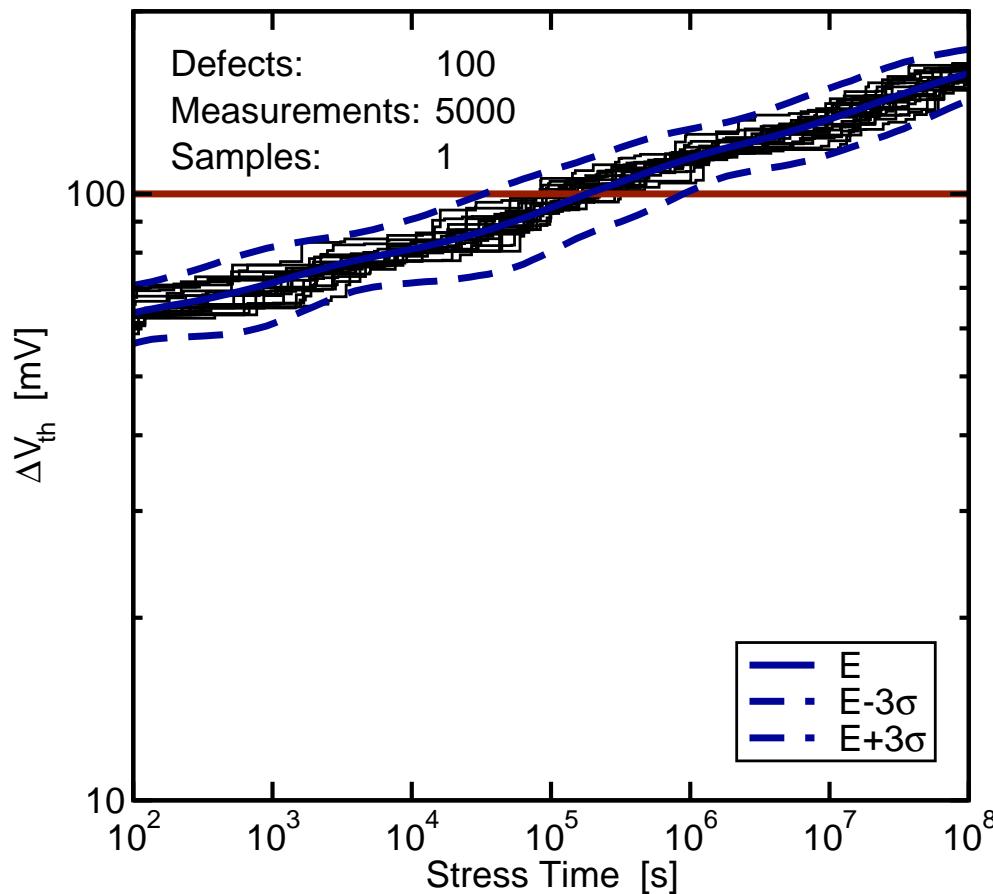
Conclusions

How to Determine the Lifetime?

Small area devices: lifetime is a stochastic quantity [1]

Charge capture/emission stochastic events

Capture and emission times distributed



$N_t = 10^{12} \text{ cm}^{-2}$; $W \times L = 100 \text{ nm} \times 100 \text{ nm} \Rightarrow 100 \text{ defects}$;

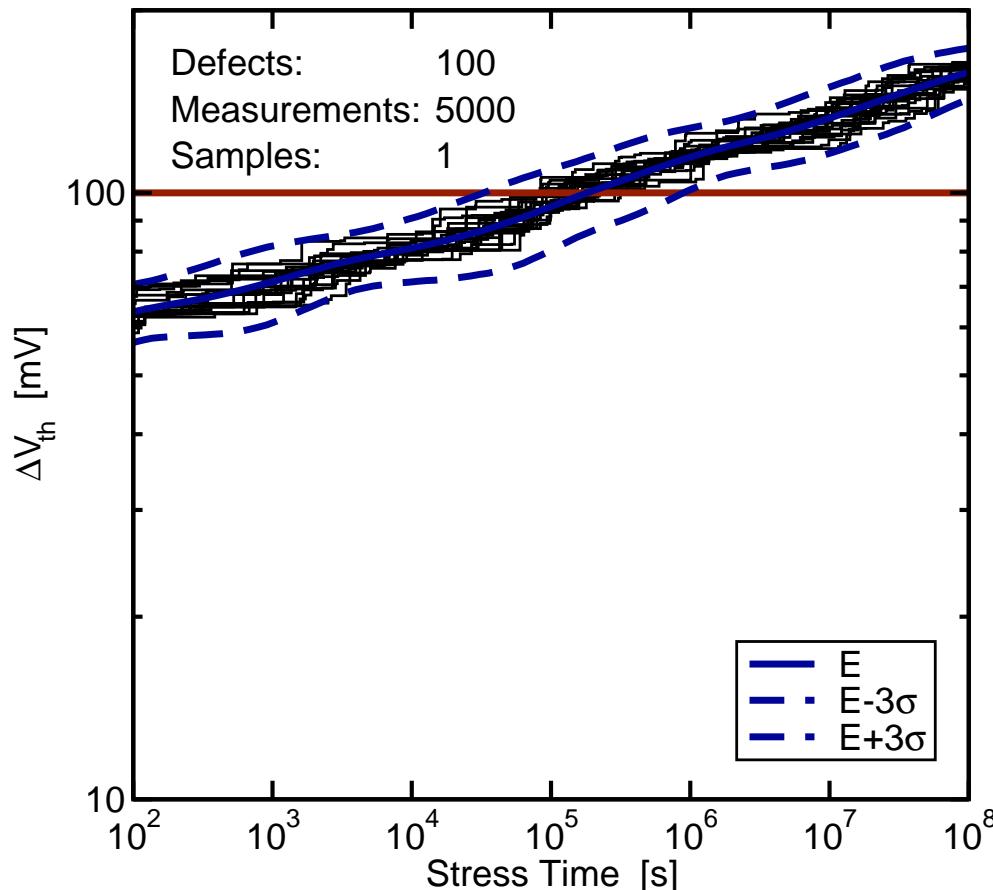
[1] Grassner et al. IEDM '10

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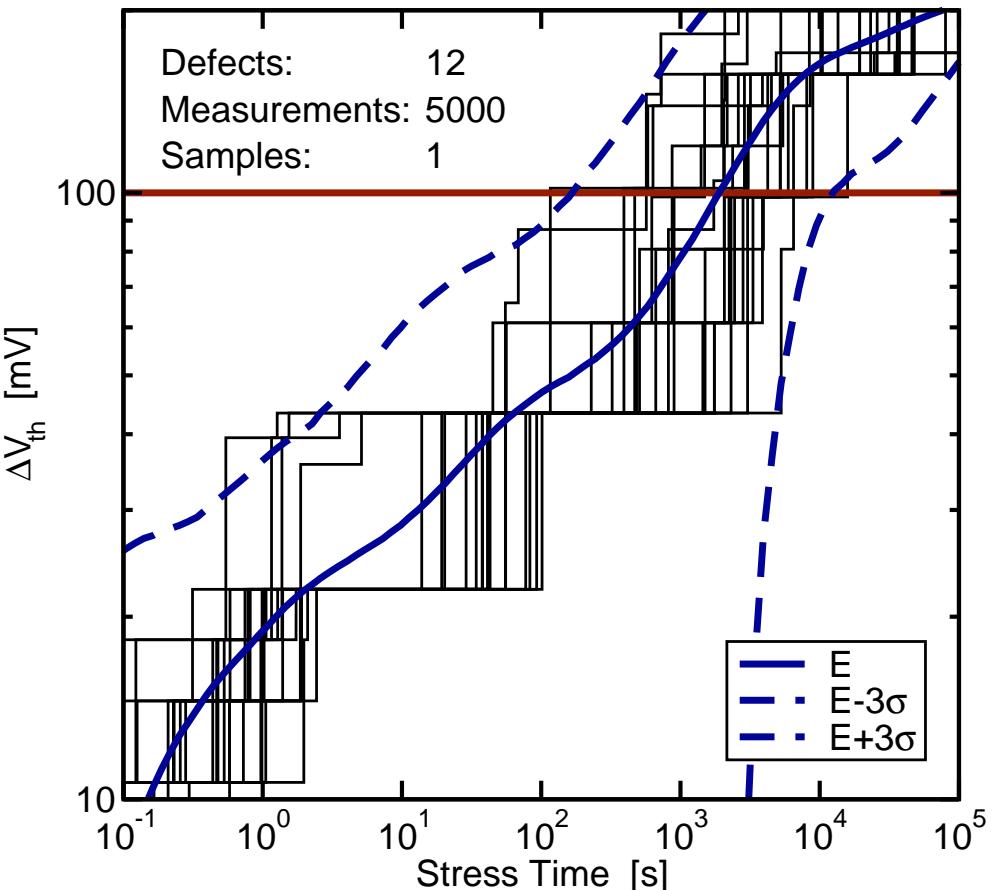
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$N_t = 10^{12} \text{ cm}^{-2}$; $W \times L = 100 \text{ nm} \times 100 \text{ nm} \Rightarrow 100 \text{ defects}$;



$35 \text{ nm} \times 35 \text{ nm} \Rightarrow 12 \text{ defects}$

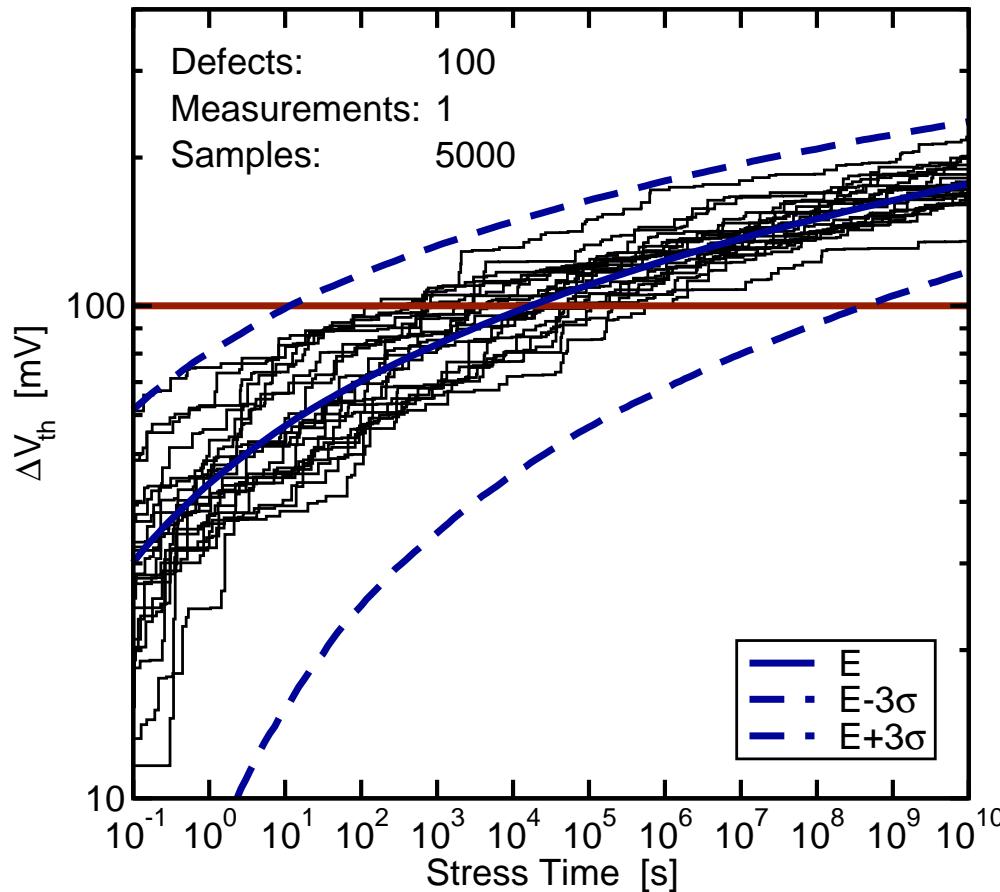
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[1] Grassner et al. IEDM '10

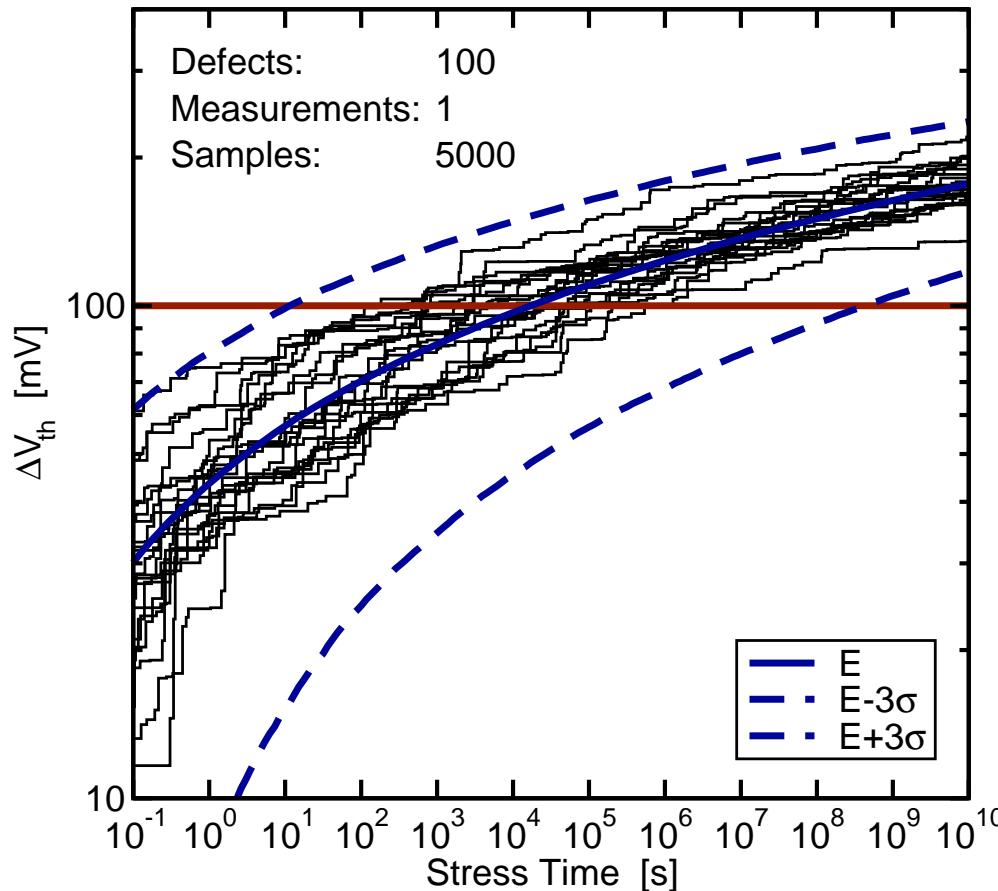
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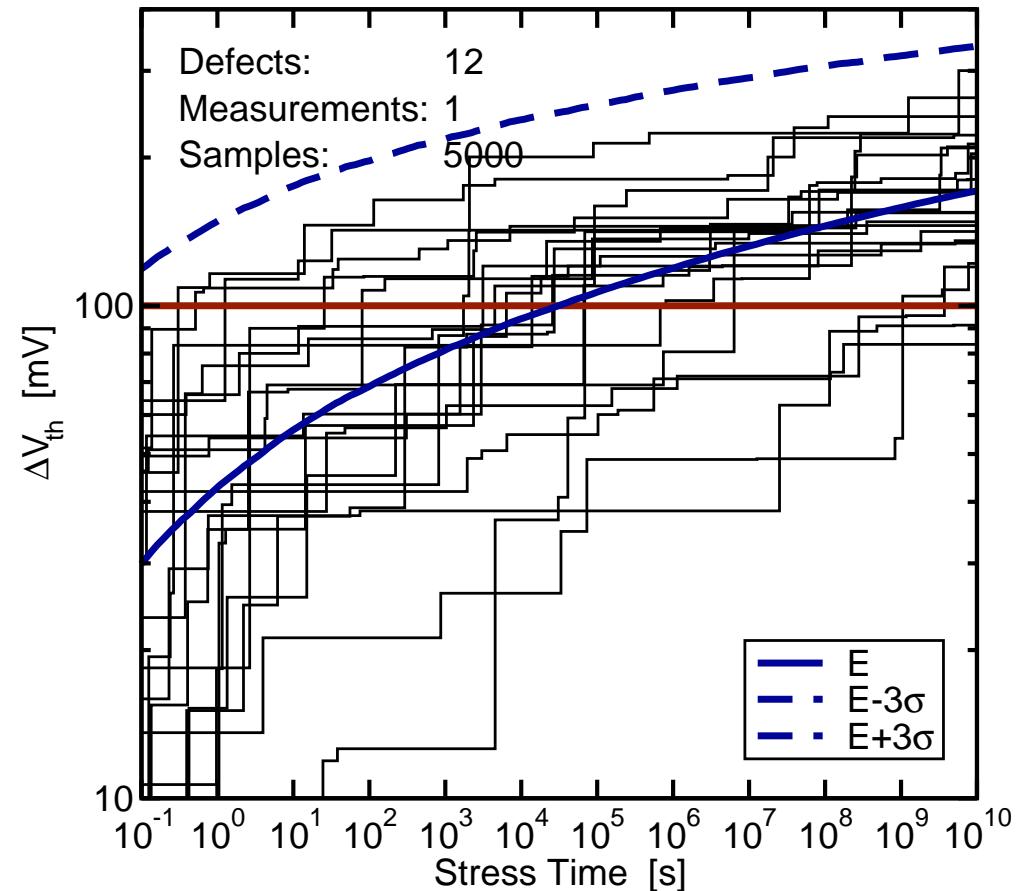
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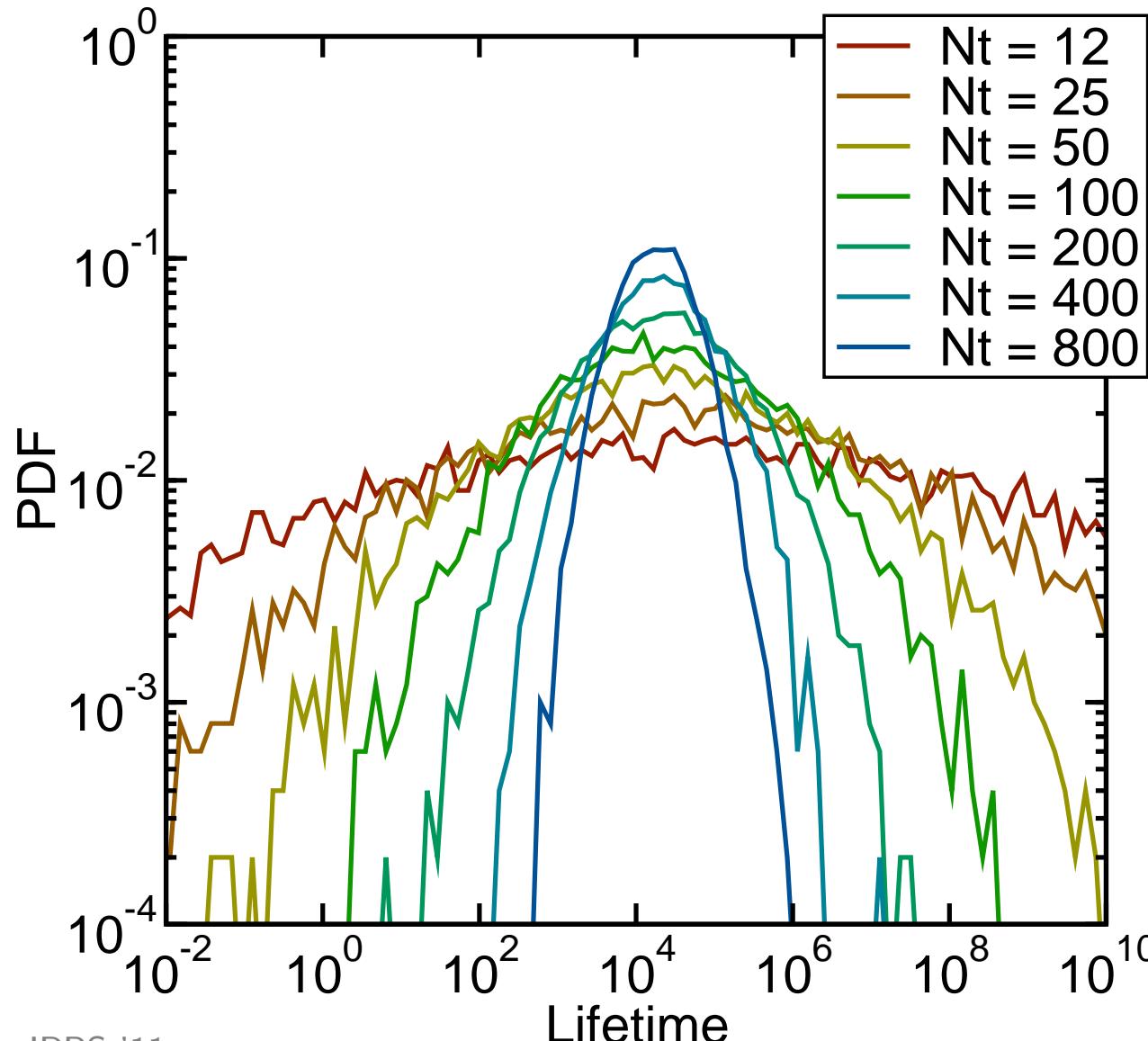


$35 \text{ nm} \times 35 \text{ nm} \Rightarrow 12 \text{ defects}$

Stochastic Lifetimes

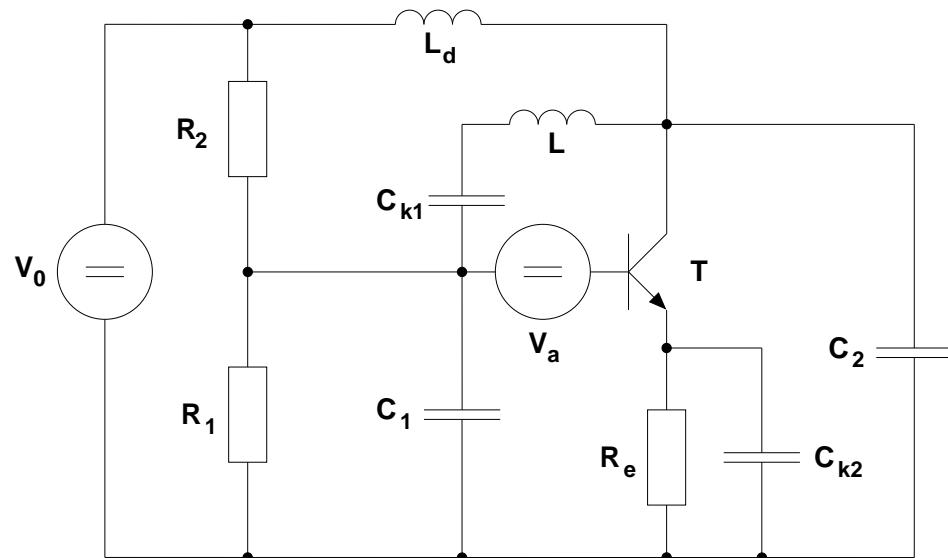
Distribution of lifetime^[1]

Variance increases with decreasing number of defects



[1] Kaczer et al., IRPS '11

How to Model This with SPICE?



Compact Modeling

First attempt: approximate multi-state model by two-state model^{[1][2]}

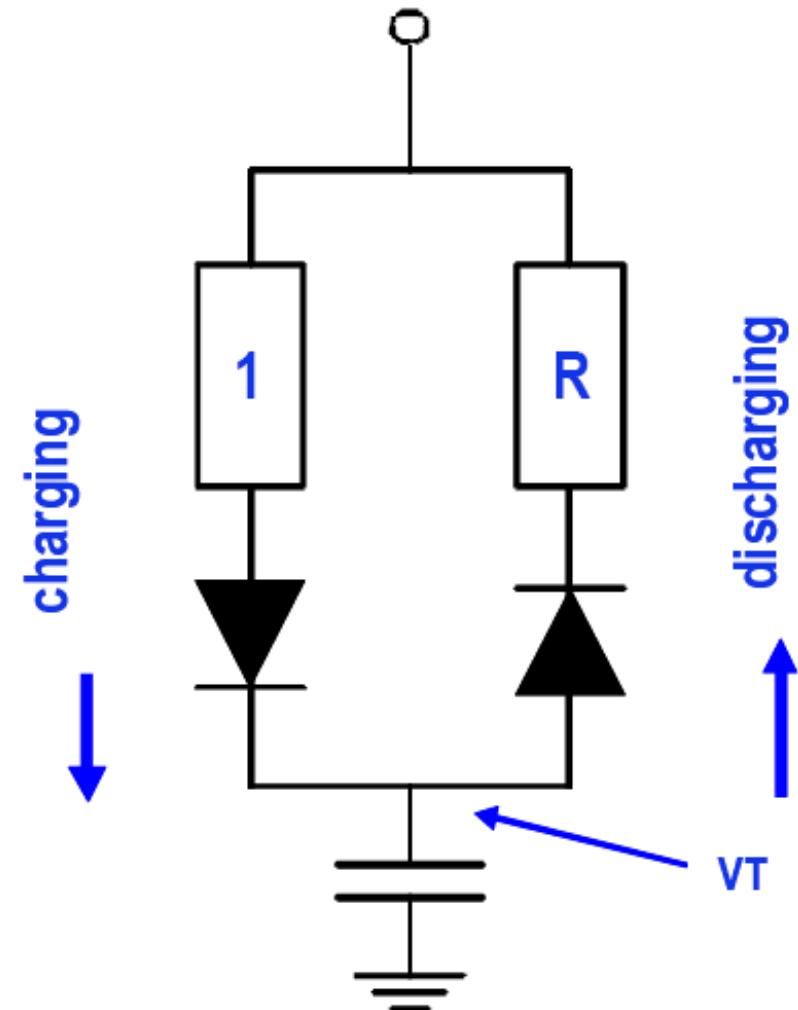
Try to capture the notoriously difficult dynamics first

Effective capture and emission time constants

Differential equation for a two-state model

Corresponds to an RC equivalent circuit

Two branches: charging vs. discharging

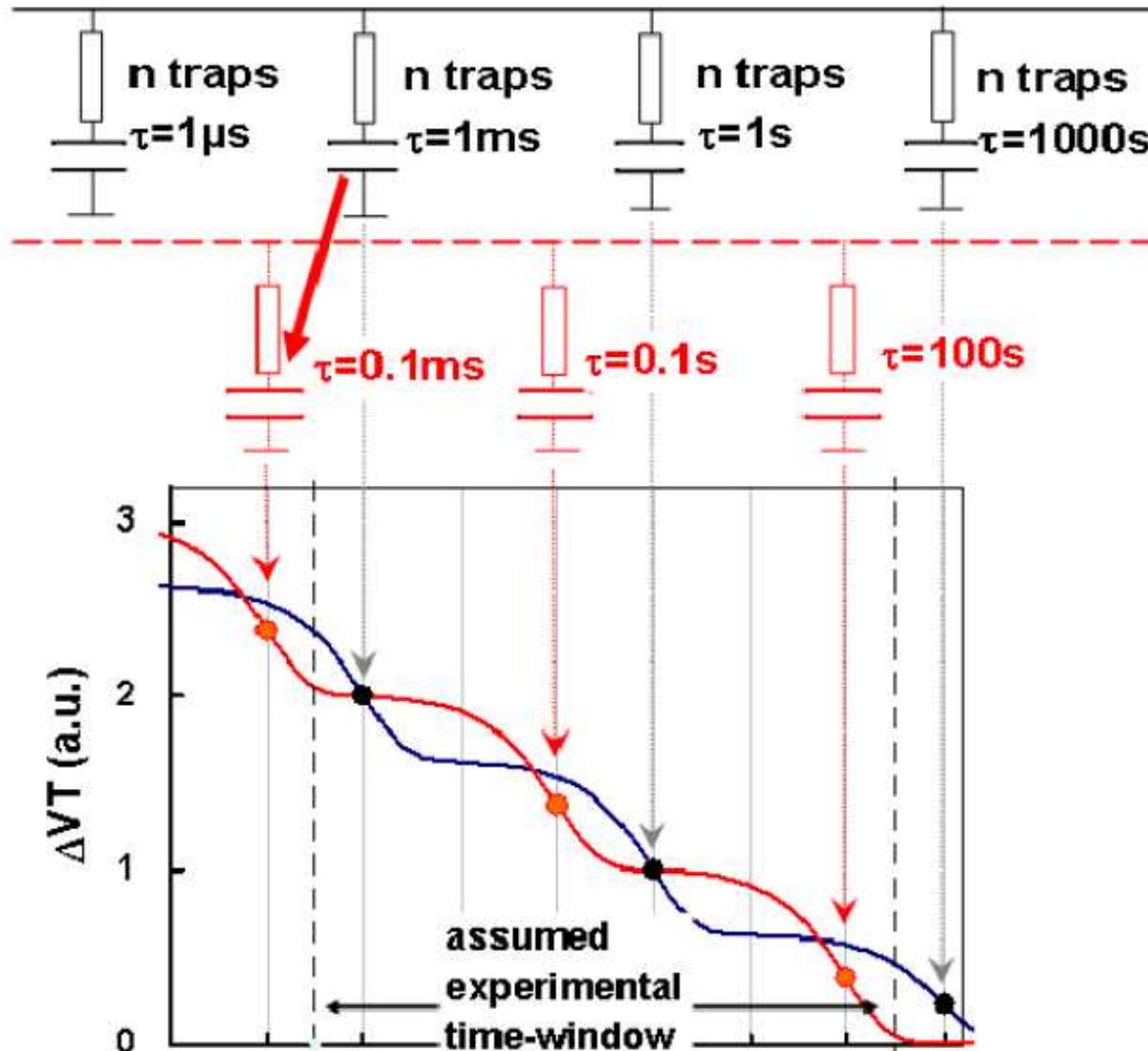


[1] Kaczer et al., IRPS '10 [2] Reisinger et al., IRPS '10

Compact Modeling

Example: modeling of recovery^[1]

Crude approximation: 1 RC element every 3 decades

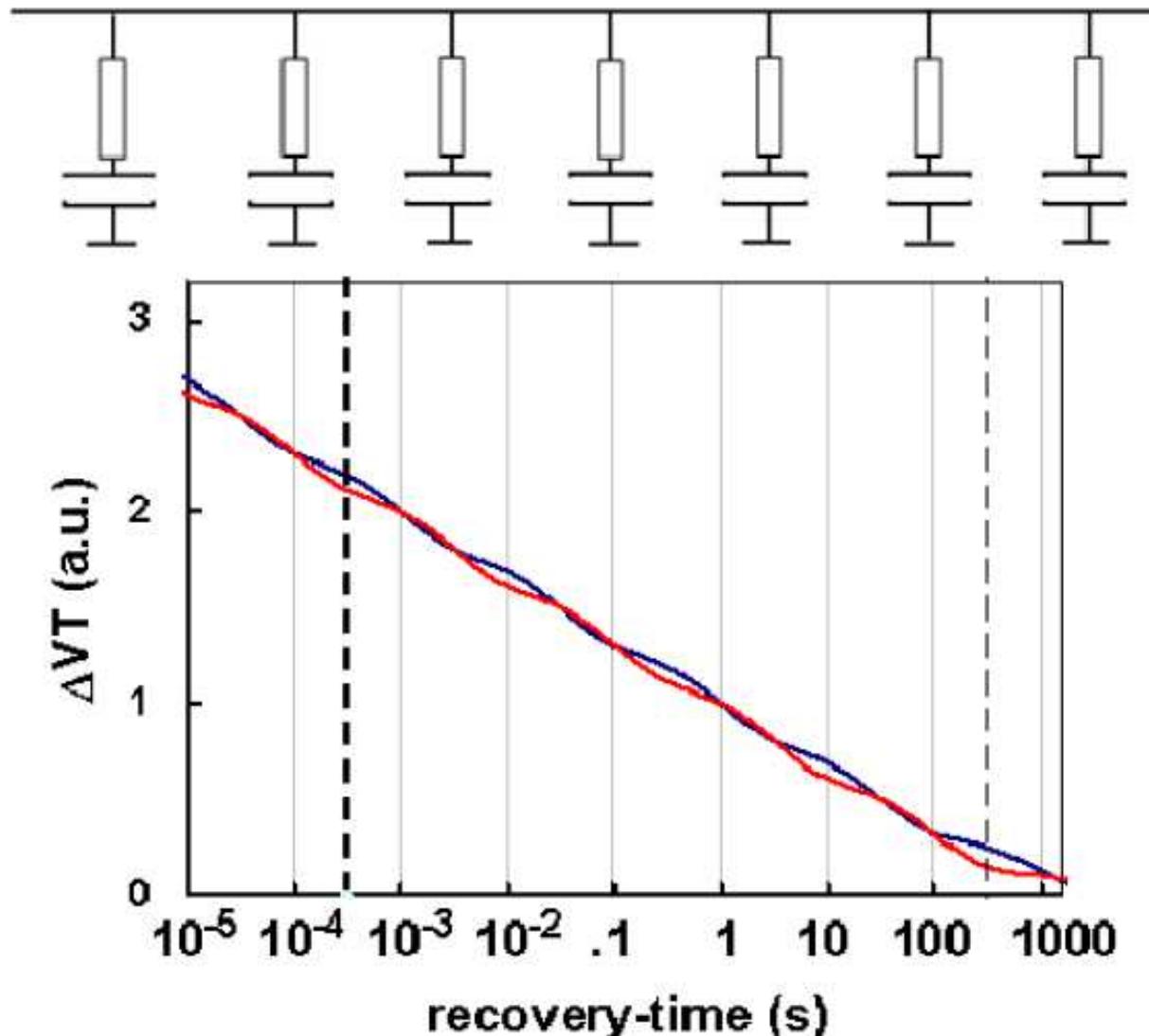


[1] Reisinger et al., IRPS '10

Compact Modeling

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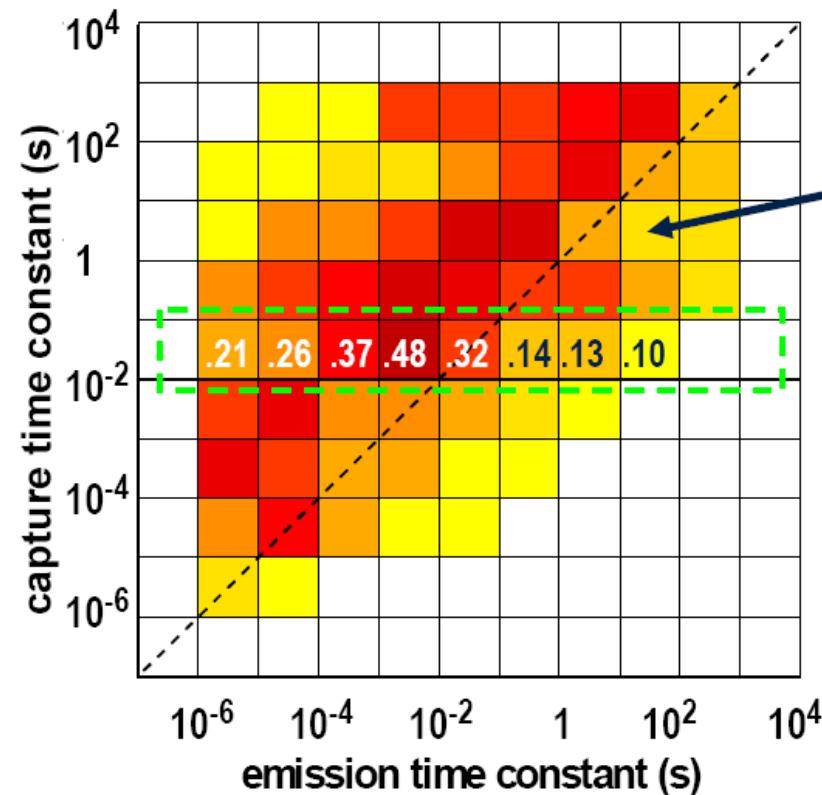
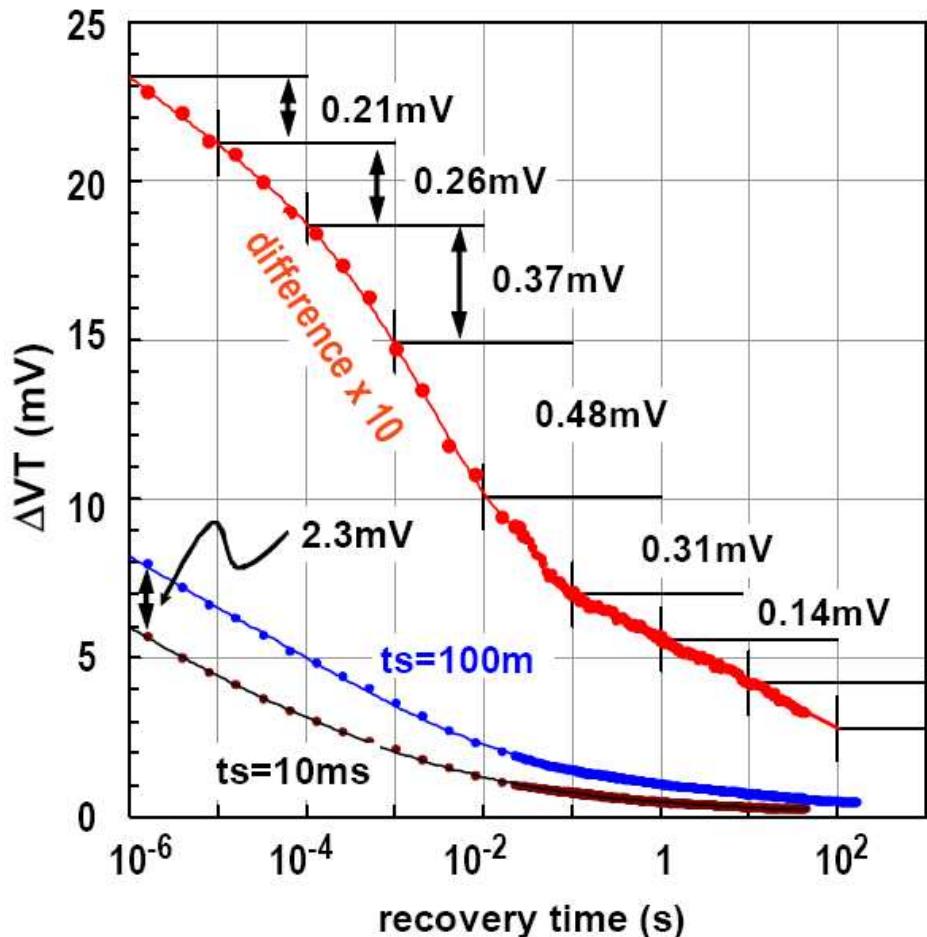
Finer approximation: 2 RC elements every 3 decades



[1] Reisinger et al., IRPS '10

Compact Modeling

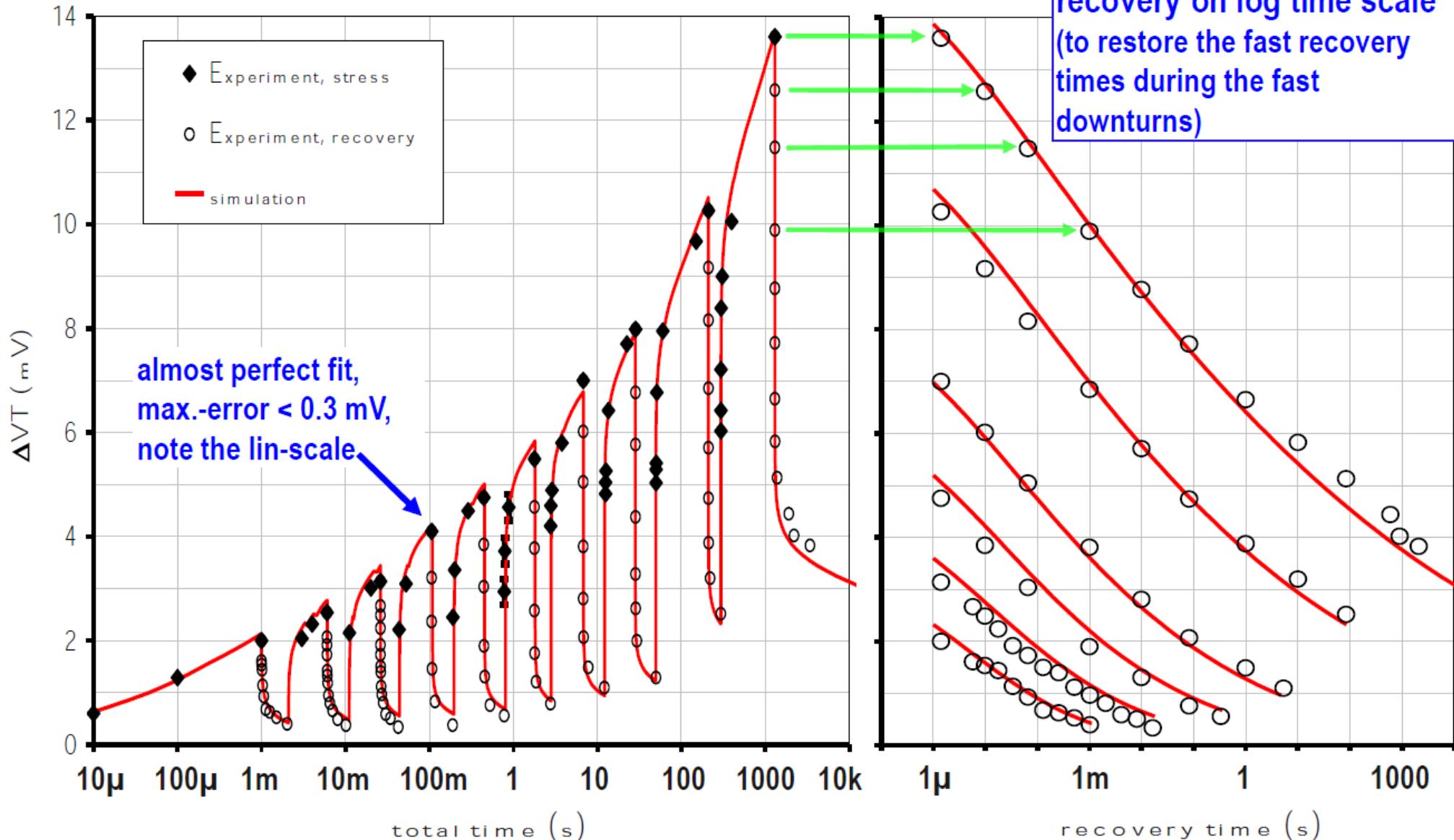
Extraction of the time constants^[1]



[1] Reisinger et al., IRPS '10

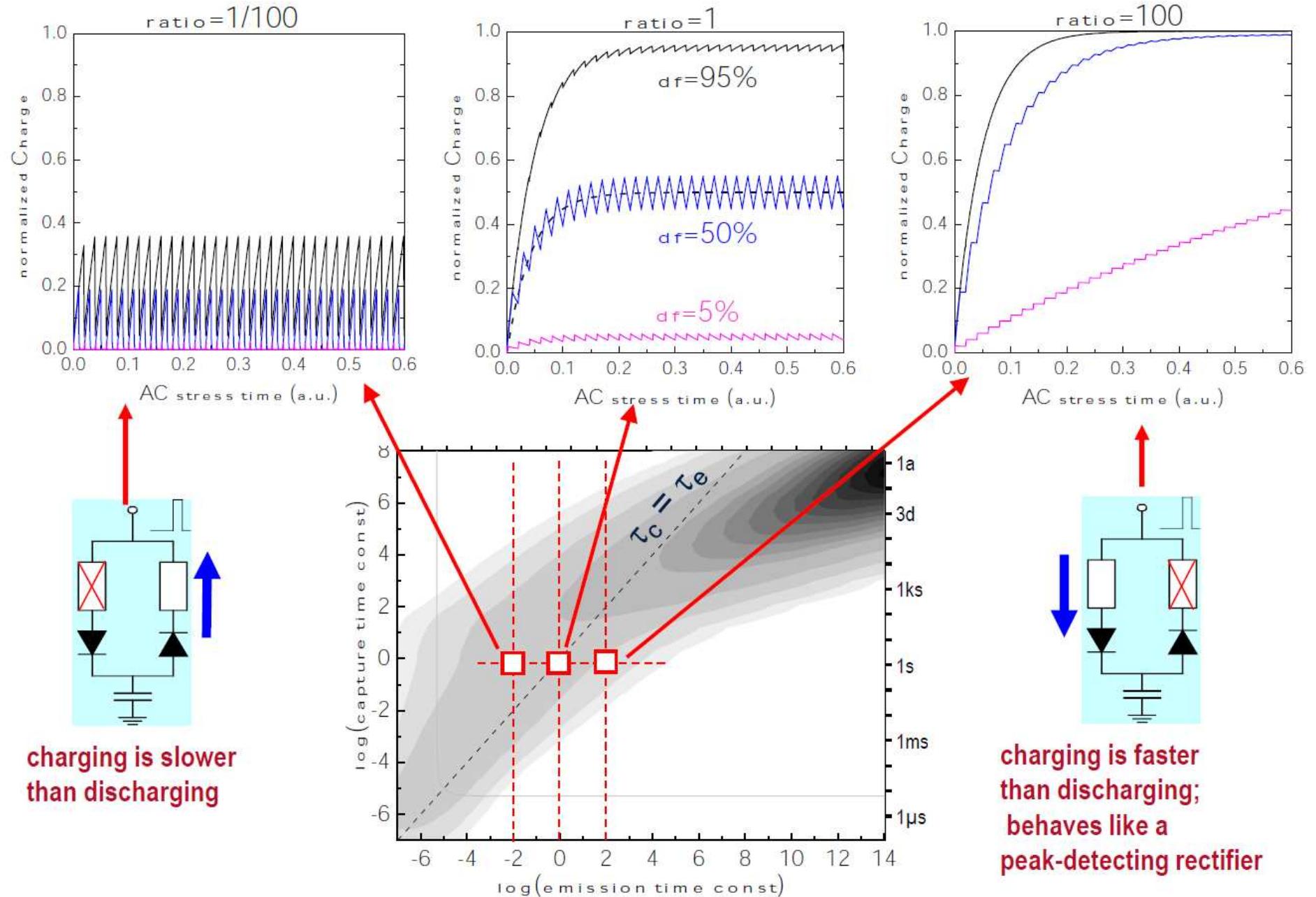
Compact Modeling

Example: dynamic stress/recovery experiment^[1]



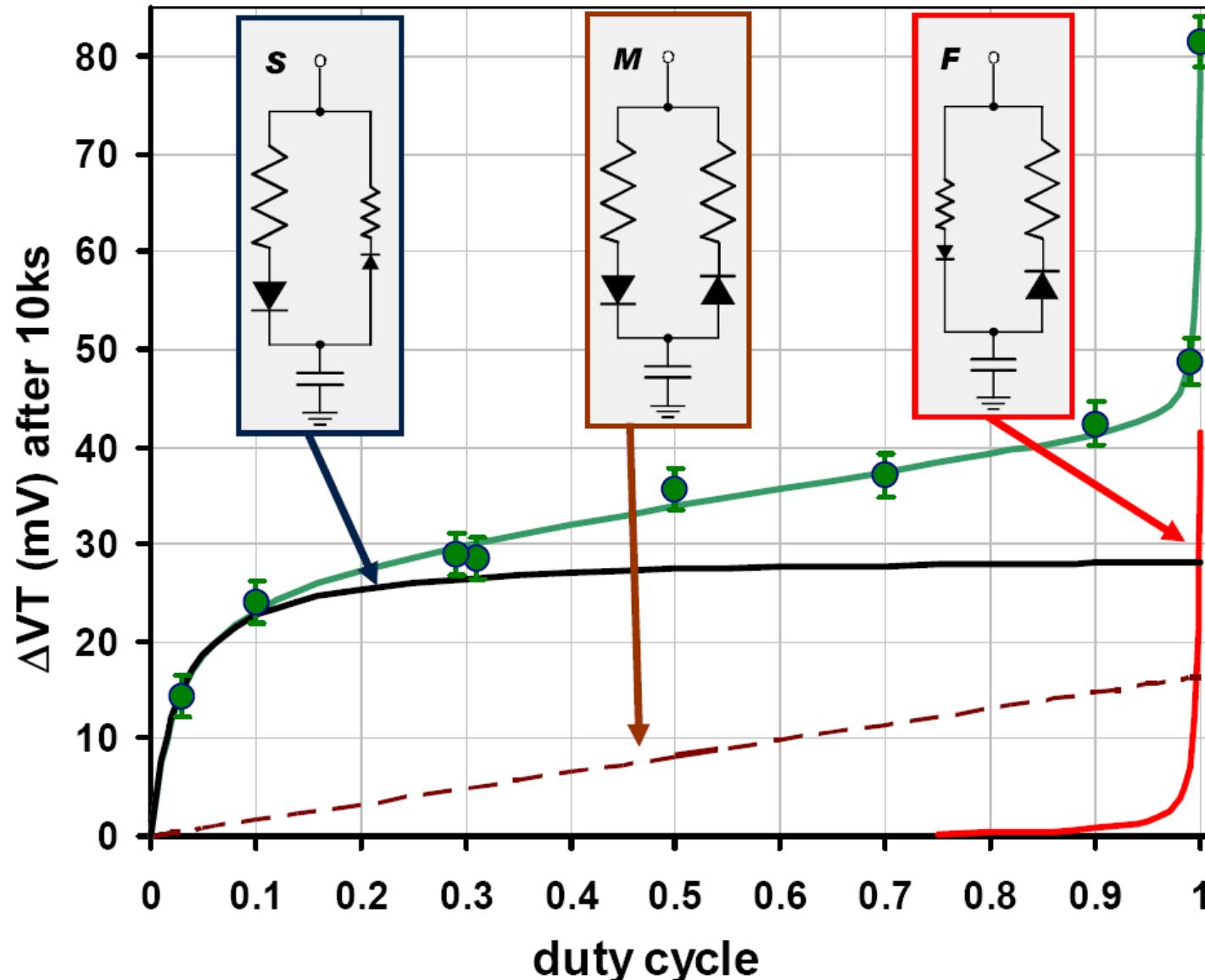
[1] Reisinger et al., IRPS '10 and IRPS '11 (Tutorial)

Compact Modeling: Duty Factor Dependence



Compact Modeling: Duty Factor Dependence

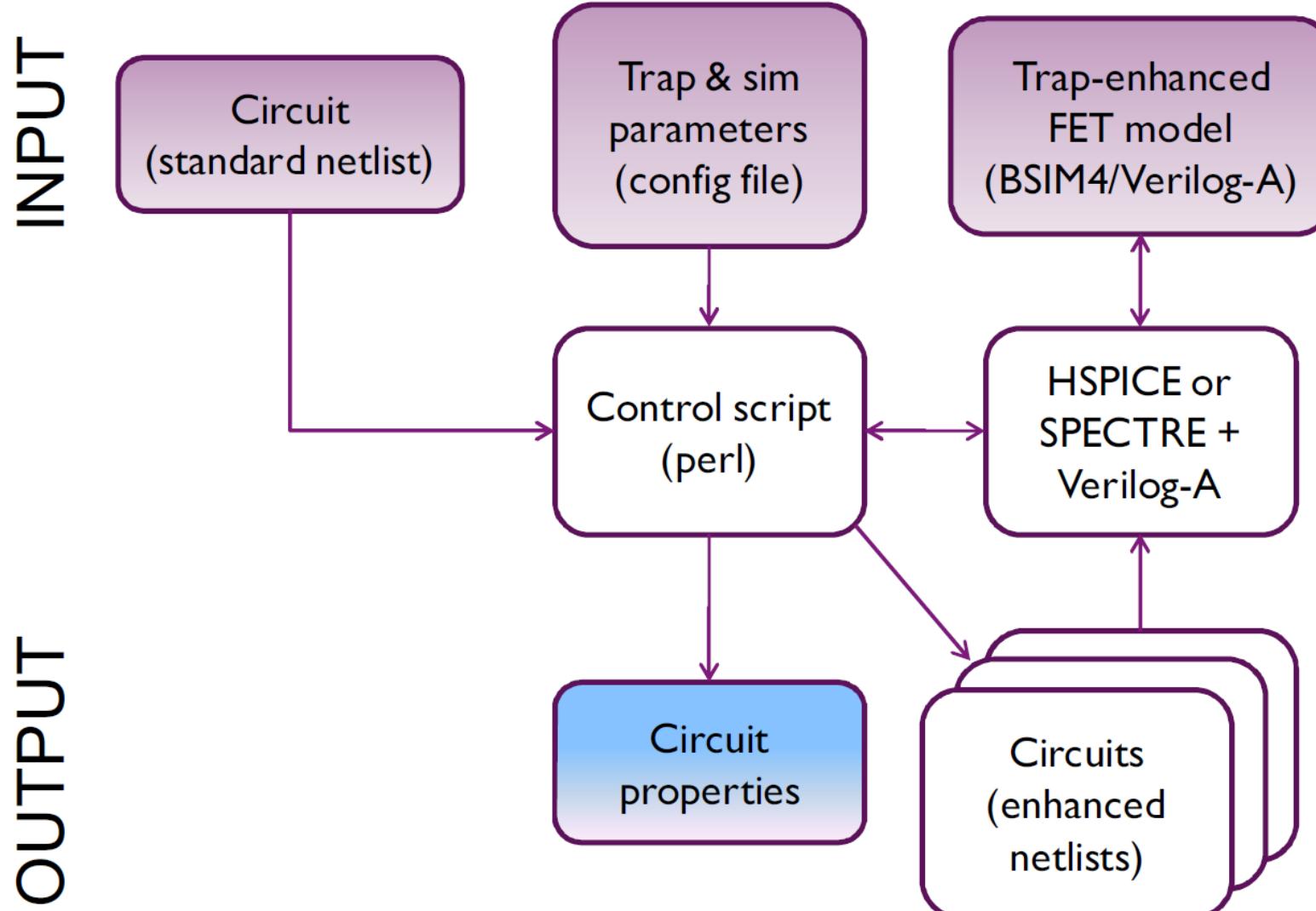
Notorious problem^{[1] [2] [3]}



[1] Grasser *et al.*, IEDM '07 [2] Grasser *et al.*, IRPS '08 (Tutorial) [3] Reisinger *et al.*, IRPS '10/IRPS '11 (Tut.)

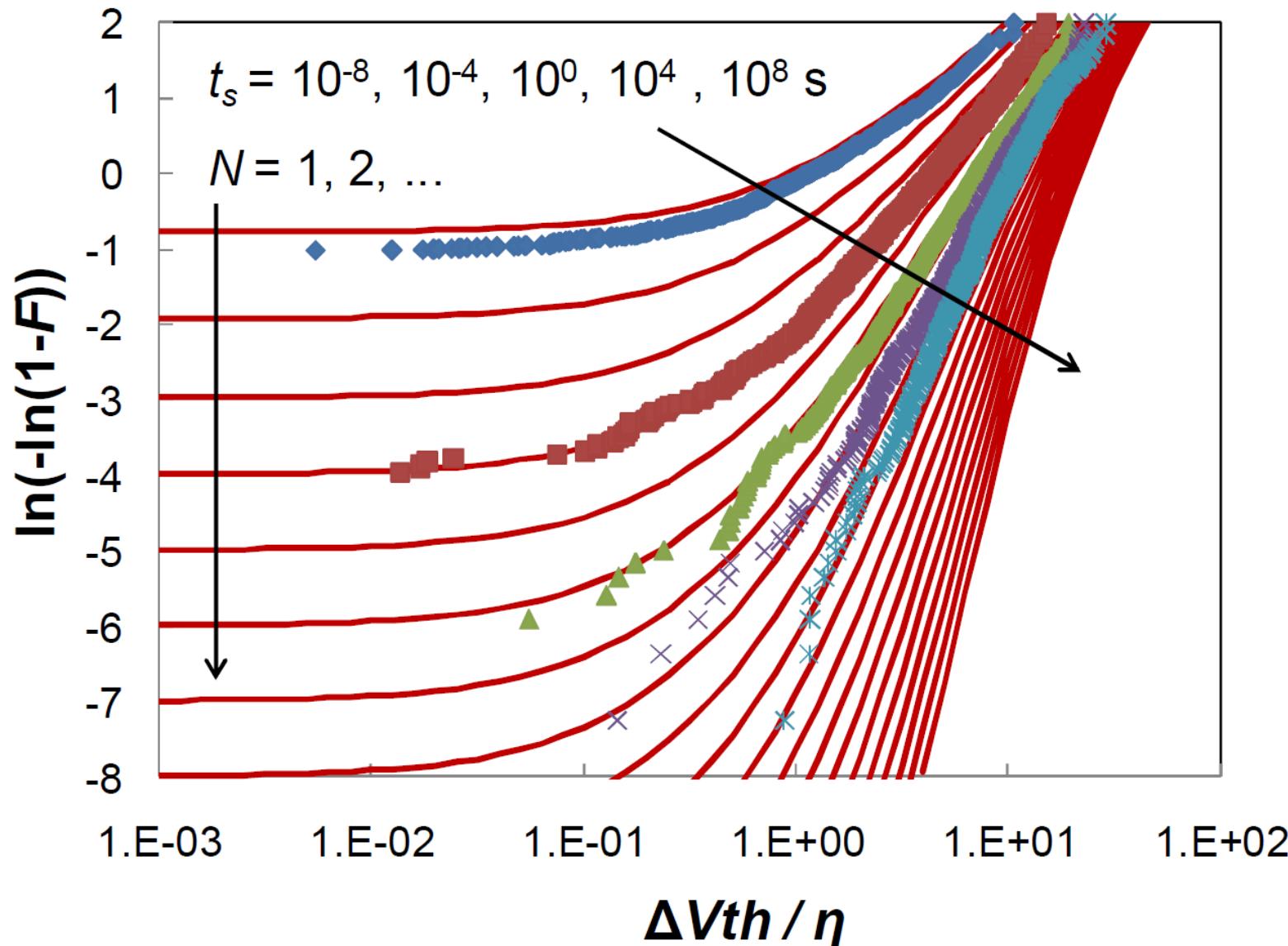
Stochastic Impact on Circuit

Implementation of stochastic behavior of distributed traps in VERILOG^[1]



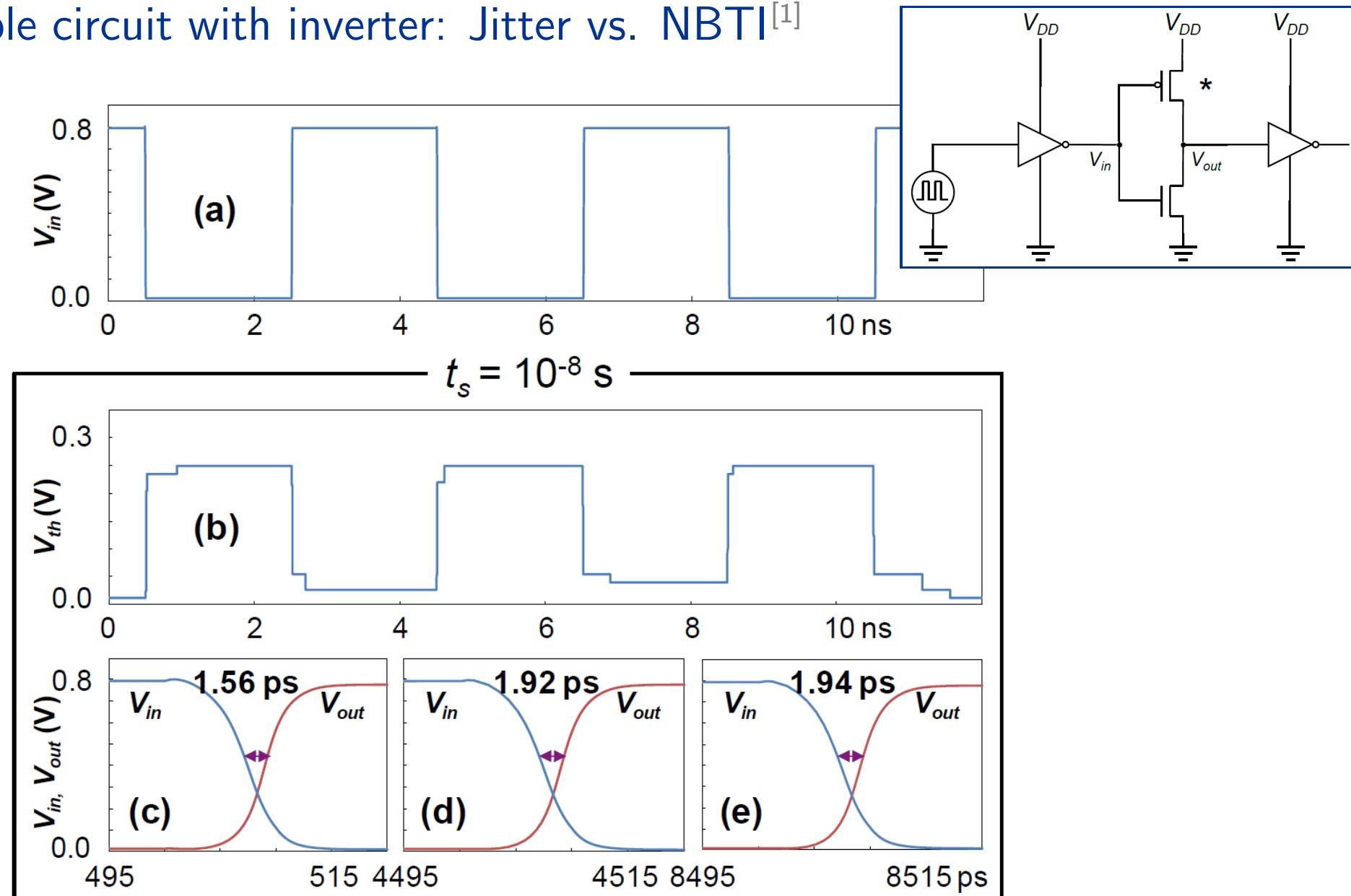
Stochastic Impact on Circuit

Model correctly incorporates distribution of ΔV_{th}



Stochastic Impact on Circuit

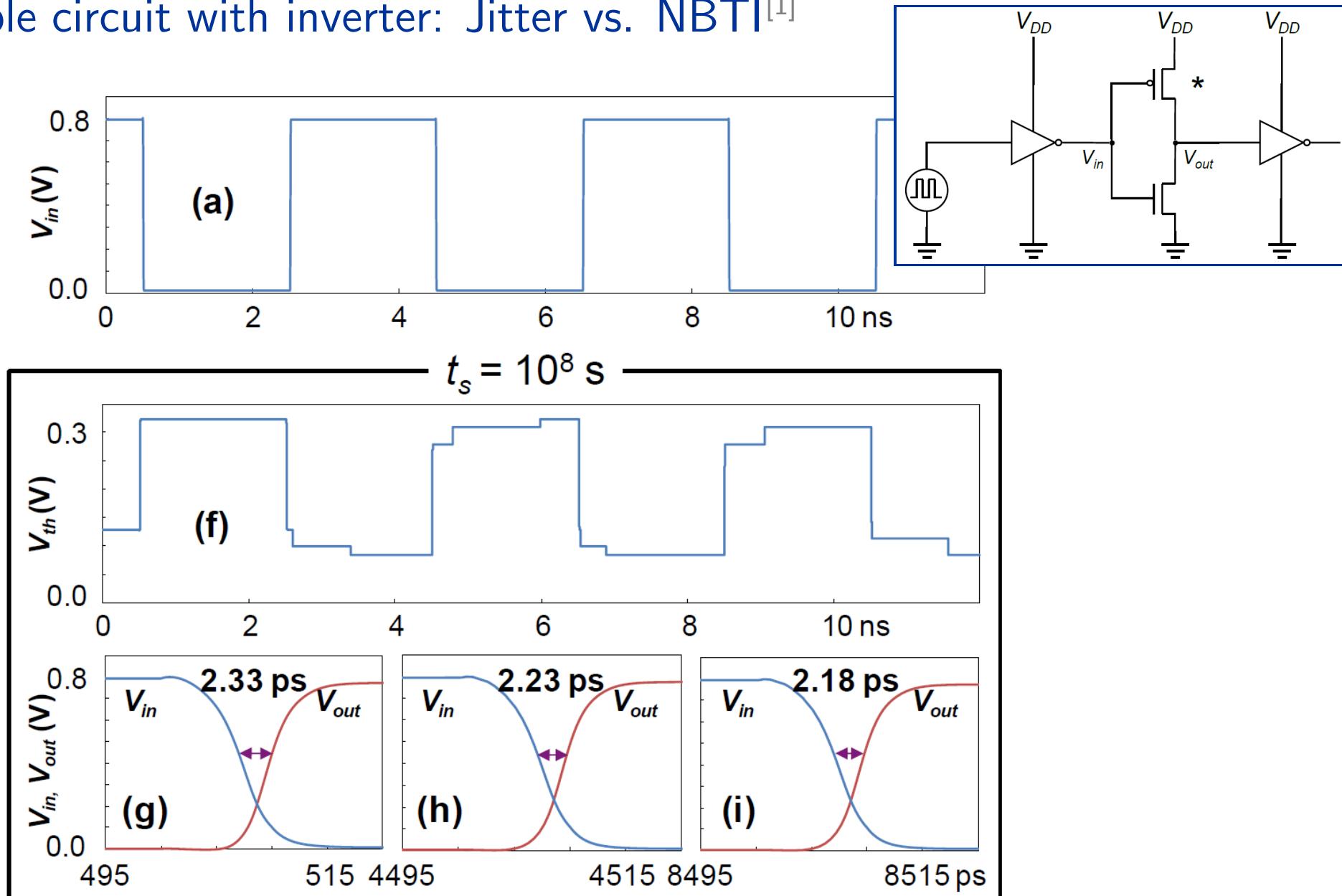
Example circuit with inverter: Jitter vs. NBTI^[1]



[1] Kaczor et al., IRPS '11

Stochastic Impact on Circuit

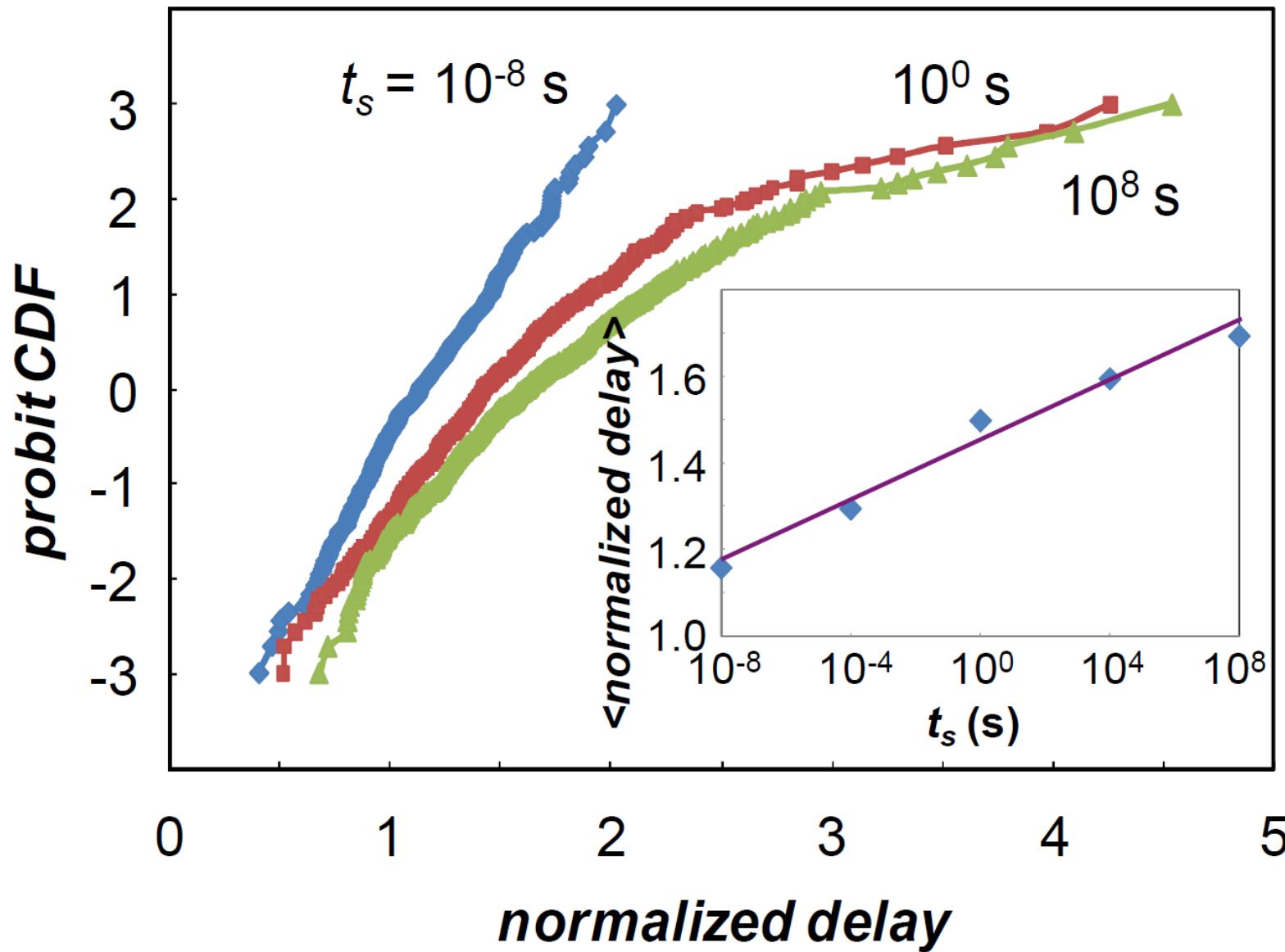
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[1] Kaczer et al., IRPS '11

Stochastic Impact on Circuit

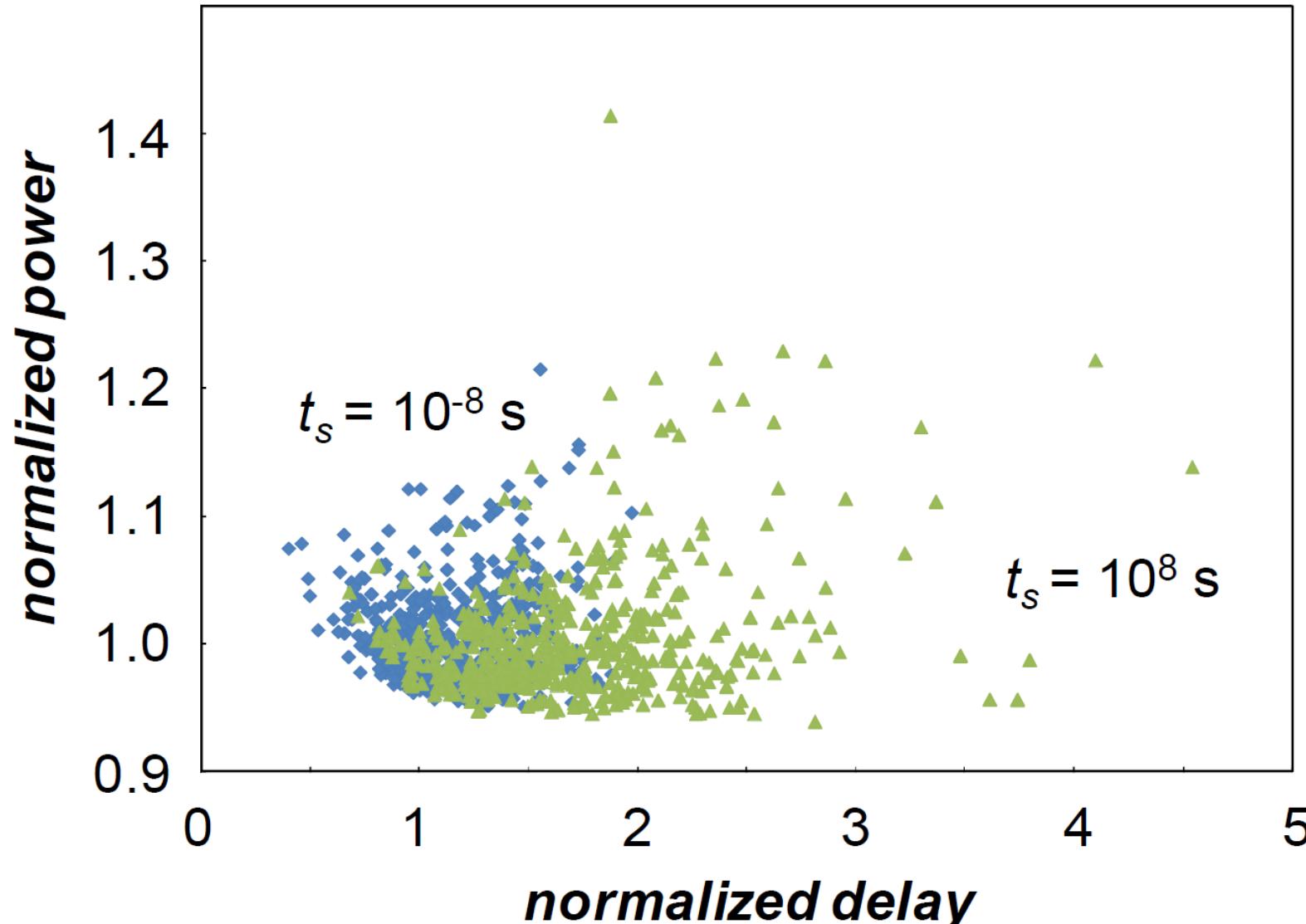
Distribution of delay widens with time^[1]



[1] Kaczer et al., IRPS '11

Stochastic Impact on Circuit

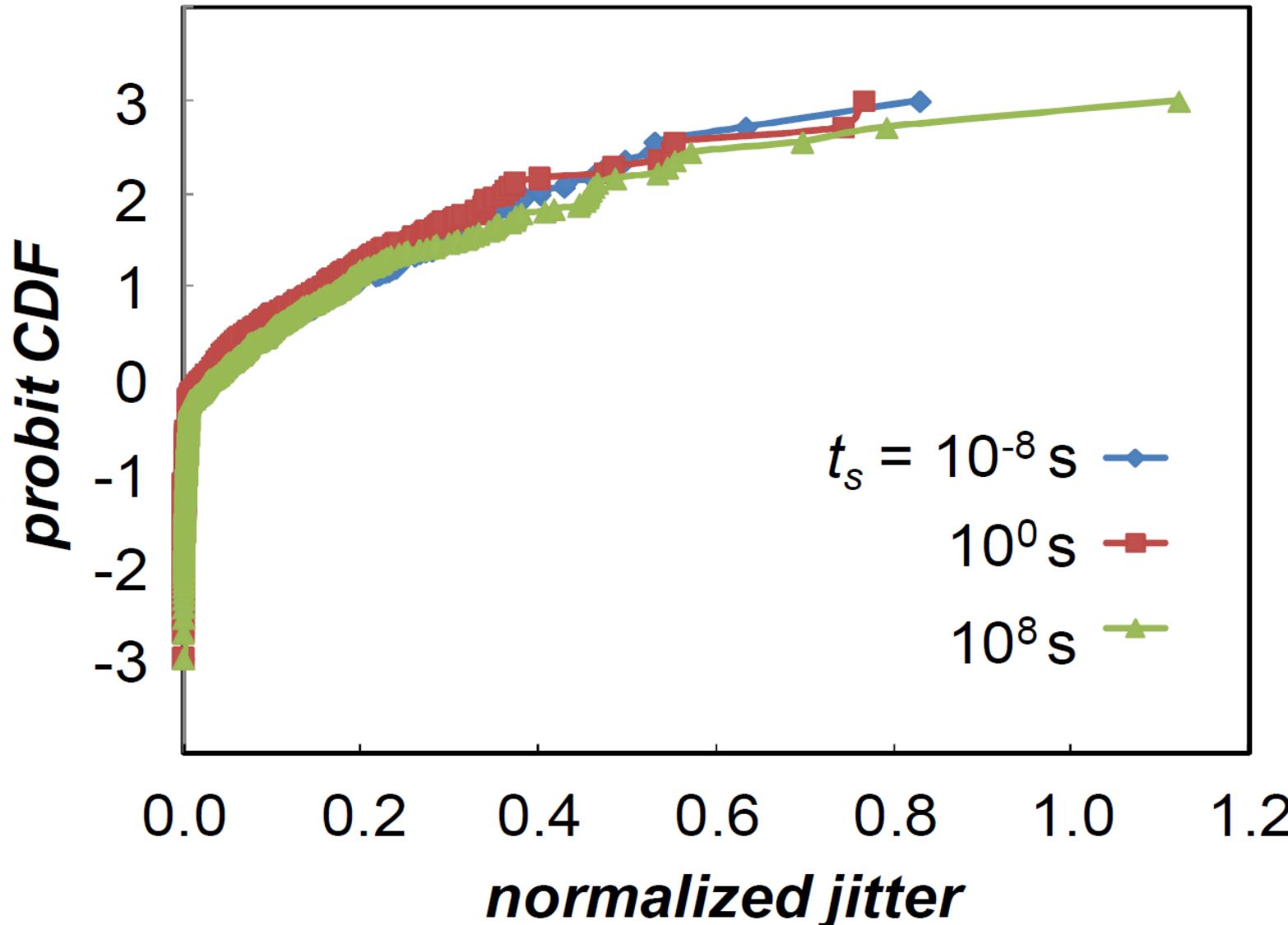
Normalized delay-power plot shifts and widens with time^[1]



[1] Kaczer et al., IRPS '11

Stochastic Impact on Circuit

In this model, jitter is independent of aging^[1]



[1] Kaczor et al., IRPS '11

Stochastic Impact on Circuit

Runtime penalty of VERILOG implementation

Example circuit with 6 MOSFETs

15 traps per MOSFET (90 traps in total)

SPECTRE 7.1.1 + BSIM4.4	SPECTRE + Verilog-A	SPECTRE + trap- enhanced Verilog-A
16.5 s	69 s	95 s
24%	100%	138%

Introduction

Stochastic NBTI on small-area devices: link NBTI and RTN

Physical defect modeling

Temperature- and bias-dependence

Anomalous defect behavior

Time-dependent variability

Reliability make variability time-dependent

Circuit model

How to approximate the essence for circuit simulation

Experimental support

Wide distribution of capture and emission times

Conclusions

Distribution of Capture and Emission Times

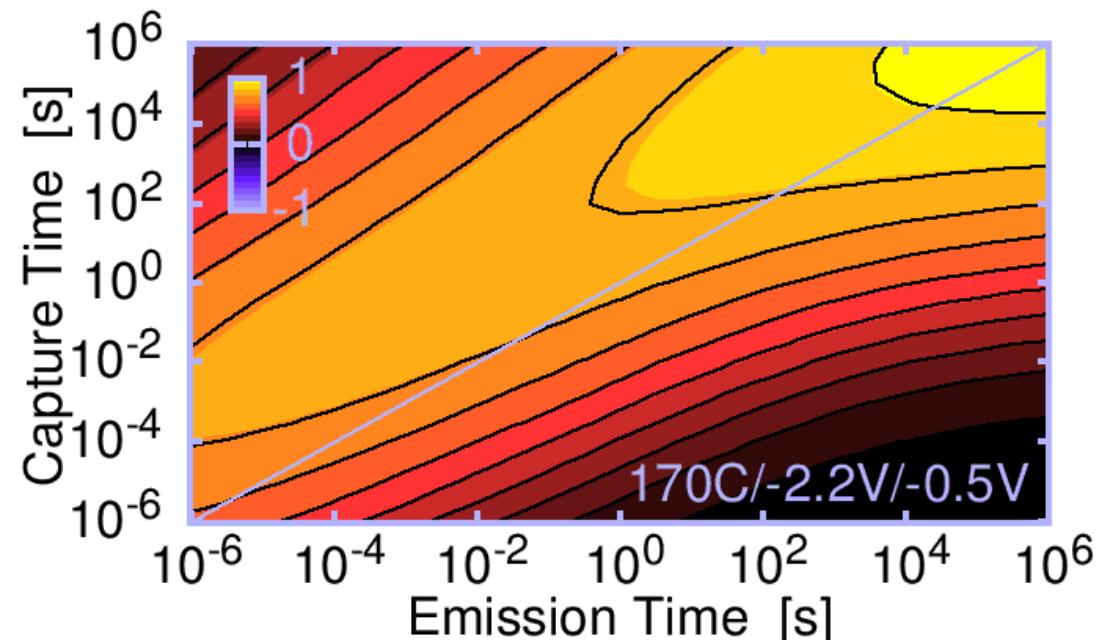
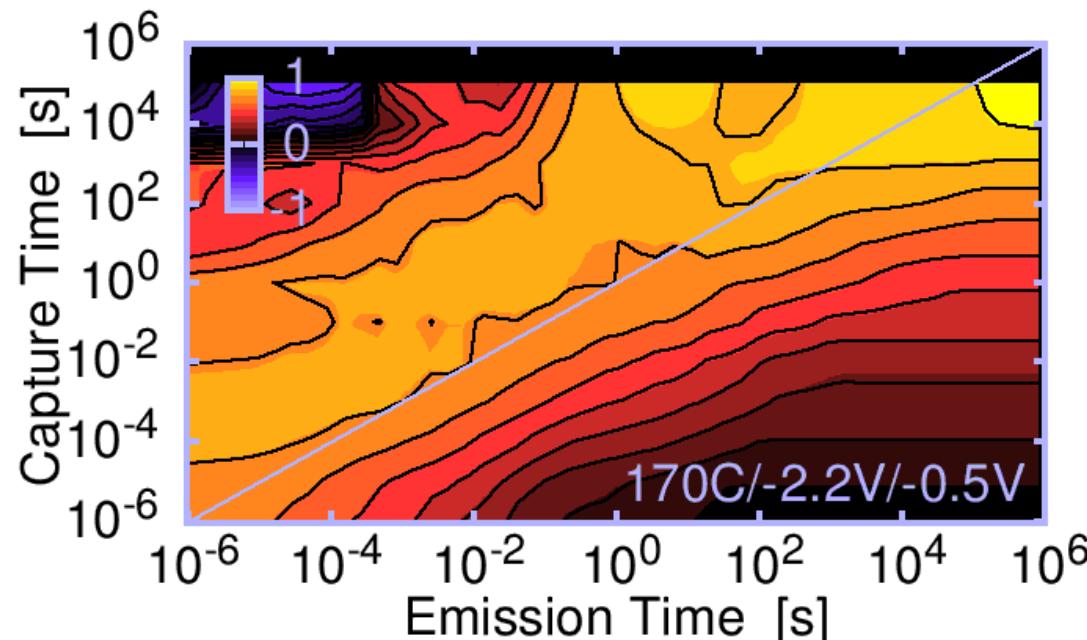
Realistic distribution (CET map) required^[1]

Measurement data fit with two Gaussian distributions

Allows estimation of the CET outside the experimental window

Uses distribution of the activation energies

Works over wide temperature and bias range



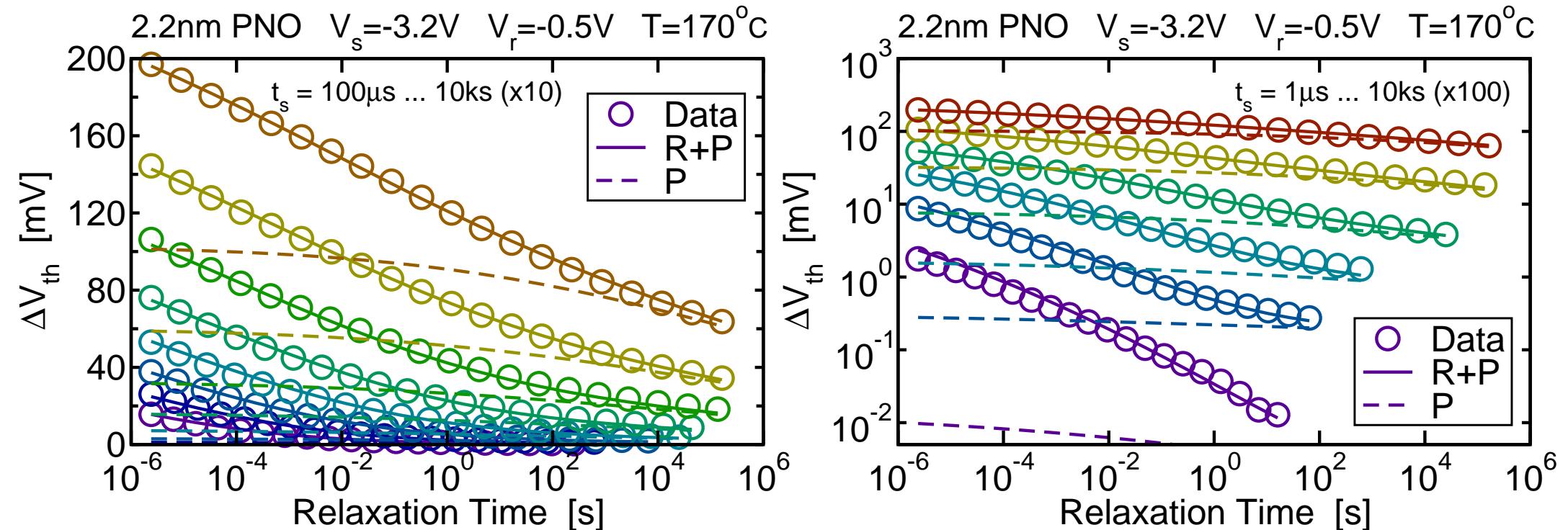
^[1] Grasser et al., IEDM '11

Distribution of Capture and Emission Times

Realistic distribution (CET map) required^[1]

Can describe arbitrary digital switching between two bias levels

Case #1: 2 weeks of DC-like on/off stress and recovery



[1] Grasser et al., IEDM '11

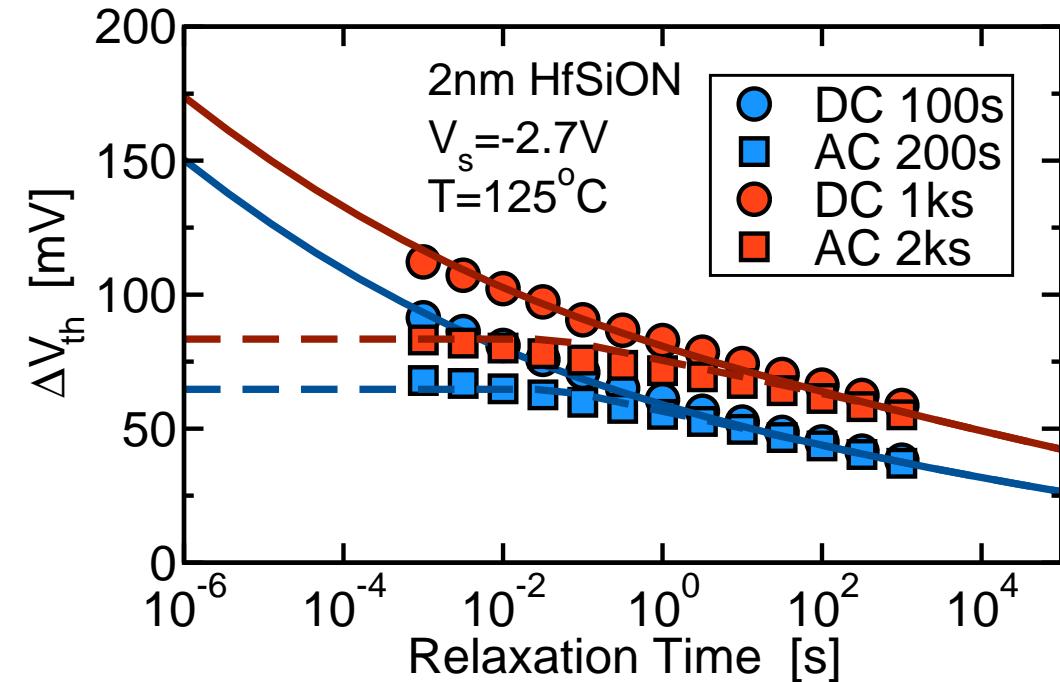
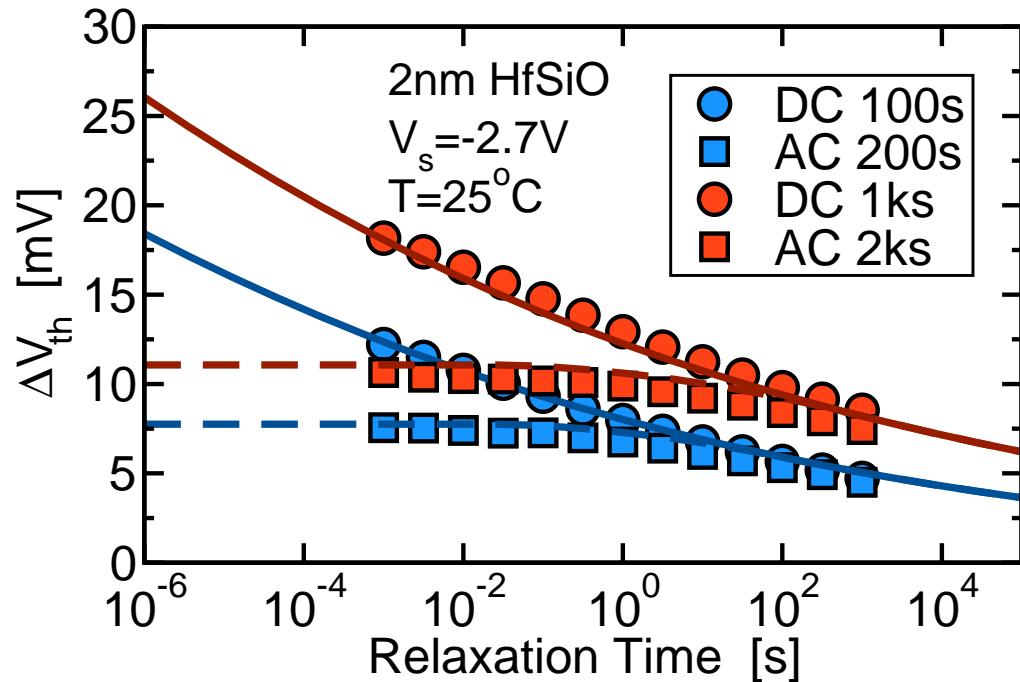
Distribution of Capture and Emission Times

Realistic distribution (CET map) required^[1]

Can describe arbitrary digital switching between two bias levels

Case #2: Comparison AC/DC NBTI on high- κ oxides

Many 'regular' stress/relax patterns can be solved analytically



[1] Grasser et al., IEDM '11

Conclusions

Statistics of individual defects become important in nanoscale MOSFETs

- Random number of traps

- Random distribution of traps in space

- Random defect properties

- Interaction with random discrete dopants

- Discrete stochastic charge capture and emission events

Fundamental implications on device reliability

- Lifetime is a stochastic quantity

- Lifetime will have a huge variance

Circuit modeling

- Capture expectation values using distributed RC elements in SPICE

- Capture all features using a VERILOG implementation

Accurate modeling requires detailed capture/emission time (CET) map

- Analytic (CET) model with built-in bias and T dependence

- Allows stochastic, circuit, and analytic solution for general AC/DC stress patterns

This work would have been impossible without the support of ...

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