Study of the Conduction Properties of the n^{++} GaN Cap Layer in GaN/InAlN/GaN E-HEMTs

Stanislav Vitanov, Jan Kuzmik and Vassil Palankovski

Abstract - **Carrier transport in normally-off n^{++} GaN/InAlN/AlN/GaN high electron mobility transistors is studied using two-dimensional numerical device simulation. We focus on the n^{++} GaN cap layer, which is removed under the gate, and its contribution to drain current. Our simulation results show that despite the high doping density and relatively high carrier concentration in this layer, no significant transport takes place during the on-state. Similarly, under the off-state bias condition, even though an increase in the electric field in the cap layer is observed, the leakage current is provided mostly by the buffer layer.**

Keywords – **HEMT, normally-off, simulation**

I. Introduction

The ongoing interest in the development of GaN-based enhancement-mode high electron mobility transistors (E-HEMTs) has resulted in several different approaches being proposed. While some rely on an additional cap layers in order to raise the conduction band [1],[2], others employ a reduction of the gate-to-channel distance either by recessed-gate technique [3],[4] or reduction of the overall barrier layer thickness. However, reducing the gate-to-channel distance has a negative impact on the HEMT access resistance [5], mainly due to the close proximity of the surface potential [6]. Another major challenge is the development of a suitable dry-recess technique, which is hindered by plasma-induced damage.

Compared to conventional AlGaN/GaN structures, InAlN/GaN HEMTs exhibit higher polarization charge even without strain in the barrier [7]. However, they also may suffer a loss in performance due to parasitic effects related to surface traps. A mechanism to mitigate this is increasing the distance of the two-dimensional electron gas (2DEG) to the surface at access regions by an undoped GaN cap layer [8]. However, in this case to remove a relatively thick GaN cap under the gate, a rather difficult two-step dry etching technique is needed. To adopt a single gate recessing, a better approach is to use a n^{++} GaN cap layer [9]. The thickness of the cap can be drastically downscaled in this case as free carriers in GaN screen the surface potential.

Such an approach is adopted by Kuzmik *et al.* [9], who analyze the impact of the cap layer on parasitic effects and on the mechanism of the off-state breakdown. In this work we complement the experimental results with data obtained from two-dimensional device simulation using our simulator Minimos-NT [10].

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We have employed it previously for the optimization studies for a whole generation of AlGaN/GaN HEMTs [11], but also for high-temperature simulations [12]. Using an established setup of models and model parameters [13] our simulation results provide an excellent agreement with the experimental data and allow for a profound study of the carrier transport in the n^{++} GaN cap layer.

II. Device Description

The simulated devices are adopted from [9]. The structures consist of a 2 μm GaN layer, followed by 1 nm lattice-matched AlN, 1 nm InAlN and 6 nm GaN:Si cap (Fig. 1). The doping concentration in the cap layer is $2\text{x}10^{20}$ cm^{-3}. The source-to-drain distance of the simulated device is 4 μm, the source-to-gate distance is 1 μm, and the gate length L_g is 0.5 μm. The structures are not passivated.

III. Simulation Setup

The simulations are performed using our two-dimensional device simulator Minimos-NT. Our choice of transport model aims to achieve maximum accuracy combined with computational efficiency. Since the drift-diffusion transport model is not able to deliver accurate results for sub-micron GaN FETs, we employ a proper hydrodynamic transport model [13]. As AlGaN/GaN HEMTs are unipolar devices, computational effort is reduced by neglecting the equations for holes in this work. Self-heating effects are accounted for by the lattice heat flow equation.

Finally, a system of four partial differential equations: Poisson, current continuity and energy balance for electrons, and the lattice heat flow equations, is solved self-consistently. These four differential equations have material-specific parameters, such as the bandgap energy, electron mobility, thermal conductivity, etc. The dependence of these parameters on temperature, energy, etc. is described by models, which are described elsewhere [12].

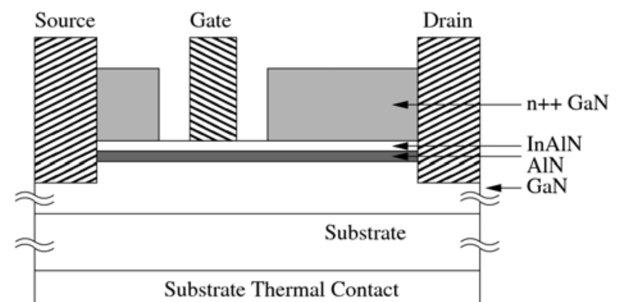

Fig. 1: Schemtaic layer structure of GaN/InAlN/AlN/GaN HEMT.

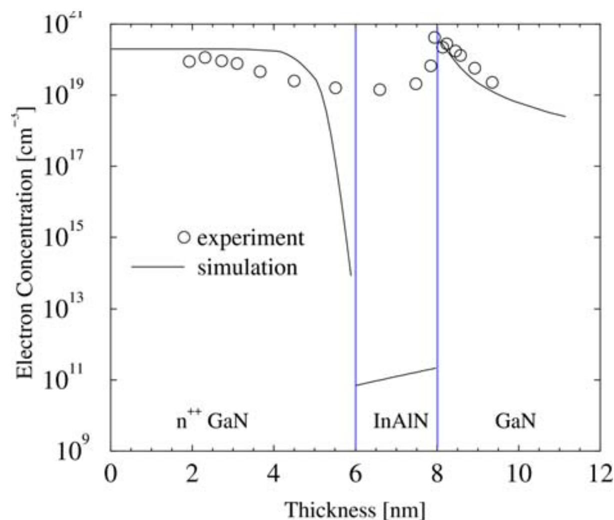

Fig. 2: Electron concentration in a vertical cut (V_{GS}=1.5V, V_{DS}=8.0V).

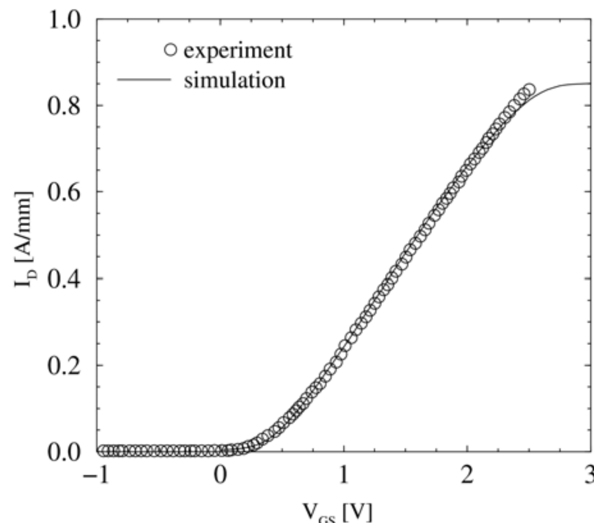

Fig. 3: Simulated and measured transfer device characteristics.

We assume a metal diffusion of the metal source and drain contacts reaching into the channel. For simplicity, the AlN/InAlN spacer/barrier system is replaced by a 2 nm thick InAlN barrier in the model. The positive charges (introduced by polarization effects) at the channel/barrier interface is compensated by a commensurate negative surface charge at the barrier/cap interface. The polarization charge density is 2.8 x 10^{13} cm^{-3} [7].

IV. Cap Layer Design

In order to provide sufficient screening of the 2DEG from the surface traps, the cap layer must fulfill certain requirements regarding thickness and doping. The volume of the cap layer needs to provide enough free carriers to compensate the charge variation at the GaN trapping surface additionally to the interface depletion effects of the ideal interfaces. Therefore, high doping is preferable, and a doping concentration of $2x10^{20}$ results in a cap layer thickness of 6 nm [9]. Indeed the experiment showed that such a specification yields a total free charge density high enough to effectively screen the 2DEG [9]. This can be observed in Fig. 2, where the electron concentration in a vertical cut is plotted as determined by the C-V measurement and the simulation. Our theoretical results are in good agreement with the experimental data, especially for the 2DEG concentration. Further, both the measurement and the simulation show depletion on the InAlN side of the cap.

On the other hand, despite the high doping in the GaN cap, Kuzmik *et.al.* [9] assumed that the carrier depletion at the GaN/InAlN junction and the termination of the current path in the GaN cap by the gate recess prevent contribution of the GaN cap to the drain-source current (I_{DS}) along the recess region. This was confirmed by a modified transmission line method (TLM) test in which the values of the contact resistance and the intrinsic channel resistance were determined directly from the access regions of the HEMT [9]. The technique also indicates that in the DC regime the HEMT access resistance is defined by the full contact-to-contact separation and not just by the narrow separation of the gate to the n^{++} GaN cap.

V. Simulation Results

In order to validate the calibration of the simulation software the theoretical results for the dc characteristics of the devices are compared to the experiment. Fig. 3 shows measured and simulated data for the transfer characteristics. These exhibit an excellent agreement. We further focus on carrier transport in the GaN cap and the 2DEG. Fig. 4 shows the current density in the region close to the gate. The simulated device is biased to on-state at V_{GS}=1.5V and V_{DS}=8.0V. The highly conductive 2DEG region is clearly distinguished. In the InAlN barrier (and AlN layer) the electron concentration is very low (see Fig. 2), therefore there is no current observed except for a narrow “channel” under the edge of the n^{++} GaN cap. In the latter, however the current is two to three orders of magnitude lower than in the 2DEG. This is confirmed in Fig. 5, which shows the current density in a vertical cut in the gate-drain region (same position as the cut in Fig. 2). Thus, the simulations confirm, that the n^{++} cap layer does not significantly contribute to the current transport.

It should be also mentioned, that while the drain side of the cap indeed does exhibit some minimal current, in the source side there is no current at all. The reason is the distribution of the electric field. The electric field distribution is further investigated under the off-state bias condition (V_{GS}=0.0V, V_{DS}=8.0V). The electric field has its peak at the drain side of the gate region (Fig. 6) so there are

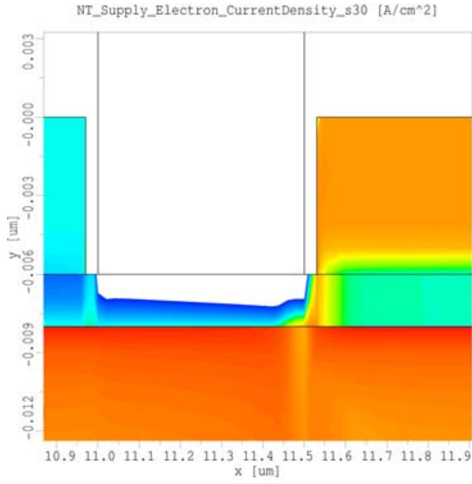

Fig. 4: Electron current density in the gate region in the on-state (V_{GS}=1.5V, V_{DS}=8.0V).

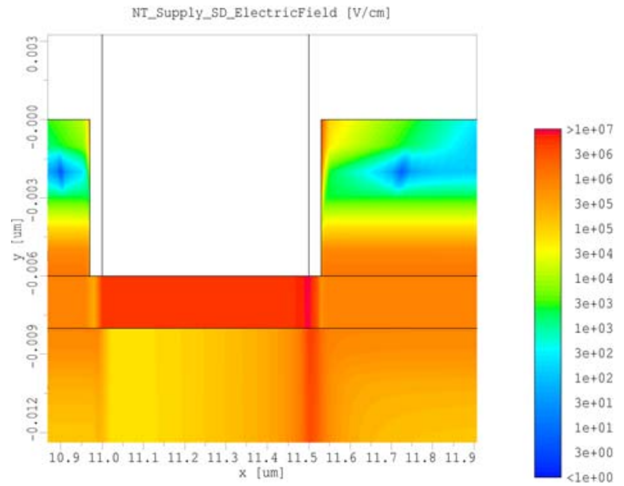

Fig. 6: Electric field distribution in the gate region in the off-state (V_{GS}=0.0V, V_{DS}=8.0V).

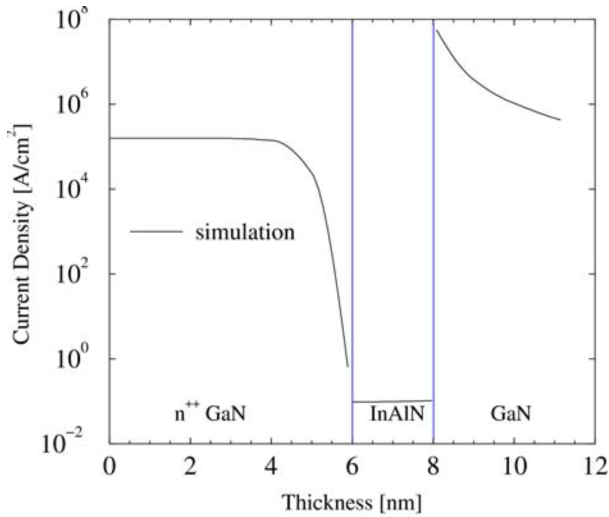

Fig. 5: Electron current density in a vertical cut in the on-state (V_{GS}=1.5V, V_{DS}=8.0V).

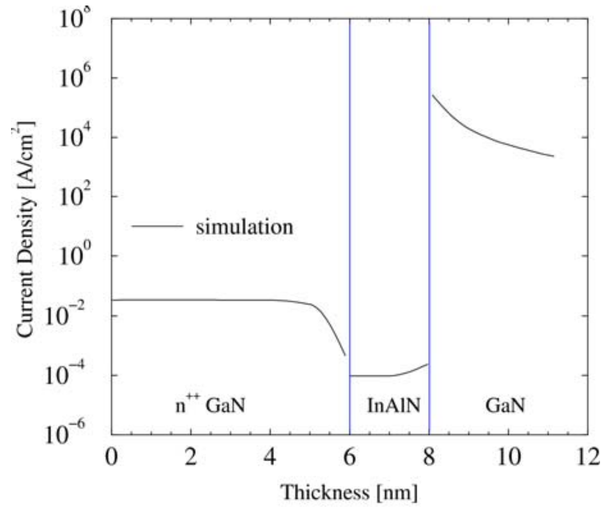

Fig. 7: Electron current density in a vertical cut in the off-state (V_{GS}=0.0V, V_{DS}=8.0V).

carriers with high enough energy to overcome the potential barrier of the InAlN barrier . On the source side of the gate the electric field is overall lower, so a transport through the barrier is not possible, which results in a minimal current density in the n^{++} cap layer.

Fig. 7 shows again a cut of the current density in the gate-drain region, however in the off-state bias of V_{GS}=0.0V and V_{DS}=8.0V. The difference with magnitude of seven orders in the current density of the 2DEG and the cap layer is seen. It should be noted that the drain leakage current is provided mostly by the buffer layer under the off-state conditions and this in agreement with the experiments [9].

Previous experiments have also shown that under the breakdown condition (V_{GS}=0.0V, V_{DS}=20.0V) most of the leakage current is provided by the GaN buffer between the source and the drain, but no drain-to-gate breakdown is observed. While our simulations does not currently account for impact ionization, the results in Fig. 6 clearly show, that as in conventional AlGaN/GaN structures, the maximum electric field is under the gate. No significant rise in the electric field in the n^{++} cap layer is observed, therefore, one can assume that this layer does not contribute to eventual gate-to-drain breakdown effects.

VI. CONCLUSION

We study current transport effects in the recessed n^{++} GaN cap layer in GaN/InAlN/AlN/GaN normally-off HEMTs. Our simulations confirm that the cap layer does not have a significant contribution to the on-state drain current. We also observe that it does not provide additional mechanism for gate-to-drain leakage under the off-state bias.

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