Strained MOSFETs on ordered SiGe dots

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ABSTRACT

The potential of strained DOTFET technology is demonstrated. This technology uses a SiGe island as a stressor for a Si capping layer, into which the transistor channel is integrated. The structure information of fabricated samples is extracted from atomic force microscopy (AFM) measurements. Strain on the upper surface of a 30 nm thick Si layer is in the range of 0.7%, as supported by finite element calculations. The Ge content in the SiGe island is 30% on average, showing an increase towards the top of the island. Based on the extracted structure information, three-dimensional strain profiles are calculated and device simulations are performed. Up to 15% enhancement of the NMOS saturation current is predicted.

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1. Introduction

Strain engineering as a means to enhance electronic device performance has become an integral part of contemporary CMOS technology. In addition, novel device architectures have been proposed to improve the way in which strain is induced in the device channel. Schmidt and Eberl suggested to use self-assembled SiGe islands as stressors for Si capping layers [1]. Thereby higher strain values can be reached as compared to strained Si grown pseudomorphically on relaxed SiGe buffers.

In this work, the process for growing self-organized SiGe islands is briefly described, followed by an experimental and theoretical assessment of the strain into the capping layer, and a prediction of the performance enhancement of n-type FETs integrated in the strained capping layer by means of three-dimensional device simulation.

2. Growth of regular arrays of SiGe islands

The growth procedures are described in detail in [2,3]. The samples were grown on a Si(0 0 1) substrate, on which a square pattern of pits with a period of 800 nm has been defined by e-beam lithography, and transferred by reactive ion etching to form pits with a width of 170 nm and a depth of 75 nm. A 36 nm thick Si buffer layer was deposited on the pit-patterned substrates by molecular beam epitaxy, while the substrate temperature was ramped from 450 °C to 550 °C. Then the substrates were heated to a growth

temperature of 720 °C, at which six mono-layers of Ge were deposited to form one dome-shaped SiGe island per pit. A Si capping layer of 30 nm thickness was deposited after cooling the substrate to 360 °C in order to avoid intermixing between the SiGe island and the Si cap. The surface morphology was investigated after each growth step by atomic force microscopy (AFM). Fig. 1 shows the AFM image of the final surface of the Si cap, which actually conformally replicates the surface after formation of the SiGe islands. Line scans across several pits and across a single pit are shown in Fig. 2, crossing the center of the pits and buried SiGe islands.

## 3. Modeling of the strain field in the DOTFET process

The processes of substrate patterning and SiGe island growth have been optimized with respect to subsequent device fabrication. Excellent island ordering, as well as island shape, size, and composition uniformity have been achieved. This optimization has been supported by simulations. Three-dimensional AFM data have been directly imported into a finite element code for strain calculation. In particular, AFM data were taken both after the Si buffer growth (surface of the pit) and after Ge depositions. As compared to the ideal equilibrium shape of the islands as reconstructed from facet plots [4], the procedure used here includes more details of the actual structure such as edge rounding and the trench surrounding the island. In the elastic field calculations a Ge content profile in the island has been taken into account with an average Ge content of 0.3. In an iterative procedure the elastic energy is minimized. At the top of the island a higher Ge content is found, whereas at the lower interface the Ge content is reduced by

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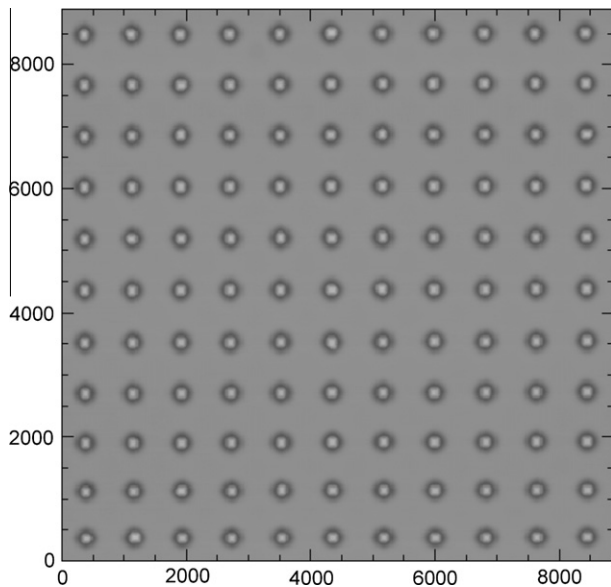
Fig. 1. AFM micrograph of the sample surface after 30 nm of Si cap has been deposited onto SiGe islands grown in pits of a prepatterned Si substrate.
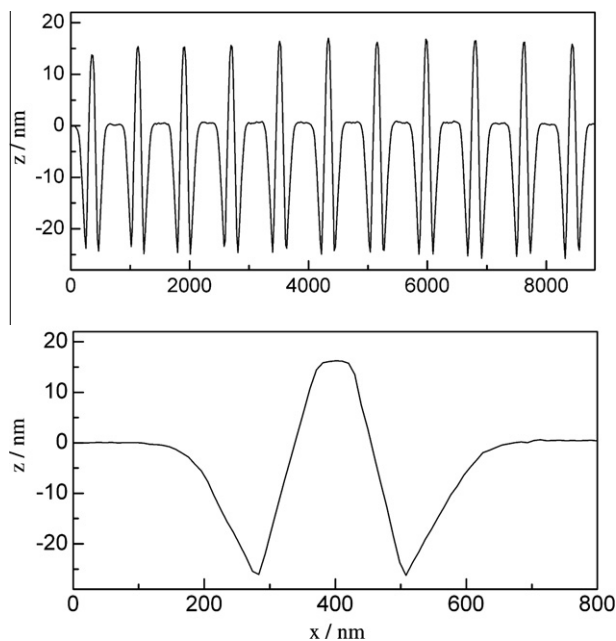
Fig. 2. AFM linescan across the islands indicates the excellent homogeneity of the island array (upper panel). The shape of the cap is shown with high resolution in the lower panel.

intermixing with the Si buffer layer. The Si capping layer is deposited at sufficiently low temperature to prevent any significant intermixing of the deposited Si with the SiGe island, so that Ge content profiles can be estimated prior to capping. Then in the whole structure including the capping layer the strain field is calculated using a finite-element code. The sample considered here shows up to 0.7% biaxial, tensile strain at the upper surface of the 30 nm Si capping layer, where the transistor channel will be integrated (Figs. 3–5). This value has also been confirmed by high-resolution X-ray diffraction [5] and Raman spectroscopy in conjunction with simulations [6].

Removing the SiGe island at some stage of the process, a silicon on nothing (SON) device architecture can be realized. In this work, however, we consider a process in which the island is preserved. In this case the thermal budget must be kept sufficiently low to prevent intermixing of Si and Ge between the Si capping layer and the SiGe island. This can be achieved by state-of-the art low-temperature processing, including low-temperature formation of the gate stack and laser annealing of the source/drain implants. A low-complexity, dedicated n-channel MOSFET process has been developed [7].

4. Three-dimensional device simulation

With the AFM data of the buffer and the SiGe island surfaces, the geometrical structure has been built. The Si capping layer is treated in the simulation by a conformal deposition. The correct representation of the Si cap is very important, since the simulated current is quite sensitive to the strain distribution at the surface. An unstructured mesh is used, which has to be sufficiently dense near the surface to resolve the surface inversion layer. On the other hand, in the SiGe island and the underlying Si buffer layer, lower point densities can be used.

4.1. Structure definition

The measured data is represented by z-values at defined xy-samples at the unstrained silicon surface, the surface of the dot, and the surface of the strained silicon regions. The tetrahedral mesher Netgen [8] is used for the three-dimensional mesh generation. This mesher features a robust meshing algorithm, which is able to handle the high aspect ratio of gate length/width to gate-oxide thickness. Input regions can be defined by a built-in solid modeler or by previously surface-meshed valid geometries. As the latter is not available in the measured data, a proper solid modeler geometry has to be built up from the existing data. Beside the usual primitives as tetrahedrons, bricks, and spheres, the solid modeler supports triangulated polyhedra. Therefore, several intermediate meshing stages have to be performed to achieve a proper input for the modeler.

In an initial step the xy-samples are two-dimensionally triangulated and the z-values are reassigned or interpolated to the delivered mesh points to achieve three-dimensional triangulated surfaces. As this mesh shows a huge number of surface elements, causing also a huge number of tetrahedral elements, an additional, adjustable smoothing stage was applied. Equipped with these data the solid modeler of Netgen was filled. To achieve a valid connectivity of the interfaces the following procedure is used (confer the final structure which is shown in Fig. 6 with the resulting mesh).

First, the most interesting segment, the strained silicon is provided by a triangulated polyhedron of its top and bottom surface. The dot is built by an extruded lower surface of the dot-samples with subtraction of the strained silicon. The gate oxide is built as a thin extruded strained silicon surface and subtraction of strained silicon. All other segments, which are the gate, the bulk, the source and the drain region, are built as a cuboid with subtraction of the former segments. By the use of this solid modeler methodology, the interfaces between the segments are properly connected.

Crucial for device simulation is the mesh density in the transistor channel. To achieve this desired high mesh density a maximum tetrahedron height for the mesh elements in the oxide region is assigned. Neighboring regions will start with these small elements growing towards the outer boundaries. With this technique an appropriate resolution in the channel region is achieved without boosting the overall number of tetrahedrons.

Characteristic data of the transistor are the gate stack consisting of a 1.5 nm thick oxide and a $60 \times 60\ nm^2$ polysilicon gate, a bulk contact is attached to the Si buffer layer, source and drain regions are 60 nm wide and the implants are approximated by analytical profiles. In Fig. 6 the final structure with the simulation mesh is
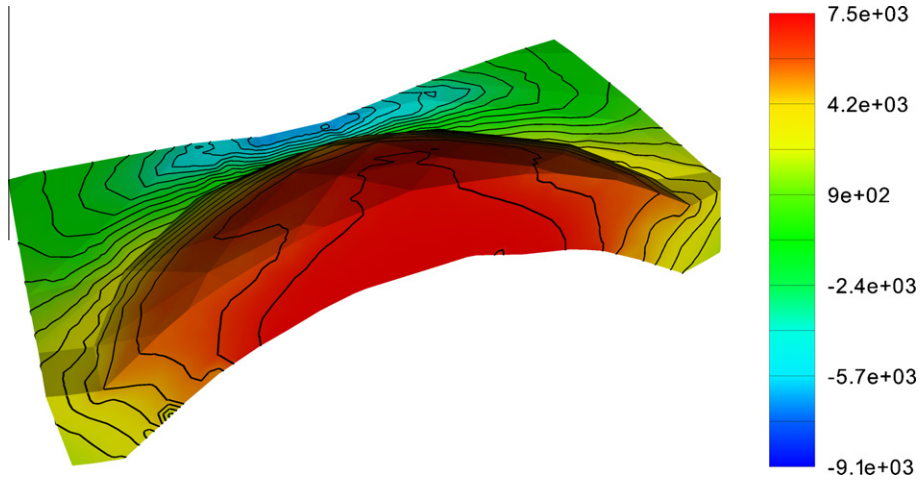
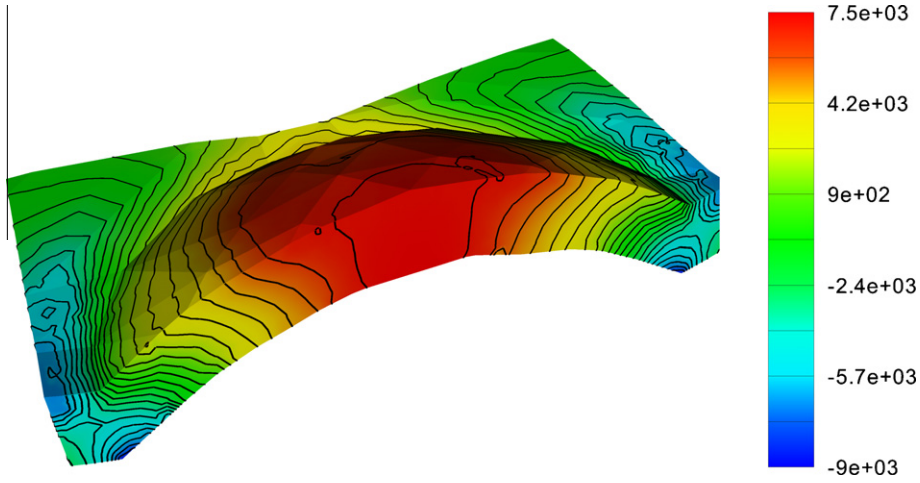**Fig. 3.** Strain component e_{xx} (channel length direction) in the Si capping layer.

Fig. 4. Strain component e_{yy} (channel width direction) in the Si capping layer.
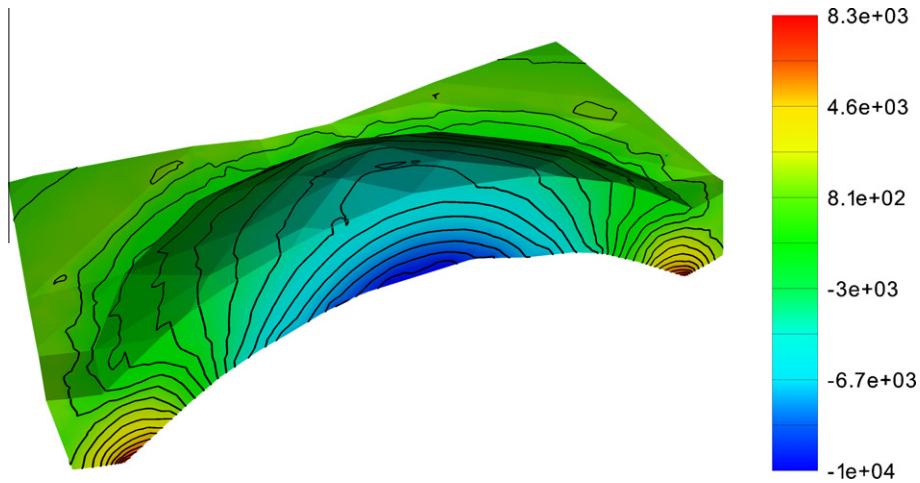

Fig. 5. Strain component e_{zz} (vertical direction) in the Si capping layer.

shown. The transistor is cut along its symmetry axis and only one half of the whole structure is analyzed.

In the Si cap layer a constant boron doping of 4×10^{18} cm^{-3} is assumed. Into the access regions to source and drain to the channel an arsenic profile with a maximum concentration of 5×10^{20} cm^{-3} is implanted (Fig. 7). Finally, the strain profile is interpolated from its originated ortho grid to the device simulation mesh. This mesh shows a high point density in the channel
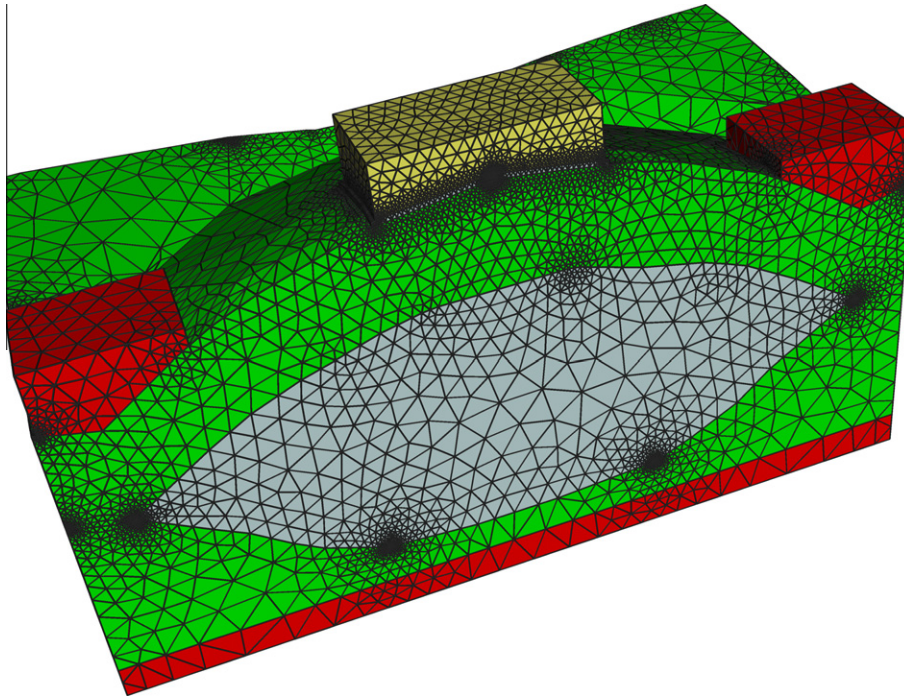
Fig. 6. The geometry of the generated transistor structure. Only one half of the transistor is simulated.
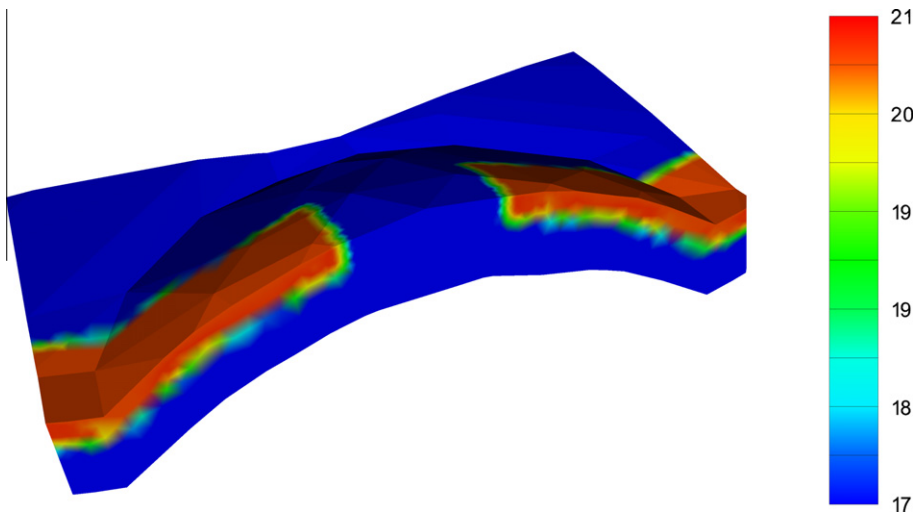
Fig. 7. The arsenic doping with shown pn-junction in the capping layer.

area. Therefore, the strain profile is well adapted in the active region.

4.2. Electrical characterization

Three-dimensional device simulations are performed using MINIMOS-NT [9]. The invoked physical models include the strain-dependent low-field mobility model described in [10] and the IMLDA quantum correction model [11]. To determine the strain-induced current enhancement, comparative simulations of the same structure are performed with and without taking the strain effect on the mobility into account.
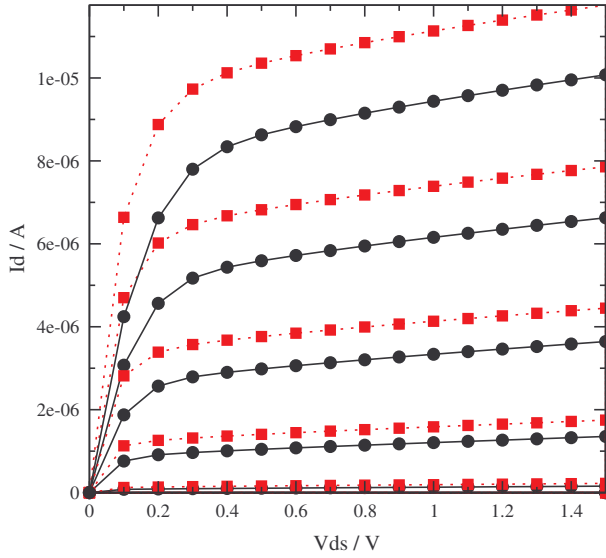
In Fig. 8 the output characteristics for the unstrained and strained device are depicted. The transfer characteristics for drain voltages of 0.05 V and 1.5 V can be seen in Fig. 9. Fig. 10 shows

the achieved drain current enhancement I_D/I_D^* (strained to unstrained drain current) as a function of the drain voltage. The current enhancement declines with growing gate voltage. Due to saturation of the electron velocity the enhancement also decreases towards higher drain voltages. At $V_{GS} = 1.5$ V and $V_{DS} = 1.5$ V an enhancement of 15% can be evaluated.
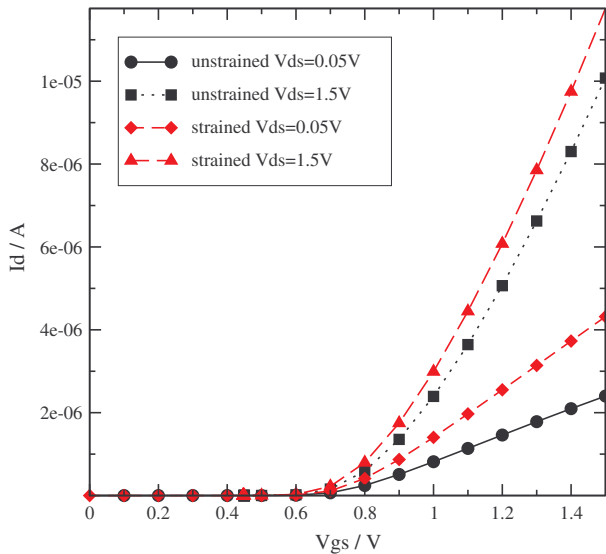
4.3. Three-dimensional impact of the dot

To examine the influence of the three-dimensional structure properties on the device characteristics the device has been cut along the channel axis. Depending on the position of the cut two-dimensional simulations were performed. On one hand side the stress profile varies towards lower stress values and on the other hand side the curvature and channel length decreases in

Fig. 8. The unstrained (black bullets) and strained (red squares) output characteristics for gate voltages of 0.7 V, 0.9 V, 1.1 V, 1.3 V, and 1.5 V are shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
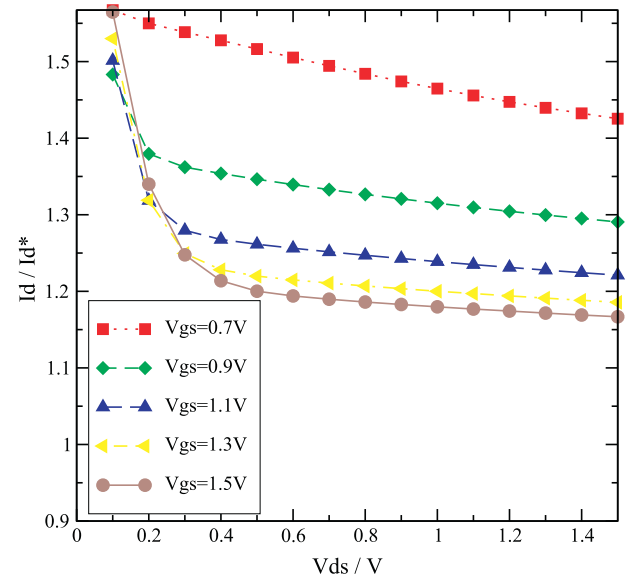

Fig. 10. The current enhancement I_D/I_D^* for several gate voltages.

Fig. 9. The unstrained and strained transfer characteristics for drain voltages of 0.05 V and 1.5 V.

Fig. 11. Current enhancement at a lateral cut of the original structure in dependence of the cut coordinate.

the regions remote of the center plane. The result can be seen in Fig. 11. Here again the current enhancement I_D/I_D^* in dependence of the cut coordinate for V_{GS} = 1.5 V and V_{DS} = 1.5 V is plotted.
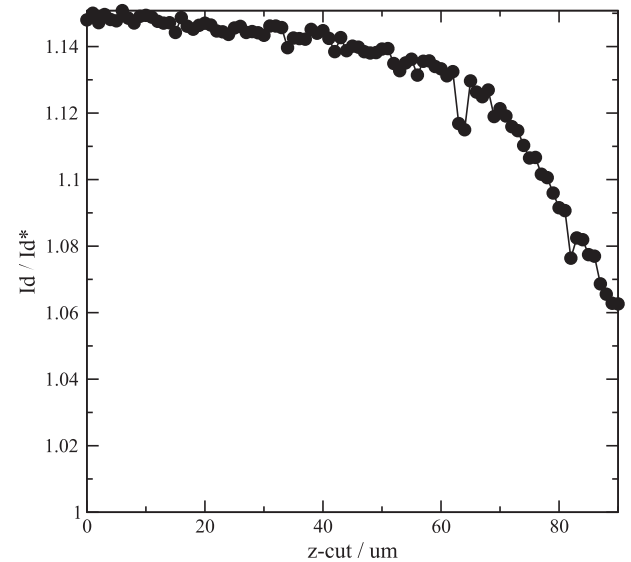
4.4. Comparison with an SOI structure

The DOTFET with removed SiGe dot has the electrostatic benefits of an SOI transistor. Due to the thermic problems arising in SOI technology this DOTFET structure is compared with an SOI structure. To have a comparable structure three different scenarios had been chosen, all based on the original device geometry, where different segments had been replaced by other materials:

- The original structure: consisting of the strained silicon bridge, the germanium dot, and the unstrained silicon buffer.

- The Silicon On Nothing structure: the germanium dot is etched away and (for simulation) replaced by air, which also can be produced by a modified process.
- The Silicon On Insulator structure: the unstrained silicon pit is replaced by insulator. This artificial geometry has been chosen to have the same geometry of the active areas, the same doping, the same channel oxide, and the same gate influence.

If self heating is included, the thermal heat produced in the channel region of the original structure can be diverted through the silicon bridge, the germanium dot and the unstrained silicon region. Even with the dot removed the heat is diverted relatively good through the silicon bridge and the unstrained silicon region. However, for the SOI structure the thermal conductivity of the silicon buffer layer disappears. The heat has to be diverted through the contacts and surrounding insulators. The results of the simulation at V_{GS} = 1.5 V and V_{DS} = 1.5 V can be seen in Figs. 12–14.
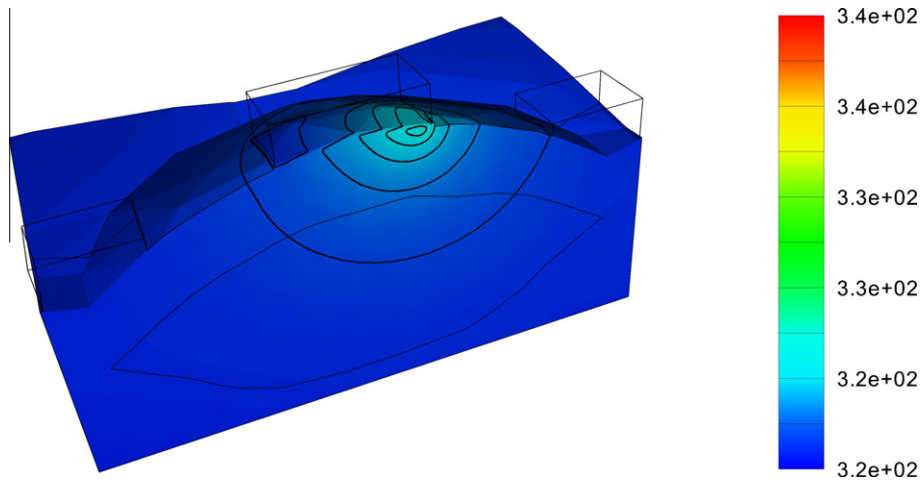
Fig. 12. Temperature distribution at the original DOTFET structure with the germanium dot.
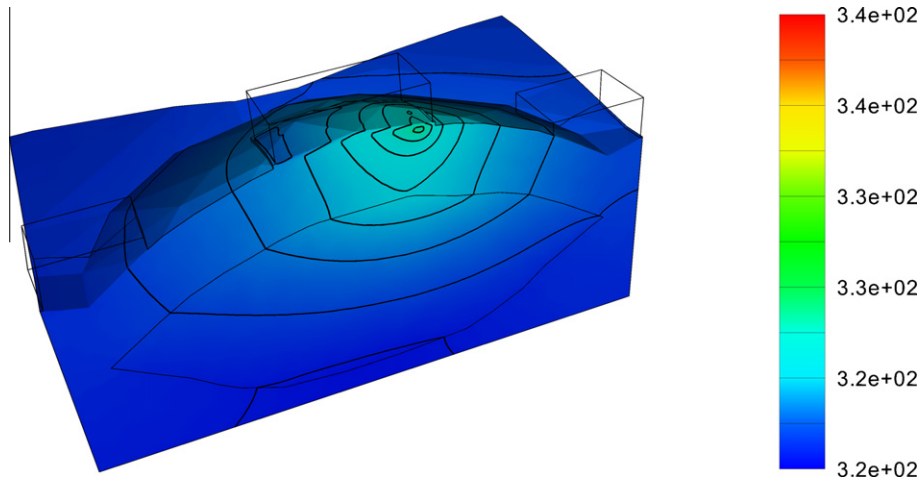
Fig. 13. Temperature distribution at the SON device with removed germanium dot.
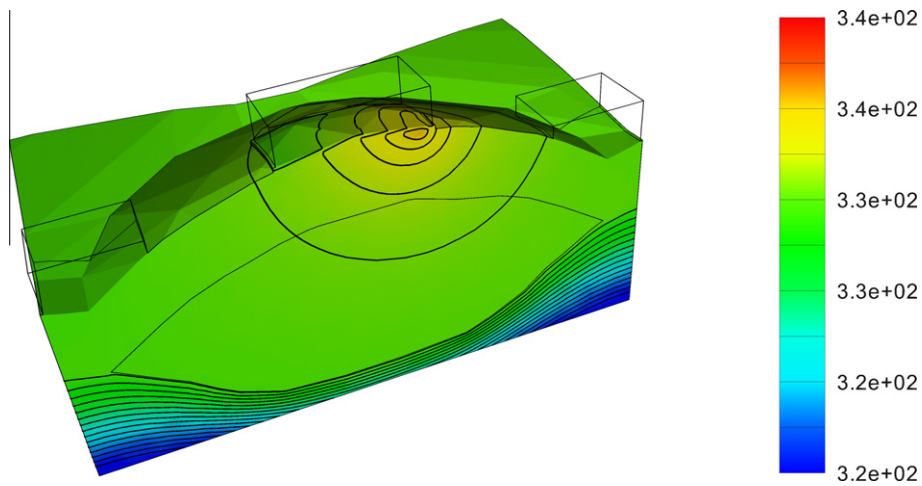
Fig. 14. Temperature distribution at the SOI device with oxide instead of the unstrained silicon region.

Removing the dot only marginally changes the temperature profile. Only in air the profile varies, but in the active regions the temperature peak is nearly unaffected. Without the unstrained segment a dominant increase of the temperature in the channel region can be observed. This effect will also have significant influence on the mobilities and on impact ionization.

5. Discussion

In this section we compare the DOTFET structure with the so-called *Reverse Embedded SiGe structure* proposed by IBM in 2006 [12]. In the latter structure, strain is induced by elastic relaxation of a Si/SiGe bilayer. Source and drain are grown by selective epitaxy. We performed a strain calculation of the IBM structure and found a rather non-uniform strain profile with the strain maximum located in the middle of the channel. In [12] a uniaxial strain of 0.24% in the Si channel and a related drive current improvement of 15% are reported.

In comparison, the DOTFET process induces a more uniform strain up to 0.7% in the Si channel. The DOTFET structure is integrated in the coherently grown Si capping layer. Our simulations predict for the DOTFET the same drive current enhancement as has been reported for the IBM process, despite the strain in the latter is about three times lower (0.24% versus 0.7%). This can be partly attributed to different extraction methods for the current enhancement used in [12] and in our simulations. This comparison also indicates that the parameters used in our simulations give a conservative estimate of the current enhancement of the DOTFET.

6. Conclusion

In this work the potential of the DOTFET has been studied by three-dimensional simulations. The geometry has been extracted from actually fabricated samples. The strain field is obtained by comprehensive simulations verified by strain measurements on the strained Si layer. A conservative estimate for the NMOS drive current enhancement of about 15% is obtained.

Acknowledgment

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