Modeling of Electromigration Induced Resistance Change in Three-Dimensional Interconnects with Through Silicon Vias

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***Abstract*—Electromigration (EM) is one of the main reliability concerns in copper interconnects. In particular, it is a critical issue for new emerging technologies, such as through silicon via (TSV) technology. In this work the impact of formation and growth of voids under a TSV located at the cathode end of a typical dual-damascene line is analyzed. The resistance change of the structure is numerically simulated and modeled. It is shown that there exist two modes of resistance development caused by large and small voids.**

I. Introduction

Three-dimensional (3D) integration has become a very promising technology for the microelectronics industry. Among its main advantages are: high density integration, multifunctionality, better performance, reduced power, heterogeneous integration, etc [1]. One key component of 3D integration to achieve these features is the through silicon via (TSV) [2]. A TSV consists of a conducting via fabricated trough a silicon substrate, which connects components of different integration levels [1].

Reliability is a critical issue for new emerging technologies, in particular, for TSVs [3]. Electromigration (EM) is one of the main reliability concerns in back-end of line (BEOL) interconnects.

EM failure mechanisms have been extensively studied in copper dual-damascene interconnects [4]. Frank *et al.* [5] have shown that for structures with a TSV formed on a pad at the cathode end of line the resistance development is somewhat different than that for conventional line-via structures. They have observed that the resistance remains initially constant and later increases following a logarithmic time dependence. Based on failure analysis methods it was shown that this behavior is due to the growth of a large void under the TSV and it was concluded that this is the major failure mechanism in such structures.

In this work we investigate the impact of small and large voids on the structure resistance development. The resistance change is determined based on 3D numerical simulations. We show that a significant resistance increase can also be caused by small voids under the TSV, since imperfections at the TSV bottom are introduced from the fabrication process. This forms an additional failure mechanism, for which an analytical model is developed.

II. Modeling

In [5] EM experiments using downstream electron flow showed void formation and growth under the TSV at the cathode end of a line as sketched in Fig. 1 and Fig. 2. It was observed that the development of the resistance as a function of time can be divided in two periods: at first the resistance remains practically constant, which is then followed by a measurable resistance increase. Failure analysis indicated that during the first period the void diameter is smaller than the TSV section, while the measurable resistance increase period starts as soon as the void diameter becomes larger than the TSV section.

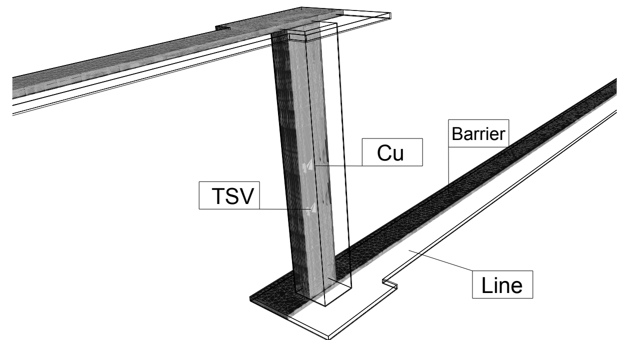

Fig. 1. Copper dual-damascene line/TSV structure.

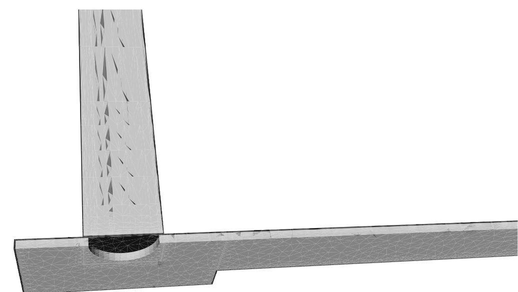

Fig. 2. Detail of the TSV bottom and void under the via.

Considering a cylindrical void with radius r_{void} under the TSV, as shown in Fig. 2, and that $r_{void} \geq r_{TSV}$, the resistance change is modeled as [5]

$$R(r_{void}) - R(r_{TSV}) = \frac{\rho_b}{2\pi t_b} \ln\left(\frac{r_{void}}{r_{TSV}}\right),\ r_{void} \geq r_{TSV}, \quad (1)$$

where r_{void} and r_{TSV} are the void and the TSV radii, respectively, ρ_b is the barrier resistivity, and t_b is the barrier layer thickness at the bottom of the via. $R(r_{TSV})$ is the resistance at $r_{void} = r_{TSV}$. The total resistance change is then given by

$$\Delta R(r_{void}) = R(r_{TSV}) - R_0 + \frac{\rho_b}{2\pi t_b} \ln\left(\frac{r_{void}}{r_{TSV}}\right), \quad r_{void} \geq r_{TSV}. \quad (2)$$

Although Frank *et al.* [5] assumed that the resistance change is negligible while $r_{void} < r_{TSV}$, void growth under the TSV leads, in fact, to a small resistance increase which cannot be experimentally measured. In this case, the resistance change is caused by the reduction of the effective conducting area in relation to the cross sectional area of the TSV. In absence of voiding, the conduction area through the barrier layer is equal to the to the cross sectional area of the TSV, πr_{TSV}^2. In the presence of a void, the effective conduction area becomes $\pi r_{TSV}^2 - \pi r_{void}^2$. Therefore, the resistance change is given by

$$\Delta R(r_{void}) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left[\frac{(r_{void}/r_{TSV})^2}{1-(r_{void}/r_{TSV})^2}\right],\ r_{void} < r_{TSV}, \quad (3)$$

which suggests a rapid resistance increase as the void radius approaches the TSV one.

Assuming that the void volume is formed by capturing vacancies driven by the electromigration force and that the vacancy flux is constant, the volume of a cylindrical void at a time t is given by [5]

$$V_{void}(t) = \pi h r_{void}^2(t) = A_l\ v_d\ t, \quad (4)$$

where h is the copper line thickness, A_l is the line cross sectional area, and v_d is the vacancy drift velocity. Thus, for isotropic void growth the void radius as a function of time is written as

$$r_{void}(t) = \sqrt{\frac{A_l\ v_d}{\pi h} t}. \quad (5)$$

Since the vacancy drift velocity is given by [6]

$$v_d = \frac{D_v e Z^* \rho j}{kT}, \quad (6)$$

where D_v is the vacancy diffusivity, eZ^* is the effective charge, ρ is the copper resistivity, j is the applied current density, k is the Boltzmann's constant, and T is the temperature.

The resistance change as a function of time is obtained by combining eq. (2), eq. (5), and eq. (6) yielding

$$\Delta R(t) = R(r_{TSV}) - R_0 + \frac{\rho_b}{4\pi t_b} \ln\left(\frac{t}{t_0}\right),\ t \geq t_0, \quad (7)$$

with

$$t_0 = \frac{\pi h r_{TSV}^2}{A_l v_d} = \frac{\pi h r_{TSV}^2 kT}{A_l D_v e Z^* \rho j}. \quad (8)$$

t_0 is the time at which the void radius becomes equal to the radius of the TSV and the logarithmic resistance increase starts [5]. Thus, eq. (7) is valid for the period $t \geq t_0$, which corresponds to $r_{void} \geq r_{TSV}$.

Similarly, the combination of eq. (3), eq. (5), and eq. (6) leads to the resistance change with time given by

$$\Delta R(t) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left[\frac{(t/t_0)}{1-(t/t_0)}\right],\ t < t_0, \quad (9)$$

for small voids under the TSV, i.e. $r_{void} < r_{TSV}$.

Eq. (7) and eq. (9) describe the resistance change for large and small voids, respectively. If the maximum allowed resistance change ΔR_c is reached for a sufficiently large void ($r_{void} > r_{TSV}$), the interconnect TTF is determined by eq. (7). In turn, if a small void ($r_{void} < r_{TSV}$) can produce a significant resistance increase, the failure time is governed by eq. (9).

Frank *et al.* [5] have analyzed EM failures based on eq. (7). However, the rapid resistance change predicted by eq. (3) indicates that it is possible that ΔR_c is reached for a smaller critical void, which implies a shorter time to build it, given by eq. (9). These early failures form an additional extrinsic mode which is critical for a correct assessment of the reliability of these interconnect structures.

The models derived above assume a circular TSV, while the via used in the experimental test structure described in [5] and used in this work is approximately square. Therefore, r_{TSV} should be viewed as an effective via radius. This does not fundamentally affect the modeling and later we will show that r_{TSV} can be determined by fitting eq. (1) and eq. (3) to the curves of resistance change as a function of void radius obtained from numerical simulations.

III. Results and Discussion

The resistance change caused by the growth of a void located under the TSV was determined from numerical simulations. The geometry, dimensions, and material parameters of the interconnect structure were obtained from [5]. A detailed view of the structure and void at the TSV bottom is shown in Fig. 2.

Considering the modeling approach described above, a cylindrical void is placed under the via and its radius is gradually incremented. For each void size the resistance of the interconnect is determined from the numerical solution of the Laplace equation. In this way we are able to extract the resistance change of the interconnect shown in Fig. 1 for the whole period of void growth.

Fig. 3 shows the electron current density distribution at the TSV bottom in the presence of a void. The void causes a reduction of the effective conducting area at the TSV bottom. The electron flow is displaced towards the corners of the via, which leads to current crowding in this region, as can be readily seen in Fig. 3.

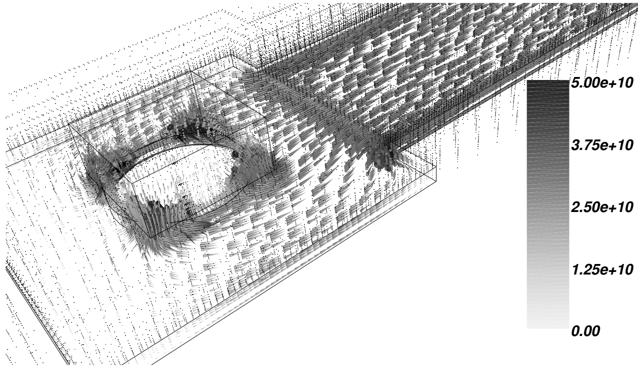

Fig. 3. Electron current density distribution (in A/m^2) under the TSV in the presence of a void. Current crowding towards the corners of the via can be seen.

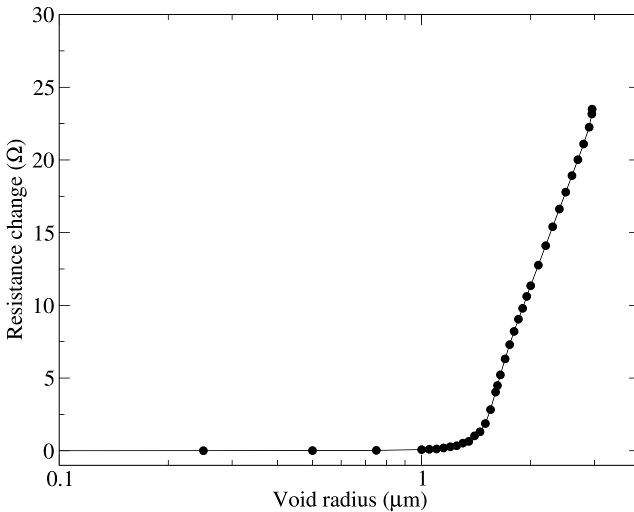

Fig. 4. Numerical simulation of resistance change as a function of void size under the TSV.

The resistance change as a function of void radius is shown in Fig. 4. The resistance change is practically negligible for small void radii ($r_{void} < r_{TSV} = 1.4\ \mu$m). For larger voids, however, a significant resistance increase is observed. Note that the void radius axis is plotted in logarithmic scale and that the resistance appears to closely follow a linear increase in this scale. Below we investigate the resistance change curve shown in Fig. 4 in more detail and verify the modeling previously proposed.

A. Resistance change for large voids ($r_{void} \geq r_{TSV}$)

The resistance change of the interconnect line as a function of the void radius for the range $r_{void} \geq r_{TSV}$ is shown in Fig. 5. The symbols represent numerical simulation results obtained for different void sizes. The solid line is a fit to the simulated data according to the model given in eq. (1). The model correctly describes the resistance change for the tested void radius range. Furthermore, the numerical simulation results reproduce the logarithmic resistance increase

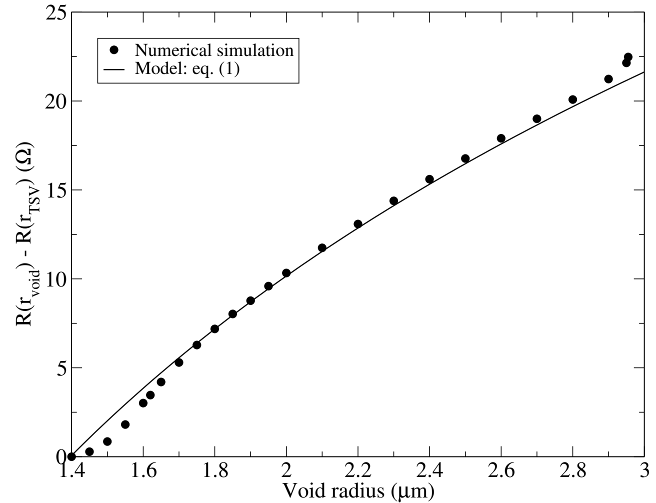

Fig. 5. Interconnect resistance change as a function of void radius for $r_{void} \geq r_{TSV}$.

suggested by Frank *et al.* [5]. By fitting eq. (1) to the numerical simulation results we have obtained as effective TSV radius $r_{TSV} = 1.44\ \mu$m.

B. Resistance change for small voids ($r_{void} < r_{TSV}$)

The simulated resistance change as a function of void size for $r_{void} < r_{TSV}$ is shown in Fig. 6. Although the magnitude of the resistance change is small, a rapid increase is expected as the void grows. A very good agreement between the numerical simulations and the analytical model given by eq. (3) is obtained for the range $r_{void} \leq 0.95\ r_{TSV}$. The estimated effective TSV radius is $r_{TSV} = 1.43\ \mu$m, which is very close to the value previously determined for the large void case.

Since the resistance increase for $r_{void} < r_{TSV}$ is rather small, EM failures are, in principle, expected to occur for critical void radii in the range $r_{void} > r_{TSV}$ [5], so the interconnect lifetime is obtained from eq. (7). However, imperfections on the bottom of the TSV are typically introduced during the fabrication process [7]. In particular, control of the thin barrier layers at the bottom of the TSV is a key issue and has a significant impact on the structure reliability.

As a consequence of these imperfections, Frank *et al.* [5] observed a high variation of the barrier layer resistivity (100 – 20000 $\mu\Omega$·cm) estimated from the experimental results, as shown in Fig. 7. Thus, the barrier resistivity distribution can be regarded as an effective parameter which takes into account mainly the dispersion of the barrier layer thickness of the TSV bottom.

The impact of such variations on the resistance change due to a small void under the TSV for different values of barrier resistivity is shown in Fig. 8. The variation of the effective barrier resistivity affects the structure resistance significantly, leading to a large resistance increase, even when the void size is still smaller than the via section. Taking a

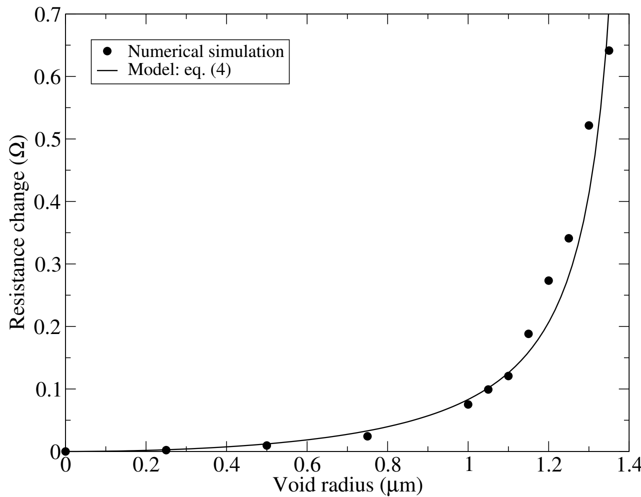

Fig. 6. Resistance change as a function of void radius for small voids ($r_{void} < r_{TSV}$).

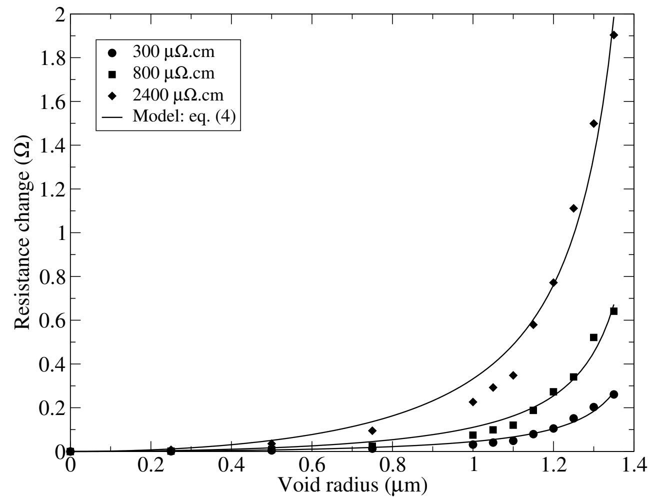

Fig. 8. Resistance change due to a small void under the TSV for different values of barrier resistivity.

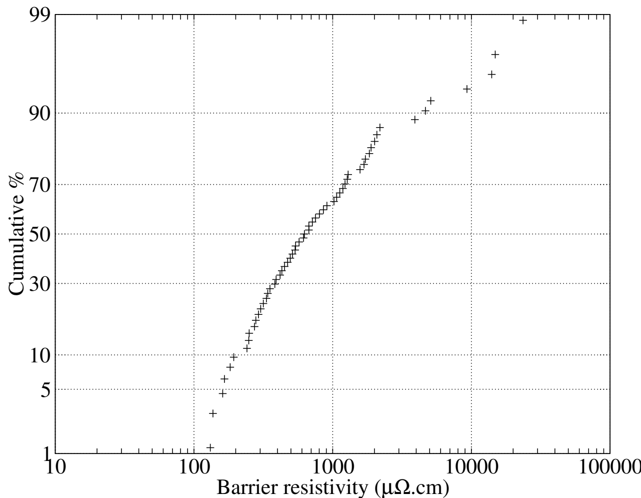

Fig. 7. Barrier resistivity distribution extracted by Frank *et al.* [5]. The large dispersion indicates the existence of imperfections at the TSV bottom introduced during the fabrication process.

10% resistance increase as failure criterion, we estimate that for $\rho_b \gtrsim 3000$ $\mu\Omega$·cm the interconnect failure is triggered also for smaller voids under the TSV ($r_{void} < r_{TSV}$). It should be pointed out that these failures form an additional failure mode. Furthermore, since a shorter time is needed to grow a smaller void, this failure mechanism constitutes an early failure mode.

Fig. 7 shows that a high barrier resistivity is found at a cumulative percentile of about 90%. This means that early failures would only be "visible" in lifetime distribution curves for low cumulative percentiles, in particular less than 10%. Considering that the reliability assessment of an interconnect is typically performed at very low failure percentiles, the early failures described above might be the main relevant mechanism for EM failure in copper dual-damascene line/TSV structures.

IV. Conclusion

Small voids under the via of a copper dual-damascene line/TSV structure generated by EM material transport can cause a significant interconnect resistance increase due to imperfections at the TSV bottom. Upon triggering the line failure, this mechanism forms an extrinsic, early failure mode, which acts primarily at low cumulative percentiles, and is expected to have a significant impact on the interconnect reliability assessment. A model which satisfactorily describes the resistance increase associated to this mode has been proposed.

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