Design and Applications of Magnetic Tunnel Junction Based Logic Circuits

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***Abstract*—By offering zero standby power, non-volatile logic is a promising solution to overcome the leakage current issue which has become an important obstacle, when CMOS technology is shrunk. Magnetic tunnel junction (MTJ)-based logic has a great potential, because of unlimited endurance, CMOS compatibility, and fast switching speed. Recently, several non-volatile MTJ-based circuits have been presented which inherently realize logic-in-memory circuit concepts by using MTJ devices as both memory and the main computing elements. In this work we present a reliability simulation method for designing MTJ-based logic gates integrated with CMOS. As an application example, we study the reliability of a magnetic full adder in two different designs based on the implication and the reprogrammable MTJ logic gates.**

***Index Terms*—Logic-in-memory, material implication (IMP), magnetic tunnel junction (MTJ), non-volatile logic, spin transfer torque (STT)**

I. Introduction

High standby power due to leakage currents has become an important obstacle for scaling CMOS logic circuits (Fig. 1) at sub-100nm technologies [1]. A possible solution to overcome this problem is introducing non-volatility into the logic circuits [2]. The Spin-transfer torque (STT) [3] switching magnetic tunnel junction (STT-MTJ) is one of the most promising non-volatile storage technologies, which combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability [4].

As shown in Fig. 2, distributing non-volatile memory elements over the CMOS logic circuit plane (so-called logic-in-memory architecture [5]) can provide extremely low standby power consumption and instant start-up by holding the information in the MTJs and eliminating the need for refreshing pulses which are critical for CMOS-based memory elements [6], [7], [8]. Furthermore, by using the MTJ technology the effective area and interconnections delay (the data traffic on a main data bus between separated logic and memory modules as shown in Fig. 1) can be reduced due to easy three-dimensional integration of the MTJs on top of the CMOS layers (Fig. 2). However, in hybrid CMOS/MTJ circuits the MTJs are used only as ancillary devices which store the computation results [9]. Therefore, sensing amplifiers [10] are required for reading the data at each logic stage and providing the next stage with an appropriate voltage or current signal as input. This limitation increases the device count, delay, and power consumption. Furthermore, the generalization to large-scale logic systems is problematic.

Recently, it has been demonstrated that STT-MTJs can be directly connected to perform logic operations [11], [12], [13], intrinsically enabling logic-in-memory architectures with no need for extra hardware (also known as "stateful" logic [14]). Here, we show how the MTJ logic gates can be generalized to large-scale logic systems based on one-transistor/one-MTJ (1T/1MTJ) cells (Fig. 3b) which are utilized as the basic memory cells in the STT magnetoresistive random-access memory (STT-MRAM) structure [15].

II. Intrinsic MTJ-based Logic-in-Memory

The MTJ device includes a fixed and a free ferromagnetic layer separated by an oxide barrier as shown in Fig. 3a. The magnetization of one layer is pinned (reference layer), while the magnetization of the other layer (free layer) can be switched freely using an external magnetic field or the STT effect. The STT switching technique improves significantly its scalability and the STT-MTJ exhibits pure electrical switching [4]. The MTJ resistance depends on the relative orientation of the magnetization directions of the ferromagnetic layers.

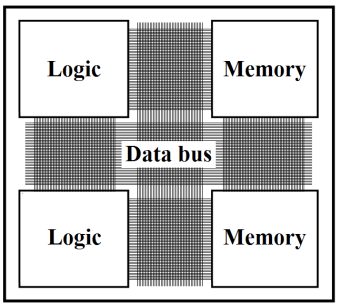

Fig. 1. Separated logic and memory units in a two-dimensional structure of CMOS logic. The interconnections delay dominates chip performance. The continuously powered memory units cause large static power consumption due to the leakage currents.

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The (anti)parallel alignment results in a low (high) resistance state across the barrier R_{P} (R_{AP}), which is mapped to logic '0' ('1'). The resistance modulation is described by the tunnel magnetoresistance (TMR) ratio, defined as $(R_{\mathrm{AP}} - R_{\mathrm{P}})/R_{\mathrm{P}}$.

The non-volatile magnetic logic-in-memory concept (Fig. 2) has been recently tested as a potential candidate for logic circuit design. For example, a magnetic full adder has been demonstrated in [6] for non-volatile arithmetic applications. However, the logic operation is still performed by CMOS logic elements, which requires 26 transistors for logic, 8 for MTJ writing, and 4 MTJs. Therefore, there is no benefit regarding the transistor count compared to the CMOS full adder. Furthermore, a key limitation of this magnetic full adder is the necessity of different kind of inputs and outputs for which some inputs or outputs are voltage signals, whereas the others are the resistance state of the MTJ elements. This mismatch causes the need for extra hardware and increases complexity.

Recently, MTJ-based logic gates have been demonstrated which use MTJs as main devices for logical computations and intrinsically enable logic-in-memory architectures with no need for extra hardware. In fact, in a logic mode the MTJs are used as the basic elements for computations and in a memory mode they are used for non-volatile storage. This enables extending non-volatile electronics from memory to logical computing applications and eliminates the need for sensing amplifiers and intermediate circuitry as compared to the hybrid CMOS/MTJ non-volatile logic circuits.

In [11] and [12], STT-MTJ-based reprogrammable logic gates (Fig. 4a and Fig. 4b) are demonstrated to realize the conventional Boolean logic operations including AND, OR, NAND, and NOR. By applying the voltage V_{A}, the resistance states of the input MTJs modulate the critical current required for the STT-switching of the output MTJ. In [13], we proposed a STT-MTJ-based implication logic gate (Fig. 4c) to realize a fundamental Boolean logic operation called material implication (IMP). Depending on the initial logic (resistance) states of the source and the target MTJs a conditional switching behavior on the target MTJ is provided, when the current I_{IMP} is applied to the IMP gate. The final logic state of the target MTJ represents the logical output of the IMP operation. By replacing the MTJ devices with 1T/1MTJ cells (Fig. 4d), the IMP logic gates can be extend to large-scale non-volatile magnetic circuits. Since the 1T/1MTJ cell is the basic element for STT-MRAMs, this concept provides magnetic logic circuits which also can be used for random-access memory applications (Fig. 5). In the next section we present a method for reliability analysis of the MTJ-based logic circuits and we consider in particular the reliability of a magnetic full adder.

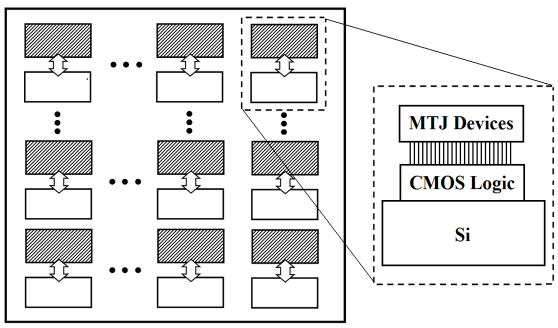

Fig. 2. Logic-in-memory architecture and the three-dimensional structure of the magnetic logic circuits.

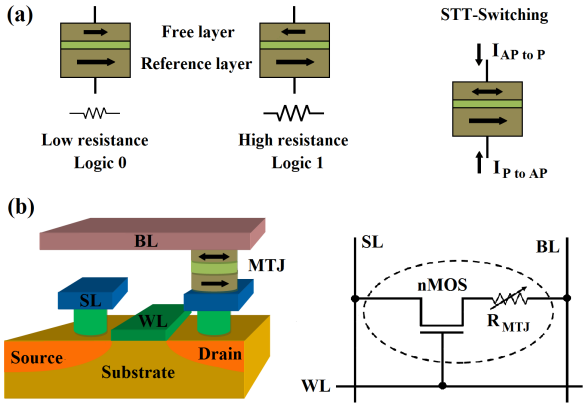

Fig. 3. (a) MTJ basic structure. (b) 1T/1MTJ structure and the equivalent circuit diagrams.

III. Modeling and Results

The realization of MTJ-based intrinsic logic-in-memory circuits relies on a conditional STT-switching behavior of the output (target) MTJ for each logic operation. It has been shown that a reliable MTJ-based logic behavior requires a high enough TMR ratio [13]. A typical 1T/1MTJ memory cell of the STT-MRAM structure consists of an access transistor and a MTJ as its storage element (Fig. 3b). The access transistor acts as on/off switch to control the current flowing through the MTJ. When a selecting voltage signal (V_{s}) is applied to a word line (WL), the current $I_{\mathrm{AP-P}}$ ($I_{\mathrm{P-AP}}$) applied to the bit line (BL) switches the MTJ (corresponding to the selected access transistor by the WL) from AP to P (P to AP) state.

For the reliability analysis of the intrinsic logic-in-memory circuits, it can be shown that the reliability of a specific logic function (f) is determined by

$$R(f) = 1 - P_{\mathrm{err}}(f) = \prod_{i=1}^{n_{\mathrm{f}}} [1 - P_{\mathrm{err}}(i)], \qquad (1)$$

where $P_{\mathrm{err}}(i)$ is the average error probability of the i^{th} MTJ-based logical step and n_{f} is equal to the total number of the MTJ-based operations (conditional switching evens) required for performing f using either implication or reprogrammable gates. For example, a NAND-based design of a full adder using the reprogrammable gate includes 9 NAND operations ($n_{\mathrm{f}} = 9$). Our design for an IMP-based full adder includes 18 IMP operations ($n_{\mathrm{f}} = 18$) [16].

For a basic logic operation using MTJ gates, $P_{\rm err}$ is proportional to the sum of the switching probabilities for undesired switching events ($P_{\rm u}$) and the term $(1-P_{\rm d})$ for the desired switching events as [13]

$$P_{\rm err}=\frac{1}{k+h}\left\{\sum_{i=1}^{k}P_{\rm u}(i)+\sum_{j=1}^{h}1-P_{\rm d}(j)\right\}, \quad (2)$$

where k and h are the number of the possible undesired and desired switching events. According to the theoretical model [17] and the measurements [15], the switching probability (P) of an MTJ in the thermally-activated switching regime (switching time $t>10$ ns) is given by

$$P=1-\exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I}{I_{\rm C0}}\right)\right]\right\}, \quad (3)$$

where $\Delta_0=E/k_{\rm B}T$ is the MTJ thermal stability factor, I is the current flowing through the MTJ, t is the current pulse duration, $\tau_0\sim 1$ns, and $I_{\rm C0}$ is the critical switching current extrapolated to τ_0 [18].

In order to calculate the current passing through the MTJs in the 1T/1MTJ-based gate (Fig. 4d), we have

$$\begin{aligned}&V_{\rm GS}^{\rm i}=V_{\rm WL},\\ &V_{\rm GS}^{\rm j'}=V_{\rm WL},\\ &V_{\rm DS}^{\rm i}=V_{\rm BL}-V_{\rm M}^{\rm i}=V_{\rm BL}-R_{\rm M}^{\rm i}I_{\rm M}^{\rm i},\\ &V_{\rm DS}^{\rm j'}=V_{\rm BL}-R_{\rm G}I_{\rm M}^{\rm j'}-V_{\rm M}^{\rm j'}=V_{\rm BL}-(R_{\rm G}+R_{\rm M}^{\rm j'})I_{\rm M}^{\rm j'},\end{aligned} \quad (4)$$

when the current $I_{\rm IMP}$ is applied and the target and the source cells are selected by a voltage $V_{\rm WL}$ applied to the $i^{\rm th}$ and $j'^{\rm th}$ word lines (WLi and WLj'), respectively. Here, $V_{\rm GS}$ ($V_{\rm DS}$) is the voltage difference between the gate (drain) and the source of the access transistor, $R_{\rm M}$ is the MTJ resistance, and $I_{\rm M}$ is the current through the MTJ device.

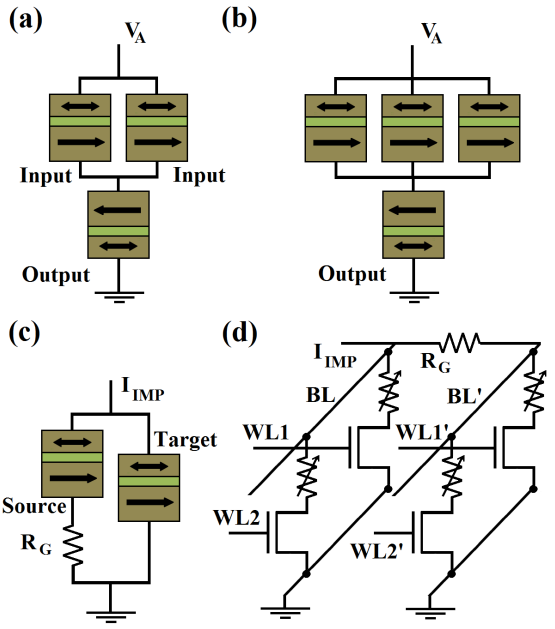

Fig. 4. Reprogrammable two-input (a) and three-input (b) MTJ-based logic gates [11], [12]. (c) Current-controlled MTJ-based implication logic gate [13]. (d) 1T/1MTJ-based IMP logic circuit.

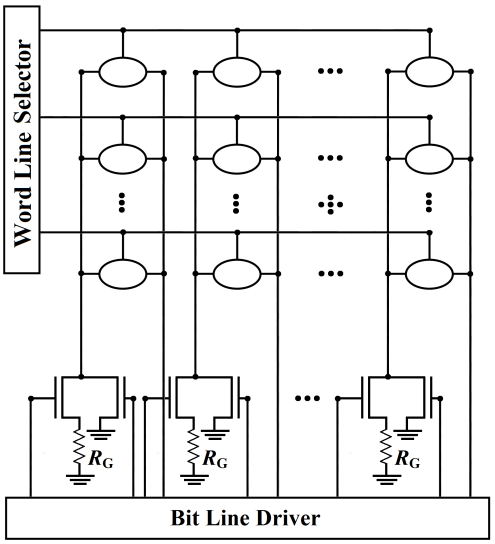

Fig. 5. The magnetic logic circuit based on the STT-MRAM architecture [13] with 1T/1MTJ cells (Fig. 3b) to realize intrinsic logic-in-memory for large-scale logic applications.

The $R-V$ characteristics of the MTJ device is determined by the voltage-dependent effective TMR model [19], if the MTJ is in the antiparallel state, as

$$R_{\rm M}=R_{\rm AP}=(1+{\rm TMR}_{\rm eff})R_{\rm P}=(1+\frac{{\rm TMR}_0}{1+\frac{V_{\rm M}^2}{V_{\rm h}^2}})R_{\rm P}, \quad (5)$$

where ${\rm TMR}_0$ (${\rm TMR}_{\rm eff}$) is the TMR ratio under zero (non-zero) bias voltage ($V_{\rm M}$), and $V_{\rm h}$ is the bias voltage equivalent to ${\rm TMR}_{\rm eff}={\rm TMR}_0/2$. The current passing through the access transistor ($I_{\rm M}$) satisfies [20]

$$I_{\rm DS}=I_{\rm M}=\mu_{\rm n}C_{\rm ox}\frac{W}{L}\left[(V_{\rm GS}-V_{\rm TH})V_{\rm DS}-V_{\rm DS}^2\right] \quad (6)$$

when the transistor is working in the triode (ohmic) region ($V_{\rm GS}>V_{\rm TH}$ and $V_{\rm DS}<V_{\rm GS}-V_{\rm TH}$). Here, $\mu_{\rm n}$ is the mobility of electrons, $C_{\rm ox}$ is the oxide thickness, and W (L) is the channel width (length). For $V_{\rm DS}>V_{\rm GS}-V_{\rm TH}$ (saturation region), the channel exhibits pinch-off near drain and the current can be approximated by the maximum value of (6) as [20]

$$I_{\rm DS}=I_{\rm M}=\frac{1}{2}\mu_{\rm n}C_{\rm ox}\frac{W}{L}(V_{\rm GS}-V_{\rm TH})^2. \quad (7)$$

From a circuit point of view, for given MTJ device characteristics the value of the circuit parameters ($V_{\rm A}$, $I_{\rm IMP}$, and $R_{\rm G}$ in Fig. 4) can be optimized to minimize $P_{\rm err}$. An example of such an optimization for the MTJ-based gate is presented in our previous work [13]. Based on (1)-(7), the

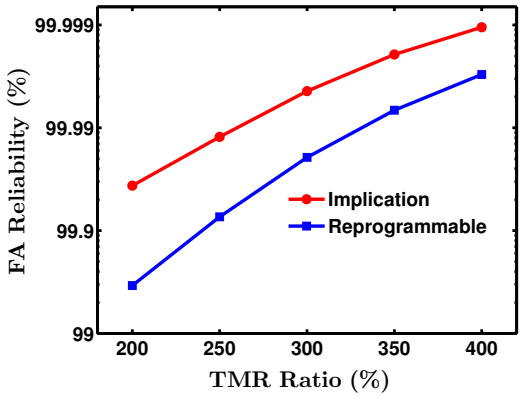

Fig. 6. Reliability of the MTJ-based magnetic full adder as a function of the TMR ratio plotted for optimized circuit parameters and $\Delta_0 = 60$. The record room temperature TMR of 604% [21] promises highly reliable MTJ-based logic applications.

reliability of a magnetic full adder as a function of the TMR ratio is plotted in Fig. 6 for IMP-based and reprogrammable-based implementations with optimized circuit parameters. It demonstrates that the reliability increases with the TMR for both circuits. Due to a more reliable conditional switching behavior exhibited by the IMP gate, it provides a magnetic full adder with smaller error probability compared to the reprogrammable gates.

The 1T/1MTJ-based implementation of the intrinsic logic-in-memory gates can extend MRAM electronics from memory to logical computing applications for complex logic functions. An IMP-based full adder design involves 27 subsequent FALSE and IMP operations [16] on 6 1T/1MTJ cells which already exist within the STT-MRAM structure (Fig. 5). As compared to the non-volatile full adder in [6], the need for CMOS-based logic is eliminated and superior logic density can be achieved.

IV. Conclusion

A method for reliability analysis of the MTJ-based logic circuits is presented. As an example, the reliability of a magnetic full adder using IMP and reprogrammable gates is considered. It is shown that the reliability improves with the TMR for both designs and the IMP-based implementation exhibits a more reliable logic behavior. These structures can be used to build more complex circuits which implement more complex logic functions. Since the 1T/1MTJ cell can be utilized as both memory and the main computing element, non-volatile intrinsic logic-in-memory can be realized with no need for intermediate circuitry. Circuits which exhibit low power consumption, high logic density, and high speed operation simultaneously can thus be designed.

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