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Toward a streamlined projection of small device bias temperature instability lifetime distributions

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As the CMOS device dimensions shrink to nanometer scale, the time-dependent V_{TH} variability (heteroskedasticity) becomes evident due to the reduced number of stochastically behaving traps in the gate oxide. Consequently, the bias temperature instability (BTI) lifetime of nanometer-sized devices can only be correctly described in the form of time- (or workload-) dependent distributions. This paper discusses a streamlined procedure to obtain BTI lifetime projections for nanometer-scaled devices from the combination of measurements of a small sample set of nanoscaled devices and several large area test devices. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4772587]

I. INTRODUCTION

With the continuous downscaling of CMOS device dimensions, (1) the amount of gate oxide defects in each device decreases to a numerable level.[1–3] while their relative impact on the device characteristics increases.[4–6] (2) The properties of each defect, such as its capture and emission times and its impact, have been shown to be voltage and/or temperature dependent and widely distributed by means of experiments[4,7–10] and corroborated atomistic simulations.[11,12] (3) The occupation kinetics of each defect appears to involve metastable states and is known to be stochastic.[13–15] All of these result in each of the nominally identical nanometer-scaled devices behaving very differently during operation, leading to increasing time-dependent variability (heteroskedasticity) of device parameters, such as the threshold voltage V_{TH}. Consequently, the bias temperature instability (BTI) lifetime of nanometer-sized devices cannot be predicted individually and can be only described in terms of time- (or workload-) dependent distributions.

It is, however, practically impossible to study the above-listed contributions or even to merely measure a sufficiently large number of devices of each new device variation and/or process split. Here we therefore discuss a possible path for obtaining the small device lifetime projections from the combination of measurements of a reasonably small sample set of nanoscaled devices and a few large area devices typically fabricated for test purposes on the same chip. We identify the sources of discrepancies in this approach.

II. EXPERIMENT

0.8-nm-SiO_2/1.8-nm-HfSiO pFETs with metallurgic length $L_{eff} \sim 45$ nm and width $W = 90$ nm were used to study the negative BTI (NBTI) reliability of deeply scaled devices. Large area devices ($W \times L = 10 \times 0.5\ \mu m^2$) fabricated on the same wafer for test purposes were also measured under identical experimental conditions. The properties of individual defects in nanoscaled devices, which ultimately control the time-dependent variability of a technology, were studied by means of NBTI measurement. After a defect charging phase at stress gate voltage V_{STRESS} (i.e., a NBTI stress), the source current relaxation transients (ΔI_S) were recorded at sense gate voltage V_{SENSE} equal to the threshold voltage of each fresh device $V_{TH,0}$. The recorded ΔI_S transients were converted to ΔV_{TH} using the initial I_S–V_G curve of the fresh device as a reference. The I_S–V_G curves after the stress period were also recorded in order to ensure that the transcharacteristics were not distorted and, therefore, the I_s–ΔV_{TH} transformation was accurate.[16] In order to get an insight into the thermal activation of the process, the experiment was repeated at different temperatures.

III. RESULTS AND DISCUSSION

Figure 1 shows the relaxation traces after a gate voltage stress of 1.5 V for 182 s at 25 °C obtained from 30 nanoscaled devices, each trace revealing the combined response of multiple defects in a device perturbed by the accelerated test. The *total* $|\Delta V_{TH}|$ (ΔV_{TH} at given $t_{RELAX} = 1$ ms) strongly varies from device to device as a result of the combination of different number of well-defined ΔV_{TH} drops with different magnitudes. Nevertheless, the average relaxation $\langle|\Delta V_{TH}|\rangle$ resembles the curve taken on a large area device indicating *that identically behaving traps are responsible for BTI in small and large area devices*.

The well-defined ΔV_{TH} drops, *single* ΔV_{TH}, observed in each nanometer-scaled device are due to individual discharge events of trapped holes during the stress phase. The number of *single* ΔV_{TH} among traces follows a Poisson distribution (not shown).[10] Figure 2 displays the *single* ΔV_{TH} in a complementary accumulative plot (1-CDF) where the y-axes is in log scale. The magnitude of *single* ΔV_{TH} can be

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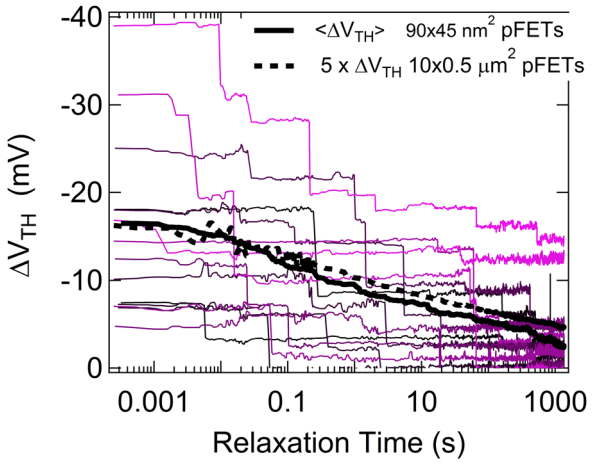

FIG. 1. (Color online) Bias temperature instability (BTI) relaxation transients obtained on 12 representative nanoscaled ($W \times L = 90 \times 45\ nm^2$) and a large ($W \times L = 10 \times 0.5\ \mu m^2$) 0.8-nm-$SiO_2$/1.8-nm-HfSiO pFETs. All the devices were stressed under identical conditions: $|V_{STRESS} - V_{TH,0}| = 1.5$ V, $t_{STRESS} = 182$ s, and $T = 25\,^{\circ}C$. Steps due to single-carrier discharge events are evident for the nanometer-scaled devices. The large dispersion is due to the stochastic distributions of N_T and the impact of each trap. Nevertheless, *the average relaxation resembles the curve taken on a large area device, indicating that identically behaving traps are responsible of BTI on small and large area FETs.*

to the first approximation described by an exponential distribution (see Fig. 2) with average *single* ΔV_{TH} value η equal to -3.4 mV. This η value is about approximately two times larger than that expected from the charge sheet approximation $\eta_0 = q/C_{ox}$. Note in Fig. 2 that extreme *individual events cause drops as large as* ~ -10 mV. Considering that the typical ΔV_{TH} BTI failure criteria for process qualification range between -30 and -50 mV, the combination of just a few extreme *single* ΔV_{TH}s may lead to a nominal failure. These giant V_{TH} shifts caused by single charged defects are explained by the nonuniform potential at the Si/SiO_2 interface caused by the random distributions of dopants in the channel and charged traps in the dielectric. The potential fluctuations produce variations of the inversion charge density and, consequently, preferential conduction paths from the source to the drain. The charging and discharging of single oxide traps over critical positions of the conduction paths then produces significant fluctuations of the drain current and, therefore, critical *single* V_{TH} shifts.[1–3]

As we have shown previously,[5] the *total* $|\Delta V_{TH}|$ distribution can be analytically described considering the convolution of *single* ΔV_{TH} exponentially distributed weighted by a Poisson distribution of the number of active traps N_T.[5,17] The resulting cumulative distribution, $H_{NT,\eta}$, in the following, plotted in Fig. 3, can properly describe the experimental data and it is defined by means of only two parameters: the average *total* $|\Delta V_{TH}|$, $\langle|\Delta V_{TH}|\rangle$, and the average impact on the V_{TH} value per trap, η. These two magnitudes are correlated through the average number of active traps, N_T, according to the following relation $\langle \Delta V_{TH} \rangle = \eta \times N_T$.[5]

Figure 3 also shows a shift of the *total* $|\Delta V_{TH}|$ distributions toward larger values with increasing temperature. Since the *single charge* ΔV_{TH}s are not thermally activated (cf. Fig. 2), the increase of the *total* $|\Delta V_{TH}|$ is attributable to an escalated N_T with temperature. Figure 4 displays the $\langle|\Delta V_{TH}|\rangle$ obtained from nanoscaled and large area pFETs at different temperatures and for different stress times in an Arrhenius plot. The data can be fitted with Arrhenius laws of activation energy $E_{ACT} \sim 118$ mV for both device sizes, pointing out again that identical states are responsible of the BTI degradation in small and large area devices. However, $\sim 5\times$ larger degradation is observed in nanometer-sized devices after the same stress. Since the average *total* $|\Delta V_{TH}|$, $\langle|\Delta V_{TH}|\rangle$, is the product of the number of active traps N_T and their average impact on V_{TH}, η,[5] the ratio of degradation for nanometer-scaled devices and large devices is given by

$$\frac{\langle \Delta V_{TH,small} \rangle}{\langle \Delta V_{TH,large} \rangle} = \frac{\eta \times N_{T,small}}{\eta_0 \times N_{T,large}}, \tag{1}$$

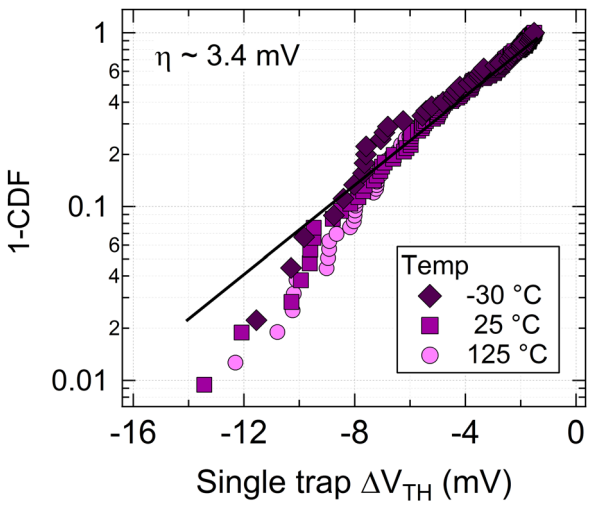

FIG. 2. (Color online) Complementary cumulative distributions (1-CDF) of ΔV_{TH} step heights due to single oxide defects, i.e., *single* ΔV_{TH}, obtained under the electrical stress conditions shown in caption of Fig. 1, follow an exponential distribution with the average *single* ΔV_{TH} step height $\eta = 3.4$ mV independently of the temperature.

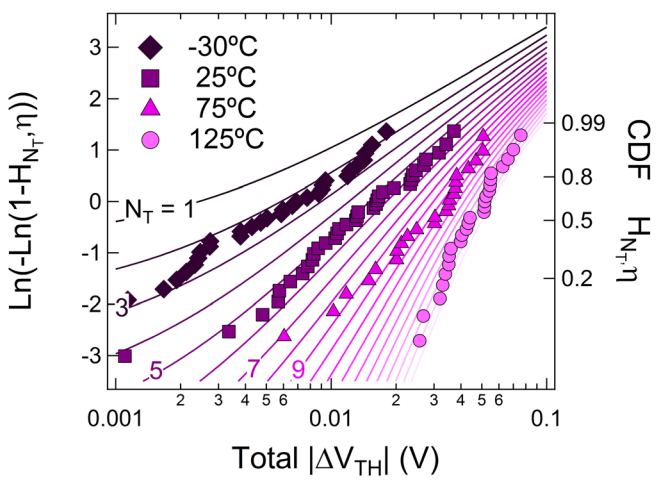

FIG. 3. (Color online) Cumulative distributions of the *total* $|\Delta V_{TH}|$ for the nanometer-sized devices after the electrical stress conditions specified in caption of Fig. 1 shown in a Weibull plot. (Lines) *Total* $|\Delta V_{TH}|$ CDFs, $H_{NT,\eta}$, for different N_T values obtained from the analytical model presented in Refs. 5 and 10 match excellently the experimental data at different temperatures.

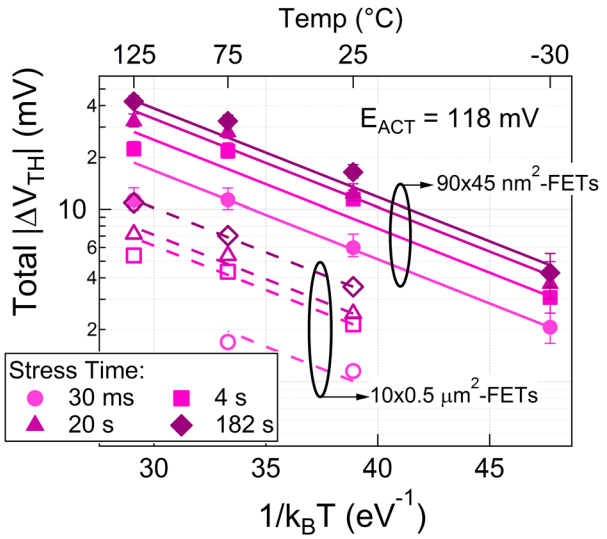

FIG. 4. (Color online) $\langle|\Delta V_{TH}|\rangle$s at 1 ms relaxation time with plus or minus standard deviation error bars obtained on small ($W \times L = 90 \times 45$ nm^2) and large ($W \times L = 10 \times 0.5\ \mu$m^2) pFETs submitted to a stress overdrive voltage of $|V_{STRESS} - V_{TH,0}| = 1.5$ V follow Arrhenius laws with apparent activation energy of 118 mV. 5× larger degradation is observed for the nanoscaled pFETs for the technology under study.

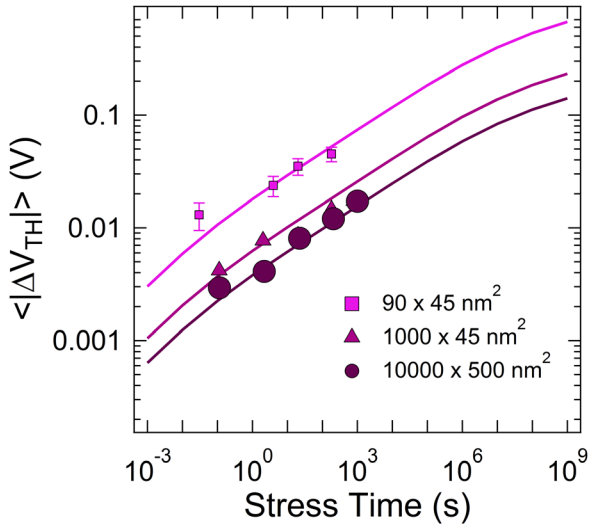

FIG. 5. (Color online) Comparison of the average *total* $|\Delta V_{TH}|$, i.e., $\langle\Delta V_{TH}\rangle$, degradation at $t_{RELAX} = 1$ ms as a function of stress time for small (90×45 nm^2), short (45 nm × 1 μm), and large ($10 \times 0.5\ \mu$m^2) pFETs stressed under the same overdrive voltage $|V_{STRESS} - V_{TH,0}| = 1.5$ V, and temperature $T = 125$ °C. Data from small and short devices are obtained after averaging a significant large number of traces taken in different devices. ΔV_{TH} degradation is fitted according to the capture and emission time parameters obtained folowing the methodology presented in Ref. 18. A significant larger degradation is observed for small devices compared to the wide ones, indicating a high trap density close the STI edge.

η_0 being q/C_{ox}. Therefore, the 5× increase is due to (1) the larger impact per charged trap ($\eta/\eta_0 \sim 2$) caused by channel percolation effects in small devices and (2) the higher trap density in smaller devices likely due to edge-related processing effects.[18,19]

In order to asses the spatial position of the traps for this particular technology, short ($L \sim 45$ nm) but wide ($W = 1\ \mu$m) devices were also tested under the same stress conditions. For these device dimensions, the effect of individual defects starts being perceptible and, the *total* $|\Delta V_{TH}|$ becomes distributed. Nevertheless, the average *total* $|\Delta V_{TH}|$ recovery traces resemble the ones obtained in the large and small area devices. As shown in Fig. 5, a slightly larger degradation is observed for the intermediate area devices, and only when the width dimensions are reduced to the nanometer scale, the *total* $|\Delta V_{TH}|$ notably increases. This fact indicates that a larger trap density is placed close to shallow trench isolation (STI) likely due to edge/stress effects for this particular technology. In order to assess the trap density close to the STI region, a complete evaluation of the doping profile and the gate oxide thickness as a function of the device dimensions is necessary.

Considering these findings, the V_{TH} degradation for nanometer-scaled and large area devices can be described by a simple power-law model for the stress time and voltage which is thermally activated[20]

$$\langle\Delta V_{TH}\rangle = A(V_G - V_{TH})^{\gamma} t_{stress}^{n} e^{-\frac{E_{ACT}}{kT}}, \quad (2)$$

where the activation energy E_{ACT} and the power factors γ and n are common for nanometer-scaled and large area devices. However, the prefactor A depends on the device area and, therefore, has to be correctly scaled. In the case of the studied technology, the scaling factor between nanometer-scaled and large area devices ($\langle\Delta V_{TH,small}\rangle / \langle\Delta V_{TH,large}\rangle = A_{small}/A_{large}$) was found to be 5. Consequently, the BTI lifetime distributions of nanometer-scaled devices can be predicted by combining (1) the power factors γ and n, the activation energy E_{ACT}, and the prefactor A_{large} obtained from ΔV_{TH} measured on large devices at different stress conditions and (2) the η value and the prefactor A_{small} determined from a reduced sample size of nanometer-scaled devices of the technology under study at only one stress condition.

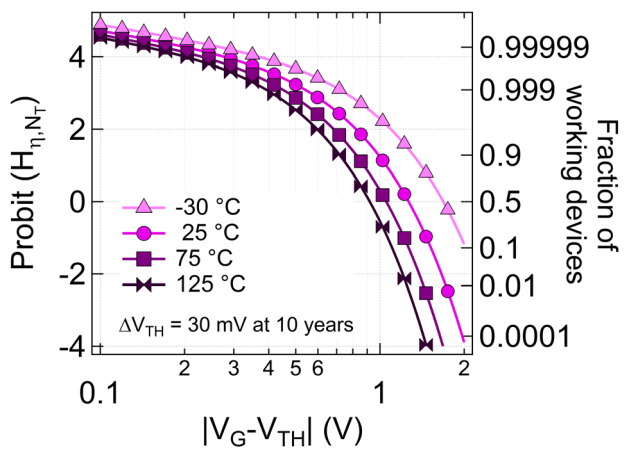

FIG. 6. (Color online) Predicted 10-yr lifetime cumulative distributions of the *total* $|\Delta V_{TH}|$ at $t_{RELAX} \sim 1$ ms for nanometer-scaled devices at different temperature. Note that the average value shifts to larger overdrives with decreasing temperature; however, no significant improvement is obtained at lower overdrives.

When Eq. (2) is used in the analytical model for the distribution of *total* $|\Delta V_{TH}|$,[5,10] the distribution $H_{NT,\eta}$ becomes dependent on the overdrive voltage, the stress time, and the temperature, $H_{NT(VG\text{-}VT,tstress,T)),\eta}$, allowing scale to lower overdrives and long times. Following this procedure, the prediction of the fraction of working devices ($|\Delta V_{TH}| < 30\,\text{mV}$) after 10 yr of operation is obtained as a function of the overdrive voltage ($V_G - V_{TH}$) for different temperatures, as shown in Fig. 6. As in the case of the large area devices, a reduction of the operating gate overdrive voltage is observed with increasing temperature. However, no significant increase of the fraction of working devices is obtained at low overdrives with decreasing temperature since the impact on V_{TH} per single trap is temperature independent (cf. Fig. 2).

IV. CONCLUSIONS

Based on a detailed understanding of the behavior and the statistics of individual defects as a function of stress conditions and temperature, we have concluded that identically behaving traps are responsible of the BTI degradation on small and large area devices. From the data measured on large area devices, the evolution of the average BTI can be extrapolated. The shape of the BTI lifetime distribution only can then be estimated from the measurement of the η value on reduced sample size of nanometer-scaled devices of the technology under study.

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