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Implication logic gates using spin-transfer-torque-operated magnetic tunnel junctions for intrinsic logic-in-memory

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ABSTRACT

As the feature size of CMOS components scales down, the standby power losses due to high leakage currents have become a top concern for modern circuit design. Introducing non-volatility in logic circuits allows to overcome the standby power issue. Magnetic tunnel junctions (MTJs) offer a great potential, because of their non-volatility, unlimited endurance, CMOS compatibility, and fast switching speed. This work proposes current- and voltage-controlled MTJ-based implication (IMP) logic gtes for future non-volatile logic-in-memory architecture. The MTJ-based implication logic realizes an intrinsic logic-in-memory known as "stateful" logic for which the MTJ devices serve simultaneously as memory elements and logic gates. Spintronic implication logic gates are analyzed by using a SPICE model for spin-transfer torque (STT) MTJs in order to show the reliability of the IMP operation. It has been demonstrated that the proposed current-controlled implication gate offers a higher performance (power and reliability) than the conventional voltage-controlled one. The realization of the spintronic stateful logic operations extends non-volatile electronics from memory to logical computing applications and opens the door for more complex logic functions to be realized with MTJ-based devices. We present a stateful logic circuit based on the common STT-MRAM architecture capable of performing material implication. As an application example, an IMP-based implementation of a full-adder is presented.

1. Introduction

The basic structure of a magnetic tunnel junction (MTJ) consists of two ferromagnetic layers separated by a non-conductive tunneling barrier as shown in Fig. 1a. The magnetization of one layer is pinned (fixed layer), while the magnetization of the second one can be switched freely (free layer) using an external magnetic field or the spin-transfer torque (STT) effect [1,2]. In the STT-operated MTJ (STT-MTJ), the spin-polarized electrons induce torque directly on the magnetization of the free layer to enforce switching. Therefore, the STT-MTJ gives pure electrical switching and better scalability than conventional MTJs switched by magnetic field.

Because of the non-volatility, unlimited endurance, fast-switching speed, and CMOS compatibility of the MTJ devices [3–5], MTJ-based non-volatile logic has received great interest to overcome the significant increase in the leakage currents in CMOS-based circuits [6]. Furthermore, MTJ-based logic can improve the conventional CMOS-based logic which combines logic units and memory units to transfer back and forth information between separated logic and memory units, by shortening the interconnection delay and opens the door for a shift away from the Von Neumann architecture for innovation in computational paradigms. However, in the previously proposed MTJ-based logic-in-memory and CMOS/MTJ hybrid circuits [7,8], the MTJs are distributed over CMOS logic elements only as ancillary devices for data storage (memory). These architectures require readout schemes for reading the stored logical data as well as providing the next logic stage with properly adjusted current or voltage signal levels. Furthermore, as the computations are localized, the generalization of the common logic-in-memory circuits to large-scale logic systems is challenging.

Here, by using two different circuit topologies of the STT-MTJ-based implication (IMP) gates (Fig. 1b and c), we show the realization of an intrinsic logic-in-memory architecture (also known as "stateful" logic [9]) for which the MTJ devices are used simultaneously as the memory elements and the main computing elements (logic gates). Therefore, MTJ-based stateful logic reduces the device counts by eliminating the need for MOS-based logic elements as compared to the common logic architecture.

2. MTJ-Based implication logic gates analysis

Material implication, p IMP q, is a fundamental Boolean logic operation which reads 'p implies q' or 'if p, then q', and is equivalent to '(NOT p) OR q' as shown in Table 1. To compute any Boolean

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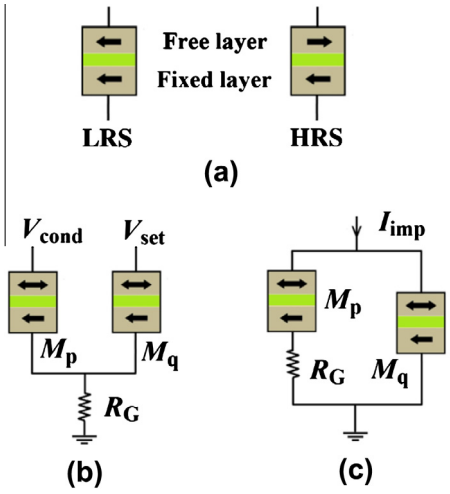

Fig. 1. (a) MTJ basic structure. The conventional [9] (voltage-controlled) implication gate, (b) and our proposed (current-controlled) implication gate, (c) circuit topologies.

function, the operations IMP and NIMP (negated IMP) form a computationally complete logic basis in combination with any operation from the sets C and C′, respectively, for which C = {NOT, FALSE, XOR, NIMP} and C′ = {NOT, TRUE, XNOR, IMP}.

To enable memristive stateful logic operations, the realization of the operation IMP has been demonstrated recently [9] using TiO_2 memristive switches [10]. However, the TiO_2-based IMP offers low speed and requires a different fabrication platform than the existing cost-effective silicon process. In contrast to [9], we use MTJs as the memory elements to build spintronic IMP gates. In addition to the conventional (voltage-controlled) IMP circuit topology (Fig. 1b), we propose and investigate a new topology (Fig. 1c) driven by a current source (current-controlled IMP), which offers a more energy-efficient and reliable implementation.

The electrical resistance of the device depends on the relative orientation of the magnetization directions of the ferromagnetic layers as shown in Fig. 1a. The parallel (P) magnetization state results in a low resistance state (LRS; R_P) across the barrier, while the antiparallel (AP) alignment places it in a high-resistance state (HRS; R_{AP}). The resistance modulation is described by the tunnel magnetoresistance (TMR) ratio, defined as $TMR = (R_{AP} - R_P)/R_P$. As a non-volatile memory element, the MTJ can store binary logic data via its low and high resistance states.

In the voltage-controlled topology (Fig. 1b), the material implication can be executed by simultaneously applying the voltage pulses V_{cond} and V_{set} to the source MTJ (M_p) and the target MTJ (M_q) for which $|V_{cond}| < |V_{set}|$. According to the polarities, these voltage pulses tend to put the MTJs in a low resistance state. In the current-controlled topology the material implication can be executed by applying the current pulse I_{imp} as shown in Fig. 1c. In this topology the source MTJ is connected to a conventional resistance (R_G) while the target MTJ (M_q) is connected to the ground directly. The current pulse I_{imp} is in a direction which tends to put the MTJs in a low resistance state.

Table 1
The material implications, IMP and NIMP (negated IMP), truth tables.

State	p	q	p IMP q	p NIMP q
1	0	0	1	0
2	0	1	1	0
3	1	0	0	1
4	1	1	1	0

In both voltage- and current-controlled topologies, depending on the initial resistance states of the source and the target MTJs, a high-to-low resistance switching event is enforced to the target MTJ (desired switching event) or not (undesired switching event). In fact, a desired switching event is a high-to-low switching event which is enforced to M_q only, when both M_p and M_q are initially at high resistance states (State 1) and for all three other possible combinations of the initial resistance states (States 2, 3, and 4), the resistance states of M_p and M_q are left unchanged and there is no undesired switching event as shown in Table 2. This conditional switching behavior corresponds to the basic Boolean operations called material implications, IMP and NIMP. The initial logic state of the source and target MTJs act as the inputs, while the final logic state of the target MTJ is the output of the logic operation. In combination with the writing operation (low-to-high resistance switching), the material implication forms a complete logic basis to compute an arbitrary Boolean function.

Indeed, as shown in Table 2, if we define the high and low resistance states (HRS and LRS) as logical 1 and 0, respectively, the realized conditional switching behavior will be equivalent to the logic operation NIMP for which the result of q_n NIMP p_n will be written into the target device M_q. Here the variables p and q indicate the logical state of the M_p and M_q, respectively. With this definition, the low-to-high resistance switching is equivalent to writing logical 1 (operation TRUE). In combination with TRUE, the operation NIMP forms a complete logic basis to compute any Boolean function.

Opposite to the conventional definition, if we define the high and low resistance states as $HRS \equiv 0$ and $LRS \equiv 1$, the realized conditional switching will be equivalent to the fundamental Boolean logic operation IMP as $q_{n+1} \leftarrow p_n$ IMP q_n. With this definition, the low-to-high resistance switching is equivalent to writing logical 0 (operation FALSE). In combination with FALSE, the operation IMP forms a complete logic basis to compute any Boolean function.

We analyze the implication gates based on the SPICE model of the MTJ [11], which uses the equivalent circuit of the STT-MTJ shown in Fig. 2. A curve-fitting circuit is used to model the voltage-dependent effective TMR, which is important to determine the R–V characteristics of the MTJ and the voltage (current) division between the source and target MTJs in an implication gate. In this SPICE model the output signals of the decision circuit (V_1 and V_2) are used to determine that when the device should switch states based on the critical switching time and current (τ_0 and I_{C0})) characteristics of the device, which are usually defined corresponding to the 50% switching probability. However, the decision signal V_1 does not fit the experimental data equally well as shown in Fig. 3. Therefore, in order to estimate the MTJ switching characteristics and analyze the logic behavior and the reliability of the implication gates, we have extended the SPICE model by introducing an error calculation circuit shown in Fig. 2. The theoretical expression of the MTJ switching probability (P_{sw} in Eq. (1)) [13] which has been experimentally verified in [12], is now reproduced well with our extended model as shown in Fig. 3.

$$P_{sw} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I}{I_{C0}}\right)\right]\right\} \quad (1)$$

Here Δ_0 is the magnetic memorizing energy without any current and magnetic field, t is the pulse width, and I is the current flowing through the MTJ. We therefore use the proposed improved SPICE model for direct calculation of P_{sw} and an implication reliability analysis.

For reliability analysis, according to Table 2, we define the implication error as:

$$E_{imp} = (1 - P_{sw}^{q1}) + P_{sw}^{p1} + P_{sw}^{p2} + P_{sw}^{q3} \quad (2)$$

Table 2
The realized conditional switching behavior equivalent to the operation IMP or NIMP depending on the definitions for the high and low resistance states (HRS and LRS) as the logical 0 and 1 or vice-versa.

State	Implication operation (conditional switching)				HRS ≡ 0, LRS ≡ 1 $q_{n+1} \leftarrow p_n$ IMP q_n			HRS ≡ 1, LRS ≡ 0 $q_{n+1} \leftarrow q_n$ NIMP q_n		
	p_n	q_n	p_{n+1}	q_{n+1}	p_n	q_n	q_{n+1}	p_n	q_n	q_{n+1}
1	HRS	HRS	HRS	LRS	0	0	1	1	1	0
2	HRS	LRS	HRS	LRS	0	1	1	1	0	0
3	LRS	HRS	LRS	HRS	1	0	0	0	1	1
4	LRS	LRS	LRS	LRS	1	1	1	0	0	0

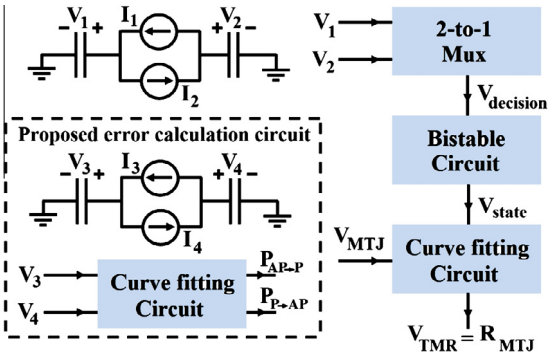

Fig. 2. The simplified equivalent circuit of the MTJ model in [11] and the proposed error calculation circuit. $I_3 = \exp[-\Delta_0(1 - I/I_{C0(AP\rightarrow P)})]$ and $I_4 = \exp[-\Delta_0(1 - I/I_{C0(P\rightarrow AP)})]$.

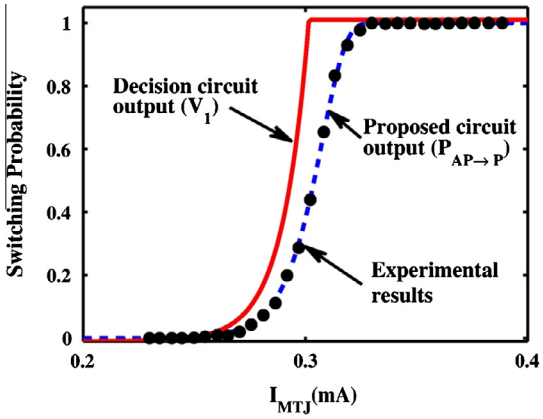

Fig. 3. Switching probability as a function of the applied current. The output of the proposed error calculation circuit reproduces the experimental data [12] as expected from the theory (1).

where P_{sw}^{q1} is the switching probability of the desired high-to-low switching event on M_q in State 1 which must goes to unity and P_{sw}^{p1}, P_{sw}^{p2}, and P_{sw}^{q3} are the switching probabilities of the undesired high-to-low switching events on M_p and M_q in States 1, 2, and 3, respectively, which must go to zero.

As an example, Fig. 4 shows the switching probabilities P_{sw}^{q1}, P_{sw}^{p1}, P_{sw}^{p2}, and P_{sw}^{q3} as a function of I_{imp} plotted for our proposed current-controlled implication gate with given MTJ device characteristics and fixed R_G and pulse durations, to show that how the state dependent modulation (SDM) of the current flowing through the target MTJ (M_q) can open a reliable window (RW) the switching windows (SWs) of the desired and undesired AP → P switching

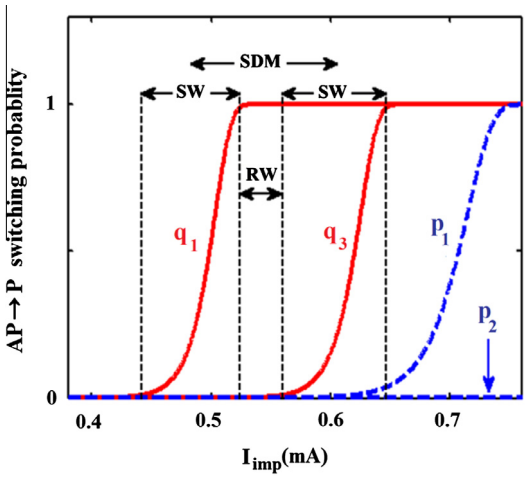

Fig. 4. The high-to-low (AP → P) switching probabilities of M_q and M_p (P_{sw}^{q1}, P_{sw}^{p1}, P_{sw}^{p2}, and P_{sw}^{q3}) plotted for a 50 ns IMP execution in the current-controlled IMP circuit topology based on physical devices characterized in [12]. The SDM opens a reliable window (RW) between the switching windows (SWs) of the desired and undesired AP → P switching events.

events. In fact, the current I_{imp} with a pulse magnitude in the reliable window (RW) provides a conditional switching behavior on the target device M_q which depends on the initial resistance states of the M_q and M_p and is equivalent to the logic operation described in Table 2.

The current I_{imp} is divided between the source and the target MTJs inversely proportional to the total resistance of each branch. Since the resistance values of the MTJs depend on the stored logical values, the current division between them depends on the initial logic states. The current flowing through each branch tends to enforce a AP → P (high-to-low) switching to the MTJ devices. The source MTJ is already in the low resistance state in States 3 and 4. Due to R_G, the current flowing through the source MTJ M_p is lower than the critical current required for high-to-low resistance switching. Therefore, the source MTJ remains unchanged in States 1 and 2 as shown in Fig. 4. The target MTJ is initially in the low resistance state in States 2 and 4. Therefore, I_{imp} can enforce a high-to-low switching event on M_q only in State 1 (as a described switching) and State 3 (as an undesired switching) which are described in the following.

The difference between the currents flowing through M_q in States 1 and 3, is caused by the difference between the initial resistance states of the source device M_p. In State 1, M_p has a high resistance which is added to R_G. So the majority of the current I_{imp} flows through M_q which is higher than the critical current required for high-to-low resistance switching ($I_{AP\rightarrow P}$). To compensate the current flowing through M_p, the current I_{imp} must be higher than the current $I_{AP\rightarrow P}$. During the switching the resistance of the M_p

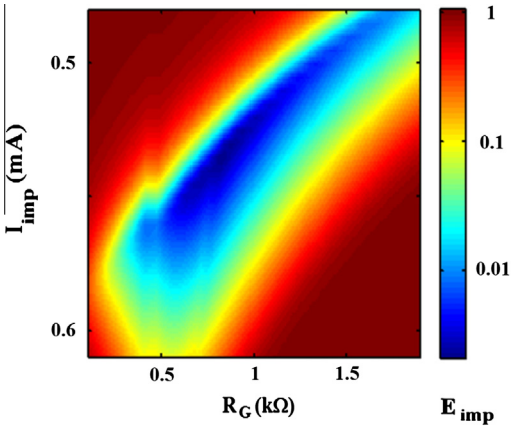

Fig. 5. The implication error as a function of the circuit parameters R_G and I_{imp} in the current-controlled gates plotted for a 50 ns IMP execution based on physical devices characterized in [12].

decreases while the resistance of the M_q remains unchanged. Therefore, the current flowing through the M_q increases. This acts as a positive feedback which accelerates the switching. In State 3, M_p is in low resistance state. Therefore, the current flowing through the M_p is higher as compared to State 1 (the SDM shown in Fig. 4). This decreases the current flowing through the M_q below the critical current required for switching.

With the conventional topology, the initial logic state of the source MTJ (M_p) provides a voltage modulation across the target MTJ (M_q) through R_G. Due to this modulation, M_q switches (AP → P) in State 1, but remains unchanged in State 3. Thus, V_{cond} is chosen as $|V_{cond}| < |V_{set}|$ to leave M_p unchanged.

From a circuit point of view, the value of the circuit parameters (V_{cond}, V_{set}, and R_G in the voltage-controlled gate and I_{imp} and R_G in the current-controlled gate) can be optimized to minimize the implication error for given MTJ device characteristics and fixed pulse durations. Fig. 5 shows an example of such an optimization for the current-controlled gate. In order to analyze and compare the performance of the implication gates, we implemented the improved SPICE model (Fig. 2) in MATLAB. Our results show that in the traditional voltage-controlled gate (Fig. 1b), the optimal R_G is higher by a factor of two to three as compared to the current-controlled one. This is demonstrated in Fig. 6. Therefore, for fixed current level required for a given switching time, the implication energy consumption is about 60% lower in the novel

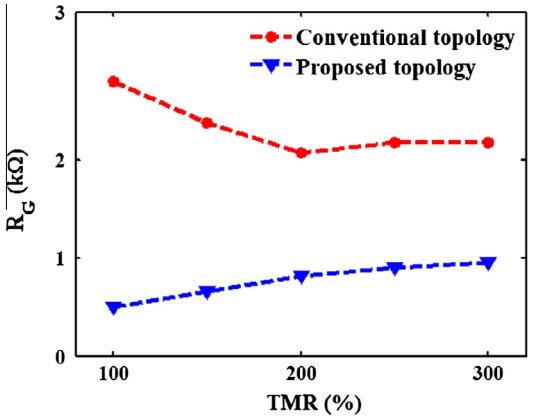

Fig. 6. The values of R_G corresponding to the minimum error design depending on the TMR ratio. The optimal R_G in the conventional voltage-controlled gates is higher as compared to the proposed current-controlled topology.

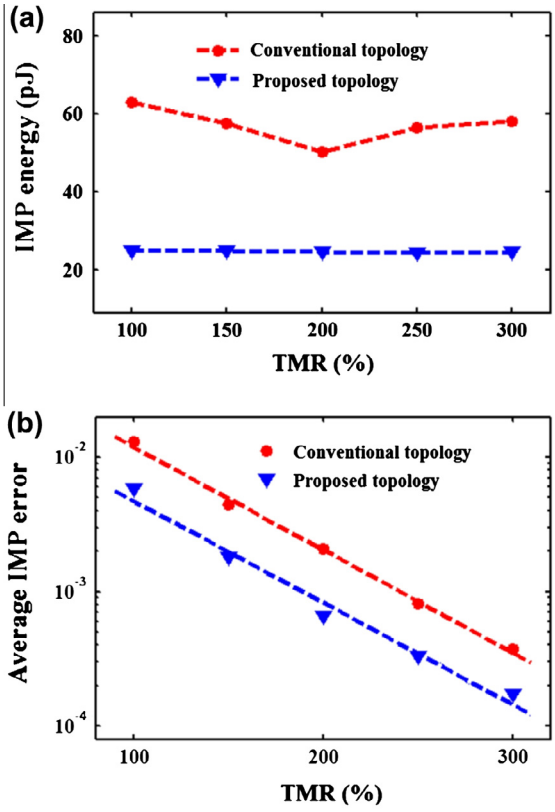

Fig. 7. The IMP energy consumption (a) and the average error, (b) depends on the TMR ratio for both conventional and proposed topologies.

current-controlled gate topology (Fig. 1c) than in the conventional voltage-controlled gate topology (Fig. 1b). A comparison of the IMP energy consumption in the two topologies is shown in Fig. 7a.

Robust implication logic behavior requires a high enough initial state dependent modulation in both topologies. This modulations on M_q which is caused by the difference between the high and low resistances of M_p, is directly proportional to the TMR ratio of the MTJ. Therefore, from the device point of view, we expect that the error E_{imp} decreases with the increase of the TMR ratio which is the most important device parameter for reliability. Fig. 7b demonstrates that the error E_{imp} decreases exponentially with increasing TMR ratio. At a fixed TMR the proposed topology (Fig. 1c) provides a higher modulation on M_q, thus reducing the IMP error by about 60% as compared to the conventional one. The record room temperature TMR of 604% [14] reported in single-barrier MgO-based MTJs is close to the theoretical maximum [15,16] which is about 1000%. This makes the MgO-based MTJs predominant candidates for STT magnetoresistive random access memories (STT-MRAMs) and promises highly reliable implication gates.

3. Implication gates for large-scale logic

The universality of the NAND and NOR operations means that they are computationally complete and any Boolean function can be performed using either NAND or NOR gate. Table 3 shows a three-step implementation of a universal logic operation (NAND or NOR) using sequential P → AP and implication operations on three MTJs M_a, M_b, and M_c containing the logical values a, b, and c, respectively. The result of the universal logic operation between the variables a and b will be written in c. In Step 1, the low-to-high resistance state switching is executed on M_c. In Step 2, the implication operation is executed between a and c for which a acts as the

Table 3
The realized conditional switching behavior equivalent to the operation IMP or NIMP. The variables c_{n+2} (a) and c_{n+3} (b) indicate the target (source) logical values of the implication operations in Step 2 and Step 3, respectively.

State	Three subsequent operation on a, b, c					HRS ≡ 0, LRS ≡ 1			HRS ≡ 1, LRS ≡ 0		
	Input		1: HRS	2: Imp. (a, c)	3: Imp. (b, c)	$c_{n+3} \leftarrow a$ NAND b			$c_{n+3} \leftarrow a$ NOR b		
	a	b	c_{n+1}	c_{n+2}	c_{n+3}	a	b	c_{n+3}	a	b	c_{n+3}
1	HRS	HRS	HRS	LRS	LRS	0	0	1	1	1	0
2	HRS	LRS	HRS	LRS	LRS	0	1	1	1	0	0
3	LRS	HRS	HRS	HRS	LRS	1	0	1	0	1	0
4	LRS	LRS	HRS	HRS	HRS	1	1	0	0	0	1

source variable and c is the target variable. In Step 3, the implication operation is executed between b and c for which b acts as the source variable and c is the target variable. Therefore, the final result is written in M_c, and M_a and M_b will remain unchanged.

Similar to the operations described in Table 2, if we define the high and low resistance states (HRS and LRS) as logical 0 and 1, respectively, the realized universal operation is equivalent to the NAND operation which has been executed in three steps including a FALSE and two IMP operations. But if we use the opposite definition (HRS ≡ 1 and LRS ≡ 0), the realized operation is equivalent to the NOR operation which includes a TRUE and two NIMP operations. This example shows that any logic circuit which is designed by using the operations AND, OR, and NOT in the Shannon's conventional logic framework can also be designed by using IMP (NIMP) and FALSE (TRUE) operations.

In order to generalize the MTJ-based implication gates to a large scale logic-in-memory circuit, we use the magnetoresistive random access memory (MRAM) architecture. In conventional MRAM architecture the MTJ is connected to the crossing points of two perpendicular arrays of parallel conducting lines. The STT switching technique brought significant advantages and eliminates the difference between reading and writing in STT-MRAM architecture [12]. A typical memory cell of the STT-MRAM, which consists of an access transistor and an MTJ as its storage element (1T/1MTJ structure) is shown in Fig. 8.

Fig. 9 shows simplified implication logic circuit architecture based on the STT-MRAM architecture to realize the MTJ-based current-controlled implication gate shown in Fig. 1c. This circuit enables MTJ-based stateful logic architecture for which the need of using extra charge-based logic gates is eliminated and the memory cells serve simultaneously as logic gates and latches via implication operation.

The implication operation between two memory cells $C_{i,j}$ and $C'_{i,j}$ ($q_{i,j} \leftarrow p'_{i,j}$ IMP $q_{i,j}$) can be performed by simultaneous selection of the i-th word lines (WLs) and the j-th and the j'-th source line (SL) selectors which connect the SLs to the ground directly and via R_G, respectively, and by applying the current source I_{imp} to the j-th and j'-th bit lines (BLs). Then the result of the implication operation will be written in $C_{i,j}$.

As compared to the STT-MRAM, we have added two *work cells* to any WL, while it has been shown that with two additional memristors all Boolean functions on any number of memory cells can be performed [18]. These *work cells* can also be used to connect different WLs. Indeed, in order to perform the implication between memory cells from different WLs, one can copy the logic data stored in one memory cell to a work cell from the other WL. It should be noted that the nonzero ON resistance of the access transistors (R_{on}) decreases the effective TMR of the 1T/1MTJ cells which can be defined as:

$$\mathrm{TMR}_{eff} = \frac{R_{\mathrm{AP}} - R_{\mathrm{P}}}{R_{\mathrm{P}} + R_{on}} \tag{3}$$

Therefore, a robust implication operation needs MTJs with sufficiently high TMR and electrical resistance. Our simulations show that the TMR of a 1T/1MTJ including the MTJ devices characterized in [12] and an access device with a width of about 1–2 μm at the 180-nm technology decreases by about 10–30%. Therefore, according to Fig. 7b, a 99.9% implication correct logic behavior requires a TMR ratio higher than 250%.

3.1. Stateful spintronic full-adder

We consider the implication-based realization of a full-adder which is a basic element of arithmetic circuits. As is well known, it adds three binary inputs (q_1, q_2, and c_{in}) and produces two binary outputs, sum ($s = q_1$ XOR q_2 XOR c_{in}) and carry ($c_{out} = [q_1$ AND $q_2]$ OR $[c_{in}$ AND $(q_1$ XOR $q_2)]$) as shown in Fig. 10. We use the definition HRS ≡ 0 and LRS ≡ 1, so the basic implication logic operations are equivalent to FALSE and IMP.

Since the implication gates cannot fan out, a logical value which is required as the target variable for an implication operation has to be copied in an additional cell, if it is needed as an input for

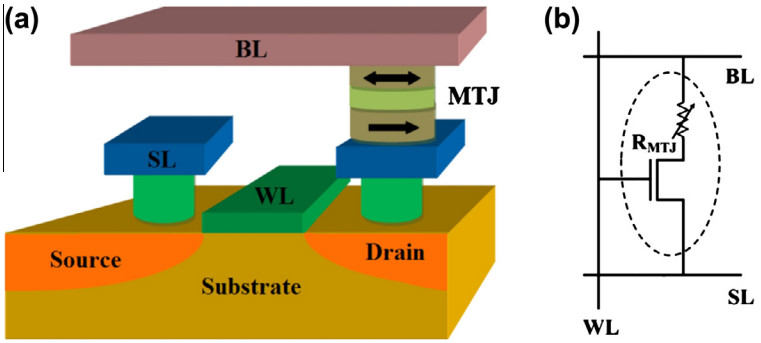

Fig. 8. 1T/1MTJ structure. Structural (a) and the equivalent circuit, (b) diagrams [17].

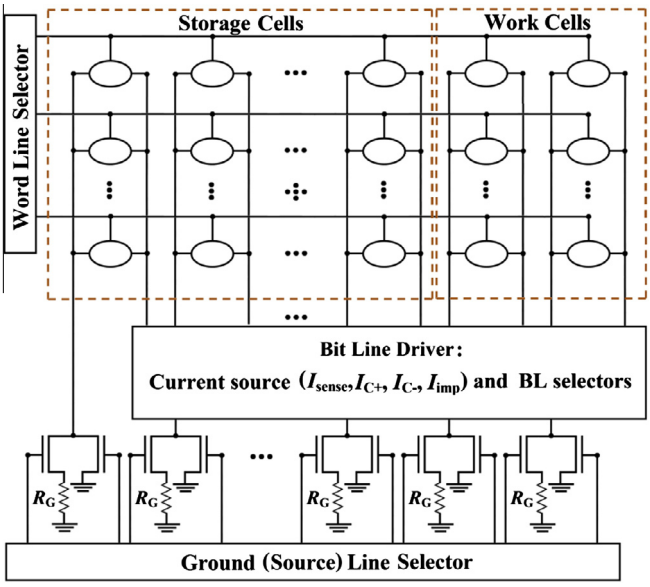

Fig. 9. Simplified spintronic implication logic circuit architecture based on the STT-RAM architecture. Controlling and programming the line drivers and selectors requires an external processor similar to the proposed circuit for the TiO_2-based architecture [9].

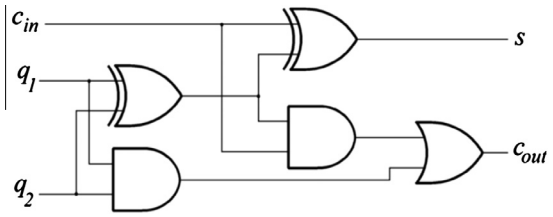

Fig. 10. A logic diagram of a full-adder.

subsequent operations. Therefore, we use the additional cells a_1, a_2, and a_3 to perform two subsequent operations FALSE and IMP, for example ($a_1 \leftarrow 0$ and $a_1 \leftarrow q_1$ IMP 0), to write $\bar{q_1}$ (NOT q_1) in the additional cell a_1 before we use q_1 as a target cell. According to (4)–(6), our design involves only 27 subsequent FALSE and IMP operations on three input cells q_1, q_2, and c_{in}) and three additional cells (a_1-a_3), in contrast to the earlier proposed IMP-based scheme [19] with 19 and 18 operations (37 total) for generating s and c_{out}, respectively, and four additional cells.

$$\{a_1 \leftarrow 0,\ q_1 \text{ IMP } a_1,\ a_2 \leftarrow 0,\quad q_2 \text{ IMP } a_2,\ a_1 \text{ IMP } a_2,\ a_3 \leftarrow 0,\ a_2 \text{ IMP } a_3,\quad a_2 \leftarrow 0,\ q_2 \text{ IMP } a_2,\ a_2 \text{ IMP } a_1,\ a_1 \text{ IMP } a_3\} \equiv \{a_3 \leftarrow q_1 \text{ XOR } q_2\} \tag{4}$$

$$\{q_1 \text{ IMP } a_2,\ q_1 \leftarrow 0,\ a_3 \text{ IMP } q_1,\quad c_{in} \text{ IMP } q_1,\ q_2 \leftarrow 0,\ q_1 \text{ IMP } q_2, a_2 \text{ IMP } q_2\} \quad \equiv \{q_2 \leftarrow c_{out}\} \tag{5}$$

$$\{a_1 \leftarrow 0,\ c_{in} \text{ IMP } a_1,\ q_1 \leftarrow 0,\quad a_3 \text{ IMP } q_1,\ a_1 \text{ IMP } q_1,\ a_1 \leftarrow 0,\quad q_1 \text{ IMP } a_1,\ a_3 \text{ IMP } c_{in},\ a_1 \text{ IMP } c_{in}\} \quad \equiv \{a_3 \leftarrow s = q_1 \text{ XOR } q_2 \text{ XOR } c_{in}\} \tag{6}$$

Therefore, our design requires less operations (delay) and devices (area). As 'p IMP 0' and 'p IMP q' are equivalent to 'NOT p' and '(NOT p) OR q', respectively, some operations can be eliminated to minimize the total effort. In the logic-in-memory circuit presented in [7], the MTJs are used only as ancillary devices which store the result of the logical computations performed by the transistors. Therefore, it requires 34 transistors and four MTJs for implementing a full-adder, while the stateful architecture uses the MTJs as the main devices for computations and eliminates the need of using extra logic gates and offers superior logic density.

4. Conclusion

We have described MTJ-based implication gates as basic elements which inherently realize a logic-in-memory architecture called stateful logic for which the memory and logic computing are combined based on existing STT-MRAM architectures. This opens an alternative path towards non-volatile MTJ-based computing devices and systems [20]. The reliability of the IMP operation is based upon a state dependent modulation (SDM) of the voltage (current) division between the source and target MTJs, which increases exponentially with increasing TMR ratio. Due to non-volatility and also because of eliminating extra charge-based logic gates, the MTJ-based stateful logic is expected to exhibit low power consumption, high logic density, and high speed operation simultaneously.

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