ECS Transactions, 49 (1) 273-280 (2012)
10.1149/04901.0273ecst ©The Electrochemical Society

Analysis of Resistance Change Development due to Voiding in Copper Interconnects ended by a Through Silicon Via

R. L. de Orio[a], H. Ceric[a,b], and S. Selberherr[a]

[a] Institute for Microelectronics, TU Wien
Gußhausstraße 27-29/E360, A-1040 Wien, Austria
[b] Christian Doppler Laboratory for Reliability Issues in Microelectronics
at the Institute for Microelectronics
Email: {orio|ceric|selberherr}@iue.tuwien.ac.at

The resistance change due to electromigration induced voiding in modern copper interconnects ended by a Through Silicon Via (TSV) is analyzed. It is shown that two different modes of resistance increase exist during the period of void growth under the TSV. Primarily responsible are imperfections at the TSV bottom introduced during the fabrication process. Consequently, the time to failure of such structures under electromigration stress is likely to follow a bimodal distribution. An analytical model is proposed to explain the resistance change development based on published experimental data and also on numerical simulations.

Introduction

Three-dimensional (3D) integration has become a very promising technology for the microelectronics industry. Among its main advantages are: high density integration, multifunctionality, better performance, reduced power, heterogeneous integration, etc (1). One key component of 3D integration to achieve these features is the Through Silicon Via (TSV) (2). The TSV consists of a conducting via fabricated trough a silicon substrate, which connects components of different integration levels (1).

Reliability is a critical issue for new emerging technologies, in particular, for TSVs (3). Electromigration (EM) is one of the main reliability concerns in backend of line (BEOL) interconnects. EM failure mechanisms have been extensively studied for copper dual-damascene interconnects, where failure is characterized by the resistance increase with time associated to EM induced material transport. Typically, resistance measurements show an initial period with very small resistance change, followed by a subtle increase phase and further linear growth (4).

Frank *et al.* (5) have shown that for structures with a TSV formed on a pad at the cathode end of line the resistance development is somewhat different. They have observed that the subtle resistance increase phase does not occur, so that the interconnect resistance remains initially constant and then starts to increase following a logarithmic time dependence. Based on failure analysis methods it was shown that this behavior is due to the growth of a large void under the TSV and concluded that this is the major failure mechanism in such structures.

In this work we investigate the resistance change development in copper dual-damascene lines with a TSV located at the cathode end of the line due to voiding under

the via. The resistance change of such interconnect structures is studied based on 3D numerical simulations. We show that imperfections at the TSV bottom originating from the fabrication process can lead to an additional failure mechanism, where a significant resistance increase is caused by small voids under the TSV. In addition, an analytical model is proposed to describe this failure mechanism.

Modeling

In (5) EM experiments using downstream electron flow show void formation and growth under the TSV at the cathode end of a line as sketched in Figure 1. It has been observed that the development of the resistance as a function of time can be divided in two periods: at first the resistance remains practically constant, which is then followed by a measurable resistance increase. Failure analyses have indicated that during the first period the void diameter is smaller than the TSV section, while the measurable resistance increase period starts as soon as the void diameter becomes larger than the TSV section.

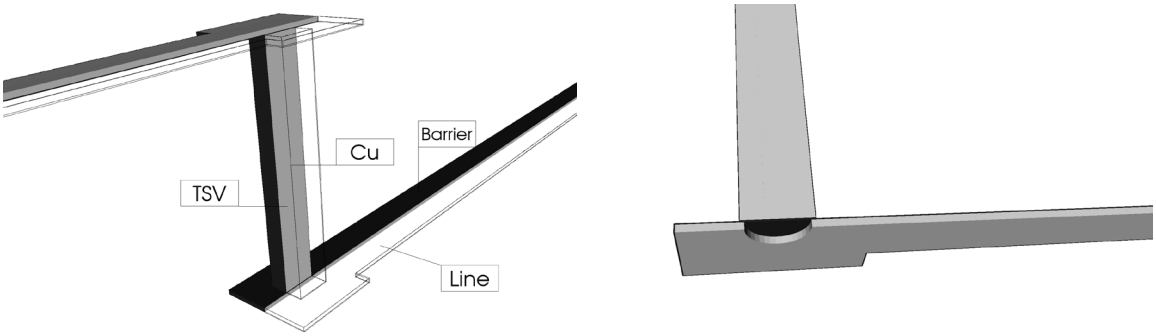

Figure 1. Full interconnect structure (left) and vertical cut through the structure showing the TSV bottom and the void in detail (right).

Considering a cylindrical void under the TSV, as shown in Figure 1, and that $r_{void} > r_{\mathrm{TSV}}$, the resistance change is modeled as (5)

$$\Delta R(r_{void}) = \frac{\rho_b}{2\pi t_b} \ln\left(\frac{r_{void}}{r_{TSV}}\right), \quad r_{void} > r_{TSV} \qquad [1]$$

where r_{void} and r_{TSV} are the void and the TSV radii, respectively, ρ_b is the barrier resistivity, and t_b is the barrier layer thickness at the bottom of the via. The resistance change as a function of time is determined by the void radius growth with time. Assuming that the void volume is formed by capturing vacancies driven by the electromigration force and that the vacancy flux is constant, the void volume at a time t is given by (5)

$$V_{void}(t) = \pi h r_{void}^2(t) = A_l v_d t\,, \qquad [2]$$

where h is the copper line thickness, A_l is the line cross sectional area, and v_d is the vacancy drift velocity. Thus, for isotropic void growth the void radius as a function of time is written as

$$r_{void}(t) = \sqrt{\frac{A_l v_d t}{\pi h}}\,. \qquad [3]$$

Since the vacancy drift velocity is given by (6)

$$v_d = \frac{D_v e Z^* \rho j}{kT}, \qquad [4]$$

the resistance change as a function of time is obtained by combining eq. [1], eq. [3], and eq. [4], yielding (5)

$$\Delta R(t) = \frac{\rho_b}{4\pi t_b} \ln\left(\frac{t}{t_0}\right), \quad t > t_0 \qquad [5]$$

with

$$t_0 = \frac{\pi h r_{TSV}^2}{A_l v_d} = \frac{\pi h r_{TSV}^2 kT}{A_l D_v e Z^* \rho j}\,. \qquad [6]$$

D_v is the vacancy diffusivity, eZ^* is the effective charge, ρ is the copper resistivity, and j is the applied current density. t_0 is the time at which the void radius becomes equal to the radius of the TSV and the logarithmic resistance increase starts. Thus, eq. [5] is valid for the period $t > t_0$, that is $r_{void} > r_{TSV}$.

Although Frank *et al.* (5) assumed that the resistance trace is constant for $t < t_0$ (i.e. $r_{void} < r_{TSV}$), void growth under the TSV leads, in fact, to a small resistance increase which cannot be experimentally measured. In this case the resistance change is caused by the reduction of the effective conducting area in relation to the cross sectional area of the TSV. Therefore, the resistance change is given by

$$\Delta R(r_{void}) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left[\frac{\left(r_{void}/r_{TSV}\right)^2}{1-\left(r_{void}/r_{TSV}\right)^2}\right], \quad r_{void} < r_{TSV} \qquad [7]$$

which together with eq. [3] and eq. [4] yields

$$\Delta R(t) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left(\frac{t/t_0}{1-t/t_0}\right), \quad t < t_0 \qquad [8]$$

for the resistance change as a function of time for small voids.

It should be pointed out that the models derived above assume a circular TSV, while the via used in the experimental test structure described in (5) and also used in this work is approximately squared. Therefore, r_{TSV} should be viewed as an effective via radius. This does not affect the modeling and later we will show that r_{TSV} can be determined by

fitting eq. [1] and eq. [7] to the curves of resistance change as a function of void radius obtained from numerical simulations.

Results and Discussion

The resistance change caused by the growth of a void located under the TSV was determined from numerical simulations. The geometry, dimensions, and material parameters of the interconnect structure were obtained from (5). A detailed view of the structure and void at the TSV bottom is shown in Figure 1.

Considering the modeling described above, a cylindrical void is placed under the via and its radius is gradually incremented. For each void size the resistance of the interconnect is determined from the numerical solution of the Laplace equation. In this way we are able to extract the resistance change of the interconnect shown in Figure 1 for the whole period of void growth.

Figure 2 shows the electron current density distribution at the TSV bottom in the presence of a void. The void causes a reduction of the effective conducting area at the TSV bottom. The electron flow is displaced towards the corners of the via, which leads to current crowding in this region, as can be readily seen in Figure 2.

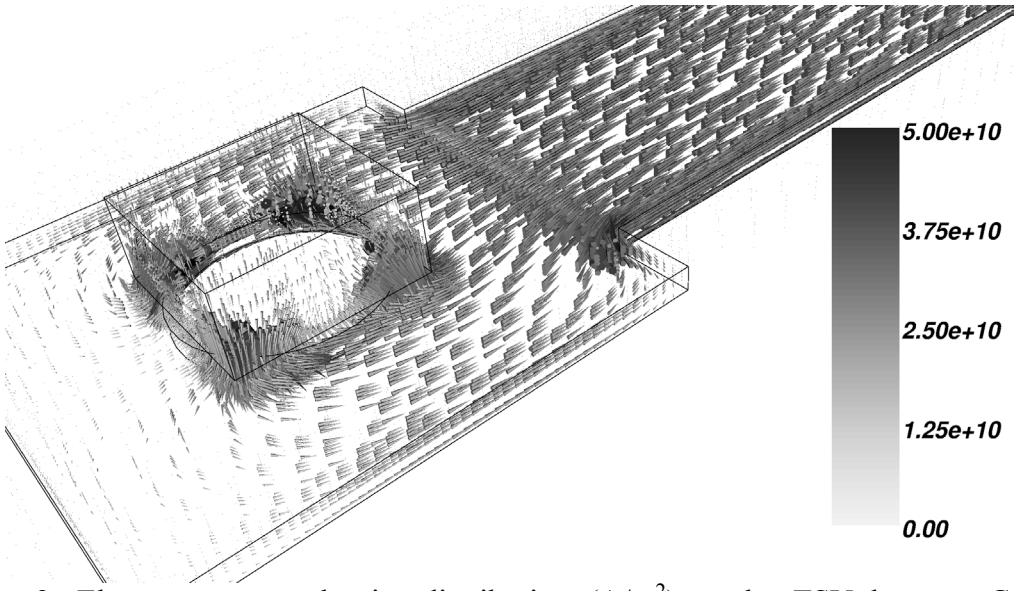

Figure 2. Electron current density distribution (A/m^2) at the TSV bottom. Current crowding towards the corners of the via due to the void can be observed.

The resistance change as a function of void radius is shown in Figure 3. The resistance change is practically negligible for small void radii ($r_{void} < 1.4\mu m$). For larger voids, however, a significant resistance increase is observed. Note that the void radius axis is plotted in logarithmic scale and that the resistance appears to closely follow a linear increase. Below we investigate the resistance change curve shown in Figure 3 in more detail and verify the modeling previously described.

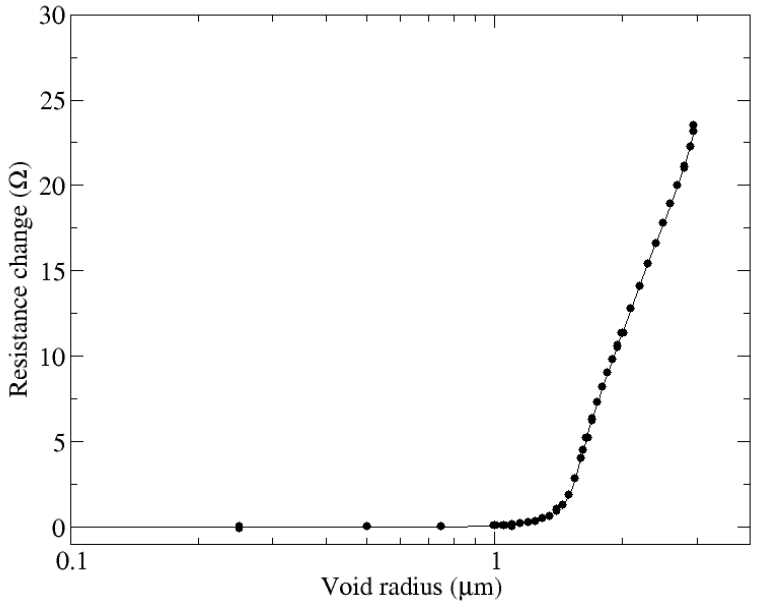

Figure 3. Numerical simulation of resistance change as a function of void radius.

Resistance change for large voids ($r_{void} > r_{TSV}$)

The resistance change of the interconnect line as a function of the void radius for the range $r_{void} > r_{TSV}$ is shown in Figure 4. The symbols represent numerical simulation results obtained at different void sizes. The solid line is a fit to the simulated data according to the model given in eq. [1]. One can clearly see that the model correctly describes the resistance change for the tested void radius range. Furthermore, the numerical simulation results reproduce the logarithmic resistance increase suggested by Frank *et al.* (5). By fitting eq. [1] to the simulations we have obtained as effective TSV radius $r_{TSV} = 1.44\mu m$.

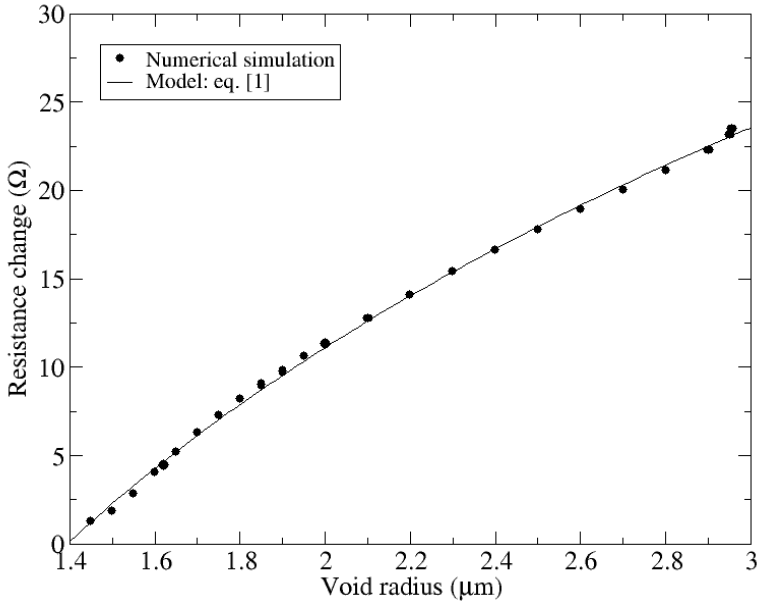

Figure 4. Interconnect resistance change for $r_{void} > r_{TSV}$.

Resistance change for small voids ($r_{void} < r_{TSV}$)

The simulated resistance change as a function of void size for $r_{void} < r_{TSV}$ is shown in Figure 5. Although the magnitude of the resistance change is small, a rapid increase is expected as the void grows. One can see that a very good agreement between the numerical simulations and the analytical model given by eq. [7] is obtained. Here, the estimated effective void radius is r_{TSV} = 1.38μm, which is very close to the value previously determined for the large void case.

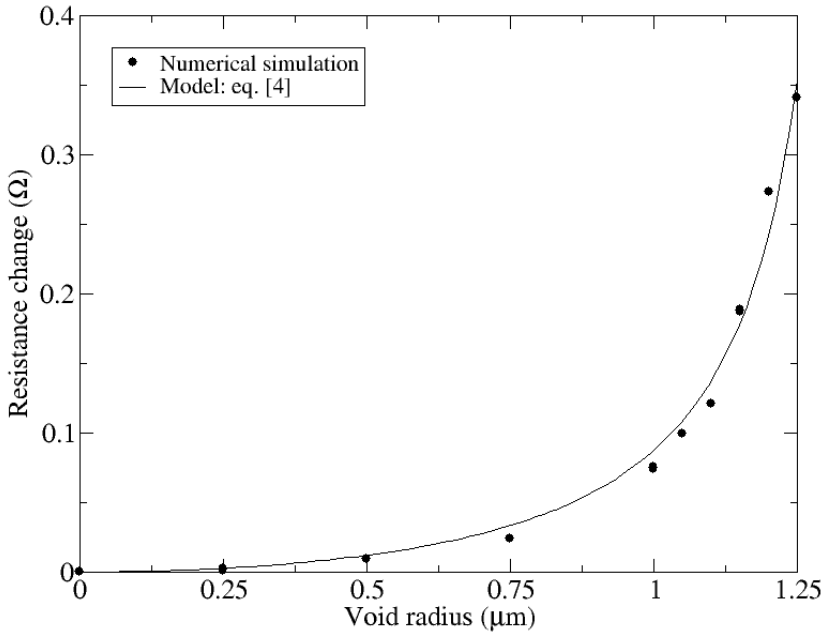

Figure 5. Resistance change for $r_{void} < r_{TSV}$. A good agreement between numerical simulations and the analytical model given by eq. [7] is obtained.

Since the resistance increase for $r_{void} < r_{TSV}$ is rather small, EM failures are, in principle, expected to occur for the range $r_{void} > r_{TSV}$ (5), so the interconnect lifetime is obtained from eq. [5]. However, imperfections on the bottom of the TSV are normally introduced during the fabrication process of such structures (7). In particular, control of the thin barrier layers at the bottom of the TSV is a key issue and has a significant impact on the structure reliability.

As a consequence of such imperfections, Frank *et al.* (5) observed a large variation of the barrier layer resistivity estimated from the experimental results, as shown in Figure 6. A variation of about two orders of magnitude for the resistivity is observed. Thus, the barrier resistivity distribution show in Figure 6 can be regarded as the effective parameter which takes into account mainly the dispersion of the barrier layer thickness of the TSV bottom.

The impact of such variations on the resistance change for small voids under the TSV is shown in Figure 7, where the resistance increase as a function of void radius is plotted for three different values of barrier resistivity. The variation of the effective barrier resistivity affects the structure resistance significantly, leading to a large resistance increase, even when the void size is smaller than the via section. Considering the typical 10% resistance increase as failure criterion, we estimate that for $\rho_b > 4000\mu\Omega$.cm the interconnect failure is triggered also for smaller voids under the TSV ($r_{void} < r_{TSV}$). It should be pointed out that these failures form an additional failure mode. Moreover, since a shorter time is needed to grow a smaller void, this failure mechanism constitutes an early failure mode.

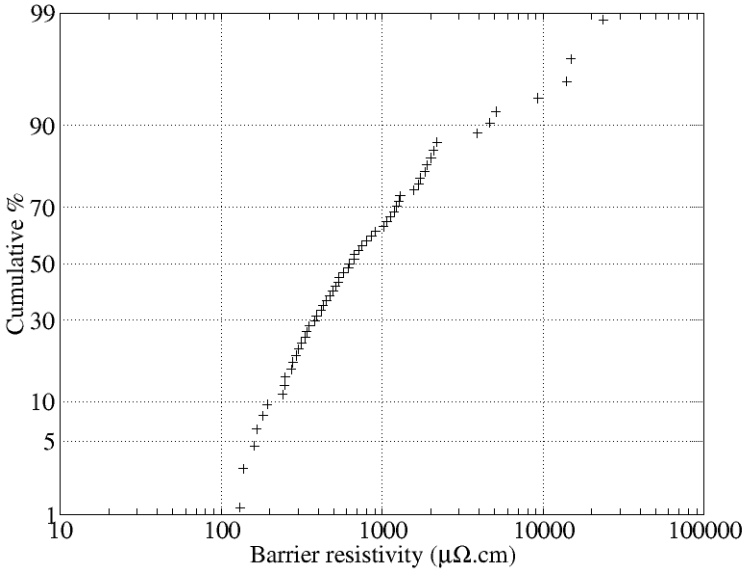

Figure 6. Barrier resistivity distribution extracted from (5). The large dispersion indicates the existence of imperfections at the TSV bottom introduced during the fabrication process.

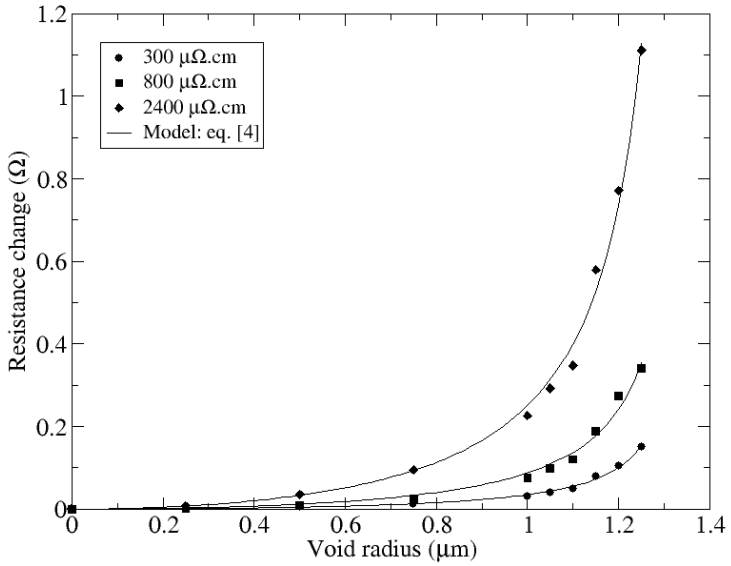

Figure 7. Resistance change as a function of void radius ($r_{void} < r_{TSV}$) for different values of barrier resistivity.

Figure 6 shows that a high barrier resistivity (ρ_b > 4000μΩ.cm) is found at a cumulative percentile of about 90%. This means that the early failures would only be "visible" in lifetime distribution curves for low cumulative percentiles, significantly less than 10%. In this way the characterization of this mode requires a large number of tests. Considering that the reliability assessment of an interconnect is typically performed at very low failure percentiles, the early failures described above are likely the most relevant ones for EM induced degradation in copper dual-damascene line/TSV structures.

Conclusion

It was shown that small voids under the via of a copper dual-damascene line/TSV structure generated by EM material transport can cause a significant interconnect resistance increase in the presence of imperfections on the TSV bottom produced during the fabrication steps. We have proposed a model which satisfactorily describes this resistance increase. In addition, we verified that upon triggering the line failure, this mechanism forms an extrinsic, early failure mode which acts primarily at low cumulative percentiles, and is expected to have a significant impact on the interconnect reliability assessment.

Acknowledgments

The authors would like to thank T. Frank for helpful discussions. This work was supported by the Austrian Science Fund FWF, project P23296-N13, and also by the European Union Project COCOA.

References

1. J.-Q. Lu, K. Rose, and S. Vitkavage, *Future Fab Intl.*, **23**, 25 (2007).
2. M. Motoyoshi, *Proc. of the IEEE*, **97**, 43 (2009).
3. M. Koyanagi, *Proc. IEEE Intl. Reliab. Phys. Symp.*, 328 (2011).
4. L. Doyen, E. Petitprez, P. Waltz, X. Federspiel, L. Arnaud, and Y. Wouters, *J. Appl. Phys.*, **104**, 123521 (2008).
5. T. Frank, C. Chappaz, P. Leduc, L. Arnaud, F. Lorut, S. Moreau, A. Thuaire, R. El Farhane, and L. Anghel, *Proc. IEEE Intl. Reliab. Phys. Symp.*, 347 (2011).
6. Z. S. Choi, R. Monig, and C. V. Thompson, *J. Appl. Phys.*, **102**, 083509 (2007).
7. T. Frank, C. Chappaz, P. Leduc, L. Arnaud, S. Moreau, A. Thuaire, R. El Farhane, and L. Anghel, *Proc. IEEE Electronics Packaging Technology Conf. (EPTC)*, 321 (2010).