TCAD Study of Electromigration Failure Modes in Sn-Based Solder Bumps

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Abstract—**For the realization of modern integrated circuits new interconnect structures like through-silicon-vias and solder bumps, together with complex multilevel 3D interconnect structures are gaining importance. The application of these new structures unavoidably rises different reliability issues like thermal gradients, electromigration, and stressmigration. In this paper we apply state-of-the art TCAD methods for studying electromigration in Sn solder bump. The results and discussion of the studied case have essentially improved the understanding of the role of Sn crystal anisotropy in degradation mechanism of solder bump.**

Keywords: 3D interconnects, electromigration, reliability, simulation

I. INTRODUCTION

Three-dimensional (3D) integration is an emerging technology which can form highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components. The potential benefits of 3D integration can vary depending on the utilized approach; they include multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs. 3D technologies can be divided into three categories based on their similarity to other technologies:

- 3D packaging technology
- 3D transistor build-up technology
- Wafer-level BEOL-compatible 3D technology

Each of these technologies has its specific electromigration (EM) and stress related reliability issues. EM and stress induced degradation act closely together and, in most cases, it is impossible to separate their impact on materials building specific interconnect structures [1]. According to the 2009 International Technology Roadmap for Semiconductors, EM will become a limiting factor for high current density packages [2].
A characteristic of 3D integration is also an increased significance of heat transfer. On a silicon chip, the elements which generate heat are the transistor, the contact metallization, the multilayered Cu and Al interconnects, and the solder bumps. The effect of increased temperature on EM and stress induced degradation is manifold; on one hand it enhances the material transport by increasing diffusivity coefficients; on the other hand, in most of the cases it activates dislocation movements producing complex plastic effects both in metals and semiconductors [3].
Solder bump is a crucial component for high performance 3D packaging technology. Many experimental studies of solder bumps have been focused on various combinations of under bump metallization (UBM), solder composition, and far back end of line (FBEOL) structure to improve current density distributions and consequently EM reliability [4]. Pb-free solders are today widely used in many commercial products; however, their reliability for high-performance logic chip application still needs to be further improved [5].
In this work TCAD based analyses of solder bump structures and their EM failure behavior described in [6] are carried out. The Sn solder bump is connected to the Cu metallization by UBMs. The UBM on the upper (cathode) side of the solder bump consists of a Ni barrier layer and on the bottom (anode) side the contact is realized by stacking TiW, Ni, and Cu layers. At the interface between Ni and Sn, an inter-metallic compound (IMC) is established (cf. Fig. 1).
During EM testing two failure modes are observed:

- Mode 1. The cathode Ni barrier layer and the IMC remain intact, while EM induced voids are formed at the Sn solder bump interface to the IMC.
- Mode 2. The Ni barrier layer and the IMC are depleted and swept away. Inside the Ni layer a void is formed.

For the understanding of this failure behavior first the role of metal microstructure in EM should be discussed.

II. MICROSTRUCTURE AND EM

Microstructure is defined by a network of grain boundaries and by the crystal orientation inside the grains. The network of grain boundaries influences vacancy transport during EM in several ways.

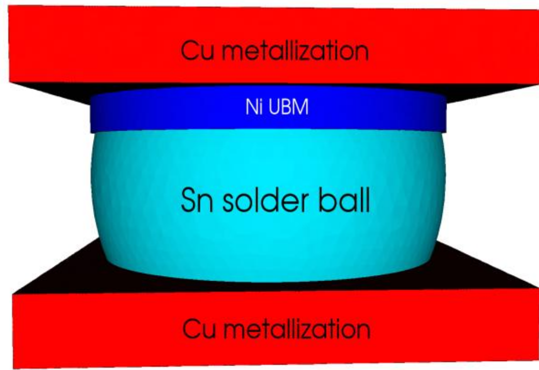

Figure 1. Solder bump structure used for simulation.

The diffusion of point defects inside the grain boundary is faster when compared to grain bulk diffusion [7], since a grain boundary generally exhibits a larger diversity of point defect migration mechanisms. Moreover, formation energies and migration barriers of point defects are, on average, lower than those for the lattice. In polycrystalline metals, grain boundaries are also recognized (together with dislocation loops) as sites of vacancy generation and annihilation [7], [8]. Therefore, the EM failure rate should depend on the grain size of the metallization. This dependence is well documented for Al interconnects; however, the dependence is found to be less pronounced in Cu interconnects. The probable reason is that EM dominates along interfaces in Cu interconnects [9].

The Sn solder bump microstructure and interface reaction also play an important role in failure scenarios. Sn solder bumps often consist of several large Sn grains, such that most solder bumps exhibit one or at most a few Sn grain orientations [10]. Sn has a bulk tetragonal crystal structure which exhibits highly anisotropic diffusional, mechanical, thermal, and electrical properties [11].

A clear dependence of the thermo-mechanical response of a Sn solder bump on microstructure and Sn grain orientation was also observed [10]. The coefficient of thermal expansion is higher in the *c*-axis direction than in *a*- or *b*-axis directions.

III. THEORETICAL MODEL

A general, three-dimensional expression for the vacancy flux $\vec{J}_v$ driven by gradients of the chemical potential and EM is given by

$$\vec{J}_v = \frac{C_v}{k_B T} \overline{\overline{D}}_v (\nabla \mu_v + |Z^*| e \nabla \varphi). \quad (1)$$

The meaning of the symbols is as in [12]. Here we also introduce a tensorial diffusivity $\overline{\overline{D}}_v$ which describes the anisotropy of vacancy transport caused by the crystal properties and the influence of mechanical deformation.

The vacancy flux expression (1) and the models based on it have been widely used for the analysis of EM in dual-damascene copper interconnects. In order to model EM in solder bumps which, in addition to host atoms (e.g. Sn), also include impurity atoms (e.g. Ni, Cu), (1) must be extended. We assume that, prior to EM stressing, all impurity atoms have occupied substitutional positions. Thus, after applying electric current, EM removes the impurity atoms from their substitutional sites and causes them to drift. Each drifting host or impurity atom induces a movement of vacancies in a direction opposite to its drifting direction and the total vacancy flux is composed of the vacancies produced by the host atoms and the impurity atoms.

The total flux $\vec{J}_v^T$ is given by

$$\vec{J}_v^T = \vec{J}_v + \sum_i \vec{J}_v^i. \quad (2)$$

Here, $\vec{J}_v^i$ is the vacancy flux corresponding to impurity i and $\vec{J}_v$ is the flux of the host vacancies. $\vec{J}_v^i$ are expressed by expressions similar to (1), but specific diffusivity coefficients and effective charges must be used. Particularly, the effective charges can vary significantly [13],[14].

Today we use sophisticated, quantum mechanics based methods in order to calculate the effective charges [15], [16], [17]. From [15], for example, at 473 K for Pb self-EM we have $Z^* = -3.4$, for Cu in Pb $Z^* = -0.6$, and for Sn in Pb $Z^* = -7.0$.

Since the vacancy volume is smaller than the volume of the atom, the EM gives rise to mechanical stress. The kinetic relation for the evolution of the strain tensor $\overline{\overline{\varepsilon}}$ caused by vacancy migration and recombination from [12], [18] is

$$\frac{\partial \varepsilon_{ij}}{\partial t} = \frac{\Omega}{3}\left((1-f)\nabla \cdot \vec{J}_v^T + f\gamma\right)\delta_{ij}, \quad (3)$$

where γ is the source term which describes the vacancy recombination and annihilation process, *Ω* is the volume of the atom, and f is the atom-vacancy relaxation factor.

For an undistorted crystal, the tensoral diffusivity $\overline{\overline{D}}_v$ is determined by [12] , [19]

$$D_{v,ij} = \frac{6D_0}{Z}\sum_{k=1}^{Z} a_i^k a_j^k \, e^{-\frac{E_S^k - E_e}{k_B}}. \quad (4)$$

Z is the number of neighboring jump sites, a_i^k are the components of unit jump vectors for each jump site (direction), E_S^k and E_e are the energy barrier for jump direction k and the energy at the initial atom position, respectively. D_0 is the vacancy diffusivity in the ideal crystal lattice [20].

$$D_0 = \frac{1}{12} Z\, \Gamma_0 \lambda^2 \quad (5)$$

λ is the mean vacancy jump length and Γ_0 is the atom jumping frequency.

IV. Simulation Results and Discussion

We have utilized an interconnect structure as presented in Fig.1. This structure consists of a Sn based solder bump with Ni under bump metallization at the cathode end. The cathode and anode ends are connected to copper interconnect layers.
In order to study the complete problem we must consider EM in both Ni and Sn segments as well as at their interface.
As we know from experimental observations, at the interface between Ni and Sn, an inter-metallic compound is formed.
EM in the Sn and Ni segment is described by the standard EM model [12]. For IMC we assume at first a simple Ni segregation model [21]. Ni has a face-centered cubic crystal and in the unstressed state self-diffusion and EM in such crystals is isotropic. In this work the predominant focus is on the effects of EM; therefore, the models for stress induced anisotropy of the diffusivity tensor are neglected [22].
The isotropic self-diffusivity coefficient of Ni is [23]

$$D_{Ni} = 2.9 \exp\left(-\frac{2.88\ eV}{k_B T}\right)\frac{cm^2}{s}. \qquad (6)$$

Measurements of self-diffusion in Sn clearly show an anisotropic atomistic transport. From [24],[25] we have

$$D_{c,Sn} = 3.7\ 10^{-8} \exp\left(-\frac{0.25\ eV}{k_B T}\right)\frac{cm^2}{s}, \qquad (7)$$

$$D_{a,Sn} = D_{b,Sn} = 8.4\ 10^{-4} \exp\left(-\frac{0.45\ eV}{k_B T}\right)\frac{cm^2}{s}. \qquad (8)$$

First we consider failure Mode 1. Here the *c*-axis of the Sn grain exibits a large angle with the current direction, where the rate of Ni diffusion in Sn is small. Failure is mainly due to Sn self-EM, resulting in a peak vacancy concentration between the IMC and solder (cf. Fig.2).

By rotating the Sn crystal by 90°, the crystal *c*-axis becomes aligned with the electric current direction. Ni atoms are transported from the Ni layer through the IMC into the solder bump below, where they electromigrate rapidly along the *c*-axis. At this instance, the peak in vacancy concentration occurs in the UBM Ni layer as can be seen in Fig.3. The locations of vacancy concentration peaks in both failure modes correspond to sites of peaks of tensile stress, which are sites of void nucleation.

Our simulations have shown that the crystal orientation in a Sn solder bump cannot be the sole reason for the difference in EM behavior between Mode 1 and Mode 2. Even if the EM of Ni in the *a*- and *b*-axis direction is much smaller than the EM in the *c*-axis direction, it is still higher than Sn self-EM, so we would expect similar behavior in both failure modes. We conclude that the structure of the transition region (IMC) plays a significant role. This structure, in the case when the Ni layer is attached to the *a*- or *b*-axis oriented crystal, is such that it represents a barrier for EM of Ni atoms. In our simulation we applied a segregation model [22] to describe the capturing of Ni atoms in IMC.
The anisotropy of Ni diffusion in Sn is much more pronounced than the anisotropy of Sn self-diffusion. In the case of fast *c*-axis Ni diffusion in Mode 2 we have an additional effect: the Sn crystal orientation produces an IMC structure which is preconditioned for a fast dissolution. This dissolution subsequently drowns atoms from the UBM causing the failure in Mode 2.
More detailed simulations by means of molecular dynamics will be necessary in order to design a more accurate phenomenological model for IMC.

In Fig. 4 we compare the time dependent rise in the vacancy concentration due to Sn self-diffusion and self-EM for different crystal orientations. Three cases are studied:

- c-axis is parallel to electric current direction
- c-axis is rotated by θ = 30◦
- c-axis is rotated by θ = 60◦

The impact of IMC and Ni-related vacancy-influx is neglected in order to obtain a clear picture of the influence of crystal anisotropy on material transport.

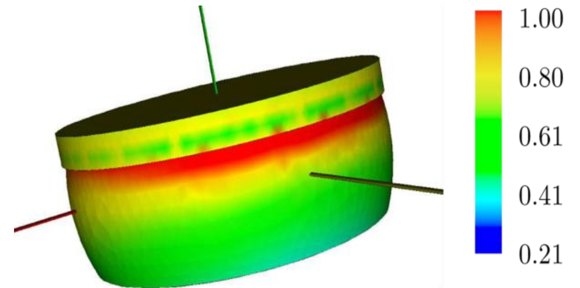

Figure 2. Normalized vacancy distribution in failure Mode 1. Peak concentration is reached in the bump.

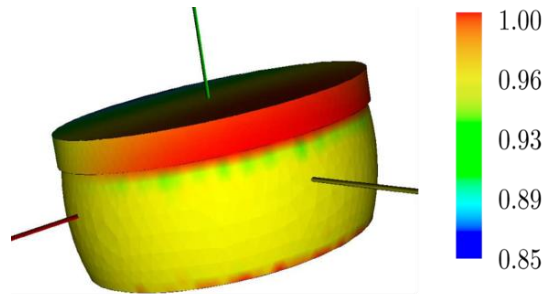

Figure 3. Failure Mode 2 - large portion of UBM with high vacancy concentration.

As we can see in Fig.4, a crystal rotation causes a reduction of the EM intensity. We denote with θ an angle between the current density and the *c*-axis of the crystal. By comparing the curves for $\theta = 0^\circ$ and $\theta = 60^\circ$ we see that the vacancy concentration at $\theta = 0^\circ$ keeps rising, while the curve at $\theta = 60^\circ$ stays almost at equilibrium. This result helps to

understand the experimental observation of failure development in solder bumps which consist of two large grains. In these cases the grain with *c*-axis oriented in parallel to the electron flow is completely swept away, while the other grain is still intact [11].

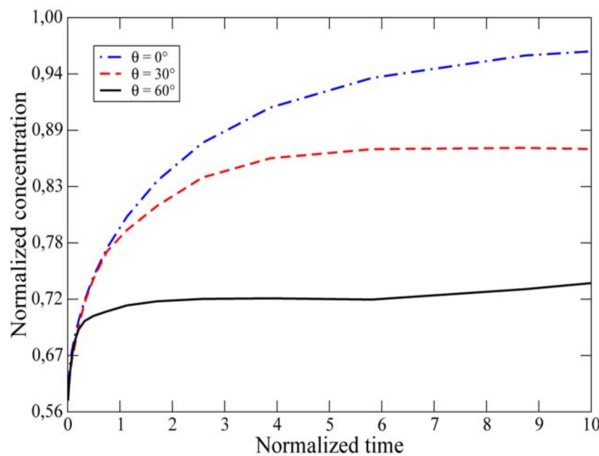

Figure 4. Increase in vacancy concentration in failure Mode 1 for three different crystal orientations.

V. CONCLUSION

In this work we present a TCAD reliability study of a solder bump technology for 3D ICs. The study of EM in Pb-free solder bumps has enabled new insights in the specific degradation mechanism in UBMs and IMCs caused by the anisotropy of crystalline Sn. Depending of the Sn crystal orientation EM of Sn and Ni is enhanced or retarded. The structure and the role of IMC is also influenced by the crystal orientation. A physical model of EM in anisotropic crystalline Sn has been used as a basis for the investigation of the failure behavior for a realistic solder bump structure by means of simulation.

The presented study as well as its further application and development provide significant support for interconnect design engineers.

[1] S.-K. Ryu, K.-H. Lu, X. Zhang, J.-H. Im, P. S. Ho, and R. Huang, "Impact of Near-Surface Thermal Stresses on Interfacial Reliability of Through-Silicon-Vias for 3-D Interconnects," IEEE Trans. on Device and Material Reliability, vol.11, no. 1, pp. 35-43, 2011.

[2] International Technology Roadmap for Semiconductors 2009.

[3] P. S. Ho and T. Kwok, "Electromigration in Metals," Rep. Prog. Phys., vol. 52, no. 3, pp. 301-348, 1989.

[4] B. Ebersberger and C. Lee, "Cu Pillar Bumps as a Lead-Free Drop-in Replacement for Solder-Bumped, Flip-Chip Interconnects," Proc. Electronic Components and Technology Conf., pp. 59-66, 2008.

[5] J.-S. Yang, K. Athikulwongse, Y.-J. Lee, S. K. Lim, and D. Z. Pan, "TSV Stress Aware Timing Analysis with Applications to 3D-IC Layout Optimization,"Proc. ACM Design Automation Conf., pp. 803-806, 2010.

[6] M. Lu "Effect of Microstructure on Electromigration in Pb-Free Solder Interconnect," Stress-Induced Phenomena in Metallization, AIP, pp. 229-234, 2010.

[7] M. R. Sorensen, Y. Mishin and A. F. Voter, "Diffusion Mechanisms in Cu Grain Boundaries," Phys. Rev. B, vol. 62, no. 6, pp. 3658-3673, 2000.

[8] R. W. Balluffi,"Grain Boundary Diffusion Mechanisms in Metals, "Metallurgical Transactions A, vol. 13, pp. 2069-2095, 1982.

[9] C. K. Hu and J. M. E. Harper, "Copper Interconnections and Reliability," Mater. Chem. Phys., vol. 52, no. 1, pp. 5-16, 1999.

[10] T. R. Bieler, H Jiang,L. P. Lehman, T. Kirkpatrick, E. J. Cotts, and B. Nandagopa, IEEE Trans. Comp. Pack. Techn. "Influence of Sn Grain Size and Orientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints," vol. 31, nr. 2, pp. 370-381, 2008.

[11] C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, "Microstructure-Electromigration Correlation in a Thin Stripe of Eutectic SnPb Solder Stressed Between Cu Electrodes," Appl. Phys. Lett., vol. 75, no. 1, pp. 58-60, 1999.

[12] H. Ceric, R. Heinzl, Ch. Hollauer, T. Grasser, and S. Selberherr, "Microstructure and Stress Aspects of Electromigration Modeling," Stress-Induced Phenomena in Metallization, AIP, pp. 262-268, 2006.

[13] H. B. Huntington and A. R. Grone, "Current-Induced Marker Motion in Gold Wires," J. Phys. Chem. Solids, vol. 20, no. 1/2, pp. 76-87 1961.

[14] N. A. Ashcroft and N. D. Mermin, Solid State Physics, Holt, Rinehart and Winston, 2003.

[15] J. P. Dekker and A. Lodder, J. Appl. Phys., "Calculated Electromigration Wind Force in Face-Centered-Cubic and Body-Centered-Cubic Metals," vol. 84, nr. 4, pp. 1958-1962, 1998.

[16] J. P. Dekker, A. Lodder, and J. van Ek, Phys. Rev. B., "Theory for the Electromigration Wind Force in Dilute Alloys," vol. 56, nr. 19, pp. 12167-12177, 1997.

[17] J. van Ek, J P. Dekker and A. Lodder, Phys. Rev. B., "Electromigration of Substitutional Impurities in Metals," vol. 52, nr. 19, pp. 8794-8800, 1995.

[18] M. E. Sarychev and Yu. V. Zhitnikov, "General Model for Mechanical Stress Evolution During Electromigration," J. Appl. Phys., vol. 86, no. 6, pp. 3068-3075, 1999.

[19] K. Schroeder and K. Dettmann, "Diffusion Reactions in Long Range Potentials," Z. Physik B, vol. 22, pp. 343-350, 1975.

[20] M. E. Glicksman, Diffusion in Solids, John Wiley and Sons, Inc., 2000.

[21] F. Lau, L. Mader, C. Mazure, C. Werner, and M. Orlowski, "A Model for Phosporus Segregation at the Silicon - Silicon Dioxide Interface," Appl. Phys. A, vol. 49, pp. 671-675, 1989.

[22] R. L. de Orio, H. Ceric, and S. Selberherr, "Effect of Strains on Electromigration Material Transport in Copper Interconnect Structures under Electromigration Stress," J. Comp. Electronics, vol. 7, no. 3, pp. 128-131, 2008.

[23] A. R. Wazzan and J. E. Dorn, "Analysis of Enhanced Diffusivity in Nickel," J. Appl. Phys., vol. 36, no. 1, pp. 222-228, 1965.

[24] P. H. Sun and M. Ohring, "Tracer Self-Diffusion and Electromigration in Thin Tin Films," J. Appl. Phys., vol. 47, no. 2, pp. 478-485, 1976.

[25] D. C. Yeh and H. B. Huntington, "Extreme Fast-Diffusion System: Nickel in Single-Crystal Tin," Phys. Rev. Lett., vol. 53, no. 15, pp. 1469-1472, 1984.