Reliability of SiGe channel MOS

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Due to the ever increasing electric fields in scaled CMOS devices, reliability is becoming a show stopper for further scaled technology nodes. Although several groups have already demonstrated functional Si channel devices with aggressively scaled EOT down to 5Å [1,2], a 10 year device lifetime at operating voltage cannot be guaranteed anymore [3,4] due to severe Negative Bias Temperature Instability (NBTI) [5], as depicted in Fig. 1 (diamonds).

Meanwhile, the use of high-mobility channels is being considered for further enhancement of CMOS performance [6]. The SiGe channel quantum well (QW) technology (Fig. 2) in particular is considered for yielding enhanced mobility and pMOS threshold voltage tuning [7].

Already in 2009 we have observed that this technology also offers a significant reliability improvement [8]. In particular a considerably reduced Negative Bias Temperature Instability was observed. A very effective reliability oriented optimization of the SiGe gate-stack was developed, including a high Ge fraction (55%) in the channel, a sufficiently thick SiGe QW (6.5nm) and a Si passivation layer of reduced thickness (0.8nm) [9]. By means of such optimization, sufficiently reliable ultra-thin EOT SiGe pMOSFETs with a 10 year lifetime at operating conditions were successfully demonstrated in both gate-first and gate-last process flows (Fig. 1) [3,10].

Furthermore, the reliability improvement was observed to be process and architecture independent, proving to be an intrinsic property of the Ge-based technology, and therefore readily transferable to different device architectures such as pure Ge-channel pMOSFETs and SiGe pFinFETs [10].

We ascribe this intrinsic reliability improvement to a reduced interaction between channel carriers and defects in the gate dielectric. In particular, assuming the existence of a defect band in the dielectric centered below the Si valence band (as observed e.g. in [11]), fewer defects are energetically favorable for trapping holes from the SiGe channel, thanks to the higher Fermi level energy in the small-bandgap SiGe QW (Fig. 3a). This simple model can explain the experimental observations, including the impact of different Ge fractions, QW thickness, and Si cap thickness on the device NBTI reliability (Fig. 3b&c).

Refs. : [1] L.-Å. Ragnarsson *et al.*, in *Proc.* IEDM 2009; [2] T. Ando *et al.*, in *Proc.* IEDM 2009; [3] J. Franco *et al.*, in *Proc.* IEDM 2010; [4] E. Cartier *et al.*, in *Proc.* IEDM 2011; [5] T. Grasser *et al.*, TED 58(11), 2011; [6] J. Mitard *et al.*, in *Proc.* IEDM 2010; [7] S. Krishnan *et al.*, in *Proc.* IEDM 2011; [8] B. Kaczer *et al.*, Micr. Eng. 86(7-9), 2009; [9] J. Franco *et al.*, in *Proc.* IRPS 2010; [10] J. Franco *et al.*, in *Proc.* IEDM 2011; [11] T. Nagumo *et al.*, in *Proc.* IEDM 2010.

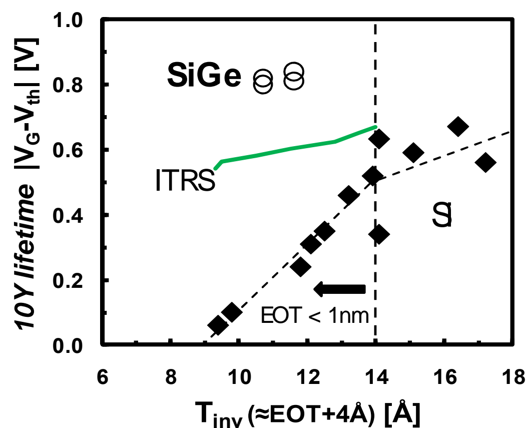


Fig. 1. Due to severe NBTI, ultra-thin EOT Si channel pMOSFETs do not allow for a 10 year lifetime at the ITRS specified operating voltage. Conversely, optimized ultra-thin EOT SiGe channel pMOSFETs show significantly reduced NBTI, clearly overcoming the operating voltage target. The reliability improvement is consistently reproduced for different process thermal budgets and for both a Metal Inserted Poly-Si (gate-first) and a Replacement Metal Gate (gate-last) process flows.

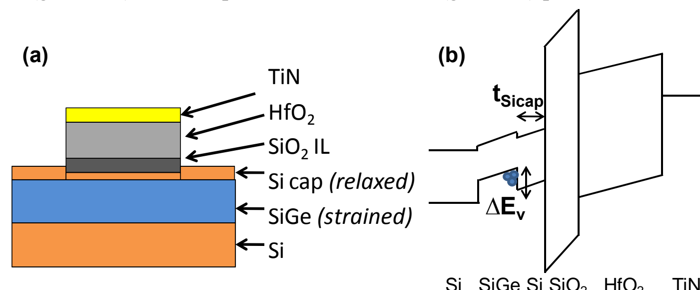
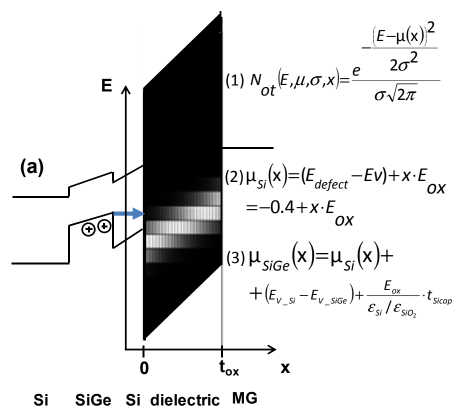


Fig. 2. (a) Gate-stack sketch of the quantum well SiGe devices studied in this work. (b) Band diagram sketch in inversion: channel holes are confined into the SiGe QW thanks to the valence band offset (ΔE_v) between the SiGe channel and the Si passivation layer.



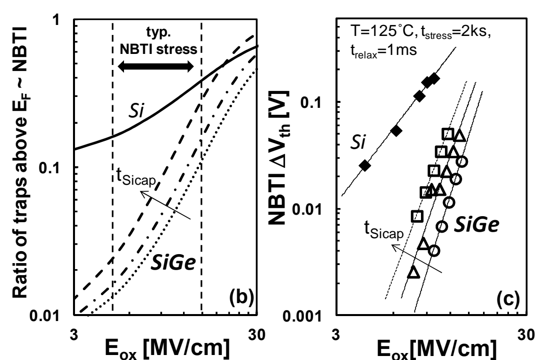


Fig. 3. (a) A model including a defect band in the dielectric centered at -0.4eV below the Si valence band as observed in [11]. The Fermi level in the channel determines which part of the defect band is energetically favorable for trapping channel holes. The defect band is modeled as a Gaussian distribution over energy (eq. 1), with its mean modulated by the E_{ox} (eq. 2), by the valence band offset between the SiGe and the Si, and by the Si cap thickness (eq. 3). (b) The ratio of accessible oxide defects can then be calculated as a function of the E_{ox} for the SiGe channel (with different Si cap) and for the Si ref. devices. *The calculation favorably compares with (c) the experimental data for SiGe devices with varying Si cap thickness.*