Abstract #2551, Honolulu PRiME 2012, © 2012 The Electrochemical Society

A Promising New n^{++}-GaN/InAlN/GaN HEMT Concept for High-Frequency Applications

V. Palankovski[1] and J. Kuzmik[1,2]

[1]AMADEA group, Inst. for Microelectronics, TU Wien, Gusshausstrasse 27-29, 1040 Vienna, Austria

[2]Inst. of Elec. Engineering, Slovak Academy of Sciences, Dubravska cesta 9, 84104 Bratislava, Slovakia

palankovski@iue.tuwien.ac.at

We study enhancement-mode n^{++}-GaN/InAlN/GaN high electron mobility transistors (EHEMTs) by means of two-dimensional numerical device simulation. An introduction of a highly-doped GaN cap layer, which is recessed under the gate, was initially proposed for an improvement of the device performance by diminishing surface traps-related parasitic effects. Our new simulation results reveal that, unlikely to planar transistor structures, the extension of the gate depletion region with drain bias is kept restricted in the presence of a n^{++}-GaN cap layer. This highly-scaled new device concept is very promising for ultra-high frequency performance.

Enhancement-mode operation of GaN-based HEMTs is very desired for various electronic applications. One way for achieving it is to reduce the barrier layer thickness, which, however, has a negative impact on the access resistance [1]. Compared to AlGaN/GaN structures, the InAlN/GaN HEMTs exhibit higher polarization charges even without strain in the barrier [2]. However, they may suffer from parasitic effects related to surface traps. A mechanism to mitigate these effects is to use a thin n^{++}-GaN cap layer, since free carriers compensate the charge variation at the GaN trapping surface, as experimentally demonstrated in [3]. The structures consist of a 2um GaN layer, 1nm AlN, 1nm $In_{0.17}Al_{0.83}N$, and 6nm GaN:Si cap, doped to $2x10^{20}cm^{-3}$. The gate length is 250nm, the source -to-drain distance is 4um, and the source-to-gate distance is 1um.

The sum of polarization charges at the AlN interfaces equals the polarization charge ($2.8x10^{13}cm^{-2}$) at the InAlN/GaN interface [4]. Thus, the AlN/InAlN barrier system is replaced by a 2 nm thick InAlN barrier in the model. We perform hydrodynamic simulations with our two-dimensional device simulator Minimos-NT, which is well-suited for numerical analysis of GaN HEMTs using an established setup of physics-based models [5]. In this work, we study the gate depletion region at different drain biases. It has been shown elsewhere that the extension of the depletion towards the drain is responsible for the delay in time required by electrons to cross the gate region [6]. The extension and corresponding delay was found to be invariant with the gate length. Consequently, the device speed may be substantially affected for gate lengths below 100nm [6].

To study the impact of the n^{++}-GaN cap layer on the possible increase of the gate depletion region with V_{DS}, we investigate the current density and the electron concentration in the EHEMT at on-state bias V_{GS}=1.5V. In the InAlN barrier, there is no current observed except for a narrow channel under the edge of the n^{++}-GaN cap at the drain side of the gate. Our simulations show that the n^{++} cap layer does not significantly contribute to the drain current both in on- and off-states. The current density contours in the barrier are restricted by the edges of the n^{++}-GaN cap layers, similarly for low V_{DS}=8V (Fig.1a) as for high V_{DS}=20V (Fig.1b). This is unlike of a planar depletion-mode InAlN/GaN HEMT (DHEMT) without n^{++}-GaN cap layer and with a 14nm barrier where the depletion region spreads significantly towards the drain contact as V_{DS} increases. Fig.1c and Fig.1d show the electron current density in the depletion mode HEMT (DHEMT) at V_{DS}=8V and V_{DS}=20V, respectively. The gate bias V_{GS}=-4V is chosen, so that the drain current is the same as in the EHEMT.

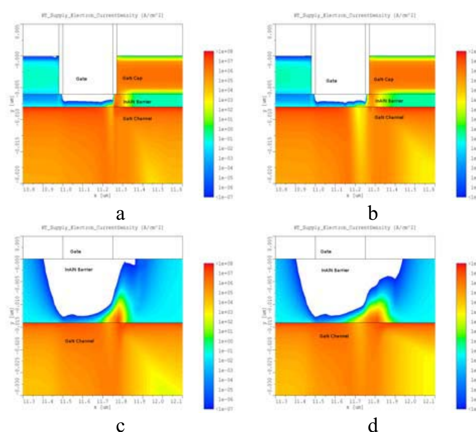

Fig.1 Electron current density [A/cm^2] in the gate regions of a n^{++}-GaN cap EHEMT (a,b) and a planar DHEMT (c,d) in on-state for V_{DS}=8V (a,c) and V_{DS} =20V (b,d).

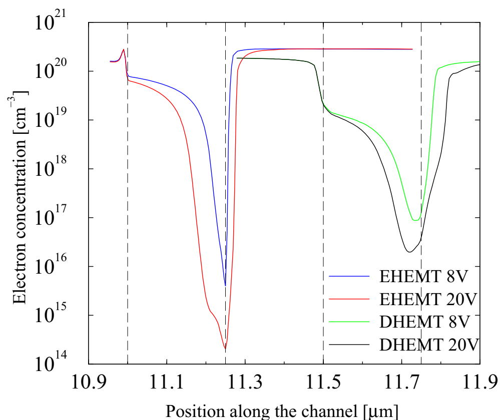

Fig.2 Comparison of electron concentration in a cut along the channels of EHEMT and DHEMT in on-state for V_{DS}=8V and V_{DS} =20V. Vertical dashed lines mark the positions of the respective gates.

Fig.2 shows cross-sections in electron concentration along the channel of both DHEMT and EHEMT structures. At V_{DS}=20V an expansion of the depletion region towards the drain by about 27nm is observed for EHEMT. This is less than a half of 62nm expansion observed for DHEMT. This reduction shows, that the combination of an n^{++}-GaN cap layer and recessed gate may be exceptionally suitable for very high-frequency devices.

Support from the Austrian Science Fund (FWF) and the Slovak R&D Agency is acknowledged.

[1] Y. Ohmaki *et al.*, *Jpn.J.Appl.Phys.* 45 (2006) L1168.
[2] J. Kuzmik *et al., IEEE Elec.Dev.Lett.* 22 (2001) 510.
[3] J. Kuzmik *et al., IEEE Tran.Elec.Dev.* 57 (2009) 2144
[4] M. Gonschorek *et al.*, *J.Appl.Phys.* 103 (2008) 093714
[5] S. Vitanov *et al.*, *IEEE Tran.Elec.Dev.* 59 (2012) 685.
[6] J.W. Chung *et al.*, *Appl.Phys.Lett.* 99 (2008) 093502.