MTJ-based Implication Logic Gates and Circuit Architecture for Large-Scale Spintronic Stateful Logic Systems

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***Abstract*— Because of the easy integration with CMOS, nonvolatility, reconfiguration capability, and fast-switching speed of magnetic tunnel junctions (MTJs), this work proposes and investigates stateful IMP-based logic gates and circuit architecture for future reconfigurable and nonvolatile computing systems. Stateful logic uses the memory unit (MTJ device) as the main computing element (logic gate) unlike the previously proposed MTJ-based logic circuits, where MTJs are only ancillary devices in logical computations. Spintronic IMP logic gates are analyzed using a SPICE model for spin-transfer torque MTJs to demonstrate the reliability of the IMP operation. The realization of the spintronic stateful logic operations extends nonvolatile electronics from memory to logical computing applications and opens the door for more complex logic functions to be realized with MTJ-based devices.**

I. Introduction

To enable stateful logic operations, the realization of a fundamental Boolean logic operation called material implication (IMP) has been demonstrated recently [1] using two equivalent TiO_2 memristive switches [2]. Stateful logic allows memory cells to serve simultaneously as logic gates and latches. This improves the conventional CMOS logic which combines logic circuits and memory elements to transfer back and forth information between them and also opens the door for a shift away from the Von Neumann architecture for innovation in computational paradigms.

By using two different circuit topologies of the magnetic tunnel junction (MTJ)-based IMP gates (Fig.1a and Fig.1b), we show the possible parallel execution of the same computational sequence in a large-scale logic system based on the spin-RAM architecture [3], which is near commercialization. The MTJ has the advantages of CMOS-compatibility, non-volatility, reconfigurable capability, and fast-switching speed [4], [5], [6] and has received great interest to overcome the significant increase in the leakage currents in CMOS circuits [7]. In addition, by utilizing the spin transfer torque (STT) effect [8] [9], the STT-MTJ gives pure electrical switching and better scalability than conventional MTJs switched by magnetic field.

Spintronic stateful logic architecture reduces the device counts and interconnection delay for which the memory elements acts also as logic gates. Using MTJ's non-volatility, spintronic stateful logic architecture is expected to reduce the static power dissipation similar to logic-in-memory [10] and non-volatile CMOS/MTJ hybrid [11] architectures. It reduces the device counts and interconnection delay by using the memory element as the main computation component (gate) as compared to the aforementioned architectures which use the MTJs as ancillary device embedded in the interconnection layer of the logic circuits.

II. Spintronic IMP Logic Gates

Material implication, 'p IMP q' or 'if p, then q', is a fundamental Boolean logic operation which in combination with FALSE (Logic 0) forms a complete logic basis to compute any Boolean function. In contrast to [1], we use MTJs as the memory elements to build spintronic IMP gates. In addition to the conventional IMP circuit topology (Fig.1a), we consider a new topology (Fig.1b) driven by a current source, which offers a more energy-efficient and reliable implementation. The MTJ contains two ferromagnetic layers separated by a thin non-conductive tunneling barrier. The magnetization of one layer (fixed layer) is pinned, while the magnetization of the second one (free layer) can be switched freely using an external magnetic field or (spin) current passing through

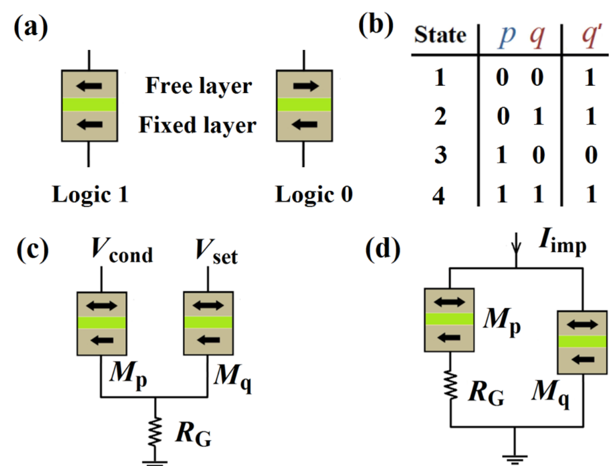

Fig. 1. (a) MTJ basic structure. (b) The IMP truth table. Conventional (c) [1] and proposed (d) IMP circuit topologies.

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the MTJ. The electrical resistance of the device depends on the relative orientation of the magnetization directions of the ferromagnetic layers. The parallel (P) magnetization state results in a low-resistance state (R_{P}; logic 1) across the barrier, while the antiparallel (AP) alignment places it in a high-resistance state (logic 0; R_{AP}). The resistance modulation is described by the tunnel magnetoresistance (TMR) ratio, defined as $(R_{\mathrm{AP}} - R_{\mathrm{P}})/R_{\mathrm{P}}$.

We analyze the IMP gates based on the SPICE model of the MTJ [12], which uses the equivalent circuit of the STT-MTJ shown in Fig.2. A curve-fitting circuit is used to model the TMR voltage(current) dependence, which is important to determine the $R-V$ characteristics of the MTJ and the voltage(current) division between the source and target MTJs in an IMP gate. The output signals of the decision circuit (V_1 and V_2) are used to determine when the device should switch states, based on the critical switching time and current (τ_0 and I_{C0}) characteristics of the device, which usually are defined corresponding to the 50% switching probability. In order to analyze the correct behavior and the reliability of the IMP gates, we use the theoretical expression of the MTJ switching probability as (1) (P_{sw}) [13], which is experimentally proved in [3].

$$P_{\mathrm{sw}} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta_0\left(1-\frac{I}{I_{\mathrm{C0}}}\right)\right]\right\} \quad (1)$$

Δ_0 is the magnetic memorizing energy without any current and magnetic field, t is the pulse width, and I is the current flowing through the MTJ. As shown in Fig.2, an error calculation circuit can be added to the SPICE model to calculate P_{sw}. Fig.3 shows how the proposed circuit can improve the SPICE model for direct calculation of P_{sw} and an IMP reliability analysis.

With the conventional topology the initial logic state of the source MTJ (M_{p}) provides a state dependent modulation (SDM) of the voltage across the target MTJ (M_{q}) through R_{G}. Due to this SDM, M_{q} switches (AP→P) in State 1, but remains unchanged in State 3. Thus, V_{cond} is chosen to leave M_{p} unchanged. With our proposed topology the initial logic state of the M_{p} provides an SDM of the current through M_{q}, which results in a correct logic behavior of M_{q} as shown in Fig.4a. Because of R_{G}, the current through M_{p} is low enough to leave it unchanged. According to the IMP truth table (Fig.1c), we define the IMP error as

$$E_{\mathrm{imp}} = (1 - P_{\mathrm{sw}}^{\mathrm{q1}}) + P_{\mathrm{sw}}^{\mathrm{p1}} + P_{\mathrm{sw}}^{\mathrm{p2}} + P_{\mathrm{sw}}^{\mathrm{q3}} \quad (2)$$

The value of the IMP gate circuit parameters can be optimized to minimize the error for fixed pulse duration and the TMR as shown in Fig.4b. Our results show that in the conventional topology, the optimal R_{G} is higher by a factor of $\times(2$ to $3)$ as compared to the new one. Therefore, the IMP energy consumption is about 60% lower than with the conventional gate topology (Fig.5a).

Robust IMP logic behavior requires a wide enough SDM window (Fig.4a). The width of the SDM window increases with the TMR ratio as shown in Fig.5b. It demonstrates that the IMP error decreases exponentially with increasing TMR ratio. At a fixed TMR the proposed topology provides a higher SDM, thus reducing the IMP error by about 60% as

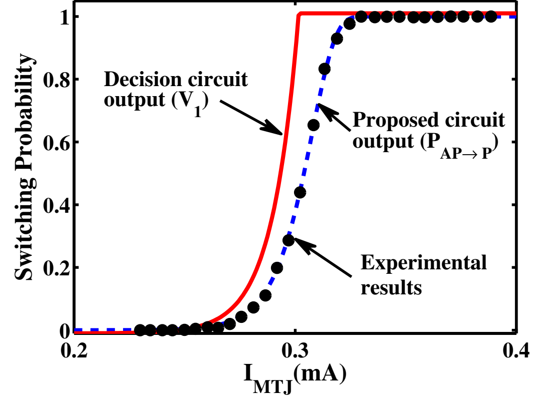

Fig. 3. Switching probability as a function of the applied current. The output of the proposed error calculation circuit reproduces the experimental data [3] as expected from the theory (1).

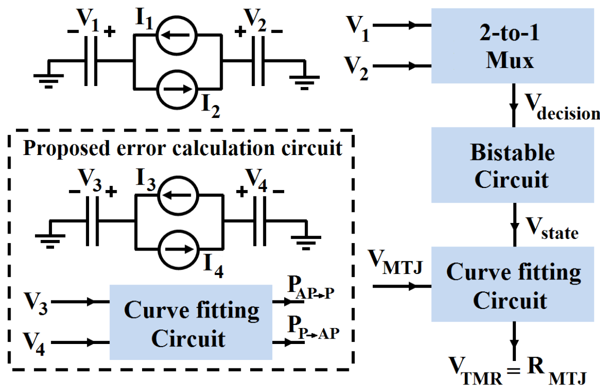

Fig. 2. The simplified equivalent circuit of the MTJ model in [12] and the proposed error calculation circuit. $I_3 = exp\left[-\Delta_0\left(1 - I/I_{\mathrm{C0(AP\to P)}}\right)\right]$ and $I_4 = exp\left[-\Delta_0\left(1 - I/I_{\mathrm{C0(P\to AP)}}\right)\right]$.

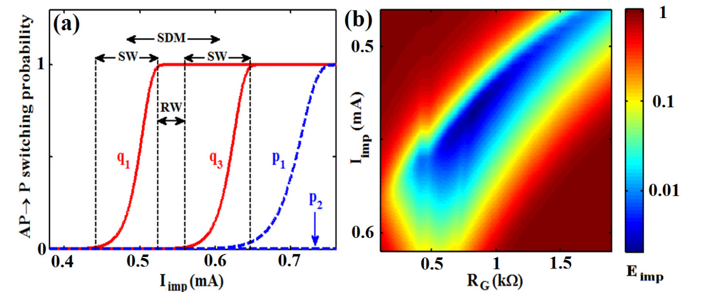

Fig. 4. Switching probabilities of M_{q} and M_{p} (a) and the total IMP error as a function of R_{G} and I_{imp} (b), plotted for a 50ns IMP execution in the new IMP circuit topology based on physical devices characterized in [3]. The SDM opens a reliable window (RW) between the switching windows (SWs) of the desired and disturbing AP→P switchings.

compared to the conventional. The record room temperature TMR of 604% [14] found in single-barrier MTJs is close to the theoretical maximum [15], [16]. This makes the MgO-based MTJs predominant candidates for STT magnetoresistive random access memories (STT-MRAMs) and promises highly reliable IMP gates.

III. Spintronic IMP Logic Circuit Architecture

In conventional MRAM architecture the MTJ is connected to the crossing points of two perpendicular arrays of parallel conducting lines. The STT switching technique brought significant advantages and eliminates the difference between reading and writing in spin-RAM architecture [3]. A typical memory cell of the spin-RAM, which consist of an access transistor and an MTJ as its storage element (the 1T/1MTJ structure) is shown in Fig.6. Stateful IMP logic architecture offers the eliminate the need of using extra charge-based logic gates, while uses the memory cells simultaneously as logic gates and latches via IMP operation. Fig.7 shows a block IMP logic circuit architecture based on the 1T/1MTJ structure, which can realize the spintronic IMP gate shown in Fig.1d.

The IMP operation between two memory cells $C_{i,j}$ and $C_{i,j'}$ ($q_{i,j} \leftarrow p_{i,j'}$ IMP $q_{i,j}$) can be performed by simultaneous selection of the i-th word-lines (WLs) and the j-th and the j' source-line (SL) selectors which connect the SLs to ground directly and via R_G, respectively, and applying the current source I_{imp} to the j-th and j'-th bit-lines (BLs). Then the result of the IMP operation will be written in $C_{i,j}$.

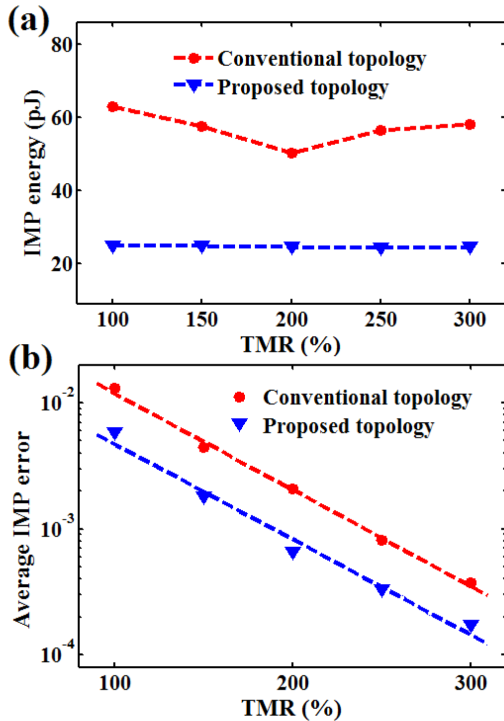

Fig. 5. The IMP energy consumption (a) and the average error (b) depends on the TMR ratio for both conventional and proposed topologies.

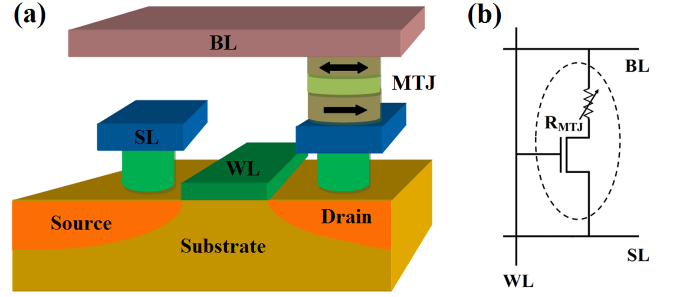

Fig. 6. 1T/1MTJ structure. Structural (a) and the equivalent circuit (b) diagrams [18].

As compared to the spin-RAM we have added two *work cells* to any WL, while it has been shown that with two additional memristors all Boolean functions on any number of memory cells can be performed [17]. These work cells can also be used to connect different WLs. In fact, in order to perform the IMP between memory cells from different WLs, one can copy the logic data stored in one memory cell to a work cell from the other WL.

It should be noted that the nonzero ON resistance of the access transistors (R_{on}) decreases the effective TMR of the 1T/1MTJ cells which can be defined as

$$TMR_{\text{eff}} = \frac{R_{AP} - R_P}{R_P + R_{on}} \tag{3}$$

Therefore, a robust IMP operation needs MTJs with sufficiently high TMR and electrical resistance. Our simulations show that the TMR of a 1T/1MTJ including the MTJ devices characterized in [3] and an access device with a width about 1-2μm at the 180-nm technology decreases about 10%-30%. Therefore, according to Fig.5, a 99.9% IMP correct logic behavior requires a TMR ratio higher than 250%.

IV. Stateful Spintronic Full Adder

We consider a full adder which is a basic element of arithmetic circuits. As is well known, it adds three binary inputs (c_1-c_3) and produces two binary outputs, sum (S = c_1 XOR c_2 XOR c_3) and carry (C =[c_1 AND c_2] OR [c_3 AND {c_1 XOR c_3}]). Since IMP cannot fan out, two operations, FALSE ($c_j \leftarrow 0$) and IMP ($c_j \leftarrow c_i$ IMP 0), should be executed in subsequent steps to write $\overline{c_i}$ in an additional cell $\overline{c_j}$ ($j = 4-6$), in order to ensure that the logical value $\overline{c_i}$ (therefore c_i) is still available, when it is needed as an input for subsequent IMP operations. As 'p IMP 0' and 'p IMP q' are equivalent to 'NOT p' and '(NOT p) OR q', respectively, some operations can be eliminated to minimize the total effort. Our design involves only 27 subsequent FALSE and IMP operations on 3 input cells (c_1-c_3) and 3 additional cells (c_4-c_6), in contrast to the earlier proposed IMP-based scheme [19] with 19 and 18 operations (37 total) for generating S and C, respectively, and 4 additional cells. Therefore, our design requires less operations (delay) and devices (area).

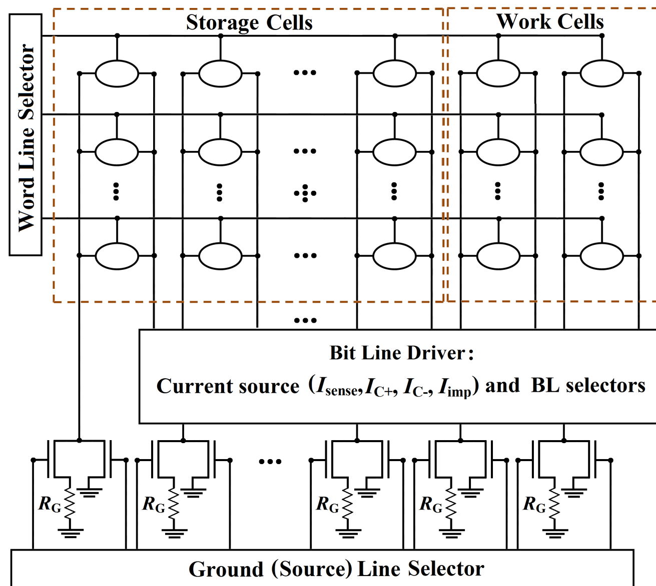

Fig. 7. A simplified spintronic IMP logic circuit architecture based on the spin-RAM architecture to realize the MTJ-based IMP gate with the proposed topology shown in Fig.1d. Controlling and programming the line drivers and selectors requires an external processor similar to the proposed circuit for the TiO_2-based architecture [1].

The logic-in-memory circuit presented in [10] uses 34 transistors and 4 MTJs for implementing a full-adder, while stateful architecture eliminates the need of using extra charge-based logic gates and offers superior logic density.

V. Conclusion

We have described MTJ-based IMP gates as basic elements to combine memory and logic computing in a stateful logic circuit based on existing spin-RAM architectures. This opens an alternative path towards reconfigurable and nonvolatile MTJ-based computing devices and systems [20]. The robustness of the IMP operation is based upon a state dependent modulation (SDM) of the voltage(current) division between the source and target MTJs. It has been demonstrated that the reliability increases exponentially with increasing TMR ratio.

Due to non-volatility and eliminating extra charge-based logic gates, the stateful IMP logic is expected to exhibit low power consumption, high logic density, and high speed operation simultaneously.

Acknowledgment

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