Spintronic stateful logic gates using magnetic tunnel junctions written by spin-transfer torque

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The realization of a logic operation named material implication (IMP) has been reported recently to enable stateful logic operations using TiO_2 memristive switches [1]. IMP is a fundamental Boolean logic operation on two variables *p* and *q* (‘*p* IMP *q*’ or ‘if *p*, then *q*’), which in combination with FALSE (Logic 0) forms a complete logic basis to compute any Boolean function.

In this work we present a novel nonvolatile logic which is based on the implementation of the IMP operation with magnetic tunnel junctions (MTJ). The circuit topology shown in Fig.1a includes a conventional resistor and two MTJs driven by a current source. Spintronic stateful logic operations enable extending nonvolatile electronics from memory to logical computing applications, for which the STT-MTJ cells serve simultaneously as logic gates and latches. The MTJs are written by spin-transfer torque (STT) and show memristive behavior [2].

The reliability of the TiO_2 memristive IMP gates is based on a high resistance switching ratio of the TiO_2 switches (about 10^3), which provides state changes that depend on the existing logic states of the memristors, which enable the circuit to function as a stateful IMP gate. Although the theoretical maximum resistance switching ratio of the MTJs is about two orders of magnitude lower than that of the TiO_2 memristors', the realization of the spintronic IMP gate relies on a threshold current density required for STT switching and a positive feedback on the electrical resistance of the target MTJ (Q). Fig.1b shows the square of the total error of the of the spintronic IMP gate as a function of R_G, based on a spice macromodel of the STT-MTJs [3]. The minimum error is about 1.5%, which is lower than the minimum predicted for TiO_2 memristors [4].

The generalization of the spintronic IMP gate to a nonvolatile logic-in-memory system can be performed by using a conventional 1T/1MTJ structure [5]. By adding a current source (I_{imp}), a bit line (BL) selector (to make possible to apply I_{imp} to two BLs simultaneously), and a source line (SL) selector (to make it possible to select the SL of the source MTJ cell (M_p) to the ground through R_G), to the spin-RAM architecture, a MTJ-based nonvolatile stateful architecture can be achieved. As an example, we consider a stateful full adder as a basic element of the arithmetic circuits. It adds three binary inputs (c_1- c_3) and produces two binary output, sum (S = c_1 XOR c_2 XOR c_3) and carry (C = (c_1 AND c_2) OR (c_3 AND (c_1 XOR c_3))). Since IMP cannot fan out, the operations FALSE ($c_j \leftarrow 0$) and IMP ($c_j \leftarrow c_i$ IMP 0) should be executed in subsequent steps to write $\hat{c}_i$ (NOT c_i) in an additional cell c_j (j=4-6), to ensure that the logical value $\hat{c}_i$ (therefore c_i) is still available, when it is needed as an input for subsequent IMP operations. As ‘*p* IMP 0’ and ‘*p* IMP *q*’ are equivalent to ‘NOT *p*’ and ‘(NOT *p*) OR *q*’, respectively, some operations can be eliminated to minimize the total effort. Our design involves only 27 subsequent FALSE and IMP operations on 3 input cells (c_1-c_3) and 3 additional cells (c_4-c_6), in contrast to the earlier proposed scheme [6] with 19 and 18 operations (37 total) for generating S and C, respectively, and 4 additional cells. Therefore, our design requires less operations (delay) and devices (area).

The MOS/MTJ-hybrid logic circuit presented in [7] uses 34 transistors and 4 MTJs for implementing a full-adder, while our proposed spintronic stateful logic architecture eliminates the need of using extra charge-based logic gates and opens an alternative path towards MTJ-based nonvolatile logic-in-memory circuits.

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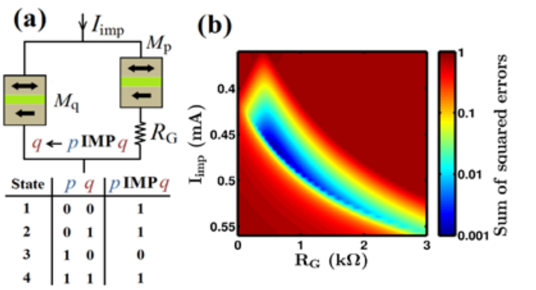

Figure 1: *(a) The IMP circuit and its truth table (b) The total error of the IMP operation as a function of R_G and I_{imp} for a pulse duration of 100ns.*

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