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◉ **Oral Presentations - Browse by Symposium and Presentation Day**

Y: Reliability and Variability of Devices for Circuits and Systems [RV-DCS]

Wednesday - 3 July, 2013

○ **Poster Presentations - Browse by Symposium**

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Wednesday - 3 July, 2013 | Symposium Y

Oral Presentations

Session Y5: Interconnect/Gate Stack
Wednesday, July 03, 2013 | 10:30 - 12:30 | Room 327
Chairs: Cher Ming Tan

Y5-1 *30 min*
ICMAT13-A-0421 Invited
About Voids in Copper Interconnects
Roberto L. DE ORIO[1], Siegfried SELBERHERR[1#+]
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Voiding in modern copper interconnects caused by electromigration (EM) is one of the main reliability concerns in microelectronics. Voids cause a reduction of the metal cross sectional area which, in turn, leads to an increase of the resistance of the interconnect line. If a void is sufficiently large and/or located at a critical site of the line, such as under a via at the cathode end of the line, the resistance increases above a maximum tolerable value characterizing the failure.

Voiding in interconnect lines encompasses two phases of development, namely void nucleation and void growth. Atomic transport due to EM is accompanied by creation of mechanical stress. A sufficiently large tensile stress build-up at a flaw or site of weak adhesion between the copper/capping layer interface at the cathode end of the line triggers void nucleation. In the second phase, the void grows by capturing vacancies driven by EM. Two main types of fatal voids have been identified in EM experiments: large trench voids which are typically observed for late failures and small slit-like voids which are normally observed for early failures. Nevertheless, before the interconnect failure is finally triggered, void development can undergo several processes like void migration and shape changes depending on the local properties of the line.

Understanding the mechanisms of void formation and evolution in interconnects is, therefore, crucial to characterize and predict an EM-induced failure. In this presentation, we discuss modeling and simulation of the void nucleation and the void evolution phase. The emphasis is put on presenting comprehensive physically-based models and discussing suitable numerical methods for the fully three-dimensional simulation of typical copper dual-damascene interconnect structures.

Y5-2 *30 min*
ICMAT13-A-3451 Invited
Design for Reliability for Advanced Nanoelectronic Gate Stack
Kin Leong PEY[1#+]
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State-of-the-art metal gate/high-k gate stacks are facing numerous reliability challenges. In particular, dielectric degradation and breakdown during device operation remain key concerns. In this talk, the challenge of start-of-the-art nano-metal/high-k gate dielectric stacks is reviewed. Various key parameters such as device material and architecture affecting the gate dielectric degradation and breakdown are identified. A new concept called Design for Reliability for extending the lifetime and reliability is proposed. Specific examples using physical analysis techniques like TEM and STM on providing direct evidence of the ultrathin dielectric degradation and breakdown mechanism and physics for understanding and formulating of the Design for Reliability will be presented.

Y5-3 *15 min*
ICMAT13-A-3614 Contributed
Effects of Fe Addition on the Sn-Ag-Cu Solder – Cu Joint Properties
Yiteng LIN[1+], Ramaswami GOPALA KRISHNAN[1#], Hui Ru TAN[2], Minqin REN[1], Eng Soon TOK[1], Yaadhav RAAJ[3]