

# Reduction of the BTI Time-Dependent Variability in Nanoscaled MOSFETs by Body Bias

J. Franco, B. Kaczer, M. Toledano-Luque, Ph. J. Roussel, G. Groeseneken<sup>1</sup>

imec

Leuven, Belgium

Phone: +32 16 28 10 85, e-mail: [Jacopo.Franco@imec.be](mailto:Jacopo.Franco@imec.be)

<sup>1</sup>also with ESAT, KU Leuven, Belgium

B. Schwarz, M. Bina, M. Waltl, P.-J. Wagner, T. Grasser

Institute for Microelectronics, T.U. Wien  
Wien, Austria

**Abstract**—We study the impact of individual charged gate oxide defects on the characteristics of nanoscaled pMOSFETs for varying body biases. Both a reduced time-zero variability and a reduced time-dependent variability are observed when a forward body bias is applied. In order to explain these observations, a model based on the modulation of the number of unscreened dopant atoms within the channel depletion region is proposed.

**Keywords**—Body Bias, Nanoscale, Negative Bias Temperature Instability, pMOSFETs, Variability.

## I. INTRODUCTION

With the aggressive scaling of CMOS device size, the number of dopant atoms and the number of defects in each device reduces to numerable levels [1]. This trend has significant technological implications: it results in increased *time-zero* (i.e., as-fabricated) variability, but also considerable *time-dependent* variability (i.e., reduced reliability) [2,3]. Several groups have recently shown that the properties of individual charged gate oxide defects (e.g. capture and emission times) can be directly observed and measured in deeply scaled MOSFETs [4-7]. We have recently studied the impact of individual defects on the  $I_D-V_G$  characteristics of nanoscaled pMOSFETs and found that each defect causes a  $V_G$ -dependent threshold voltage shift ( $\Delta V_{th}$ ) [8]. In particular we observed that the detrimental impact of defects causing a relevant shift of the device characteristic close to  $V_{th}$  is reduced at higher  $V_G$ 's of relevance for device operation [8,9].

In this work we show that the body bias also modulates the impact of individual charged defects on the device characteristics. A reduced time-zero  $V_{th}$ -variability and reduced single-defect-induced  $\Delta V_{th}$ 's are observed when applying a forward body bias. We ascribe these observations to a reduced sensitivity to current percolation paths and we propose a model based on the modulation of unscreened dopant atoms within the channel depletion region which quantitatively explains the reduced impact of individual charged defects.

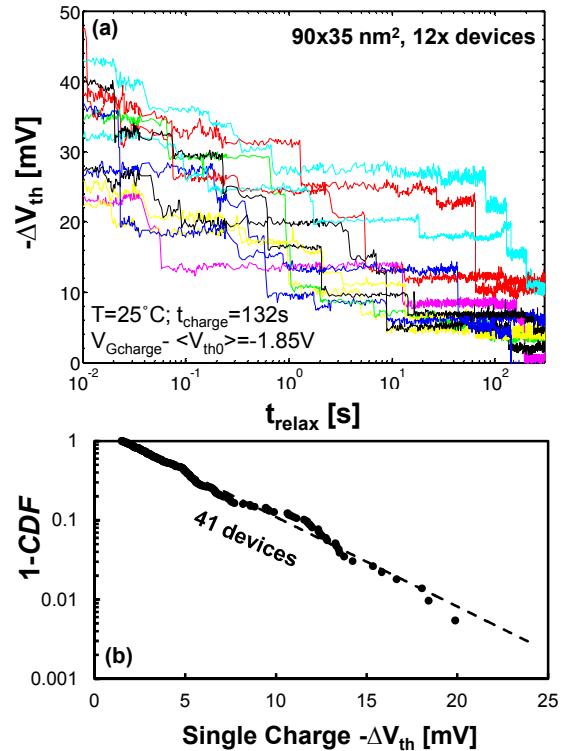


Figure 1. (a) NBTI-like relaxation transients recorded on nanoscaled ( $\sim 90 \times 35 \text{ nm}^2$ ) Si pMOSFETs. The total  $\Delta V_{th}$  strongly varies from device to device [3]. Individual gate oxide defect discharge events are visible, with varying  $\Delta V_{th}$  step heights. (b) The  $\Delta V_{th}$  step heights appear exponentially distributed, with the average step height  $\eta$  depending on the device dimensions [8], oxide thickness and doping level [10], see Eq. (2).

## II. EXPERIMENTAL

We performed Negative Bias Temperature Instability (NBTI) like experiments at room temperature on nanoscaled ( $\sim 90 \times 35 \text{ nm}^2$ ) Si/SiON/poly-Si ( $\text{CET} \approx 2 \text{ nm}$ ) pFETs: after a defect charging phase, relaxation transients were recorded [Fig. 1 (a)].

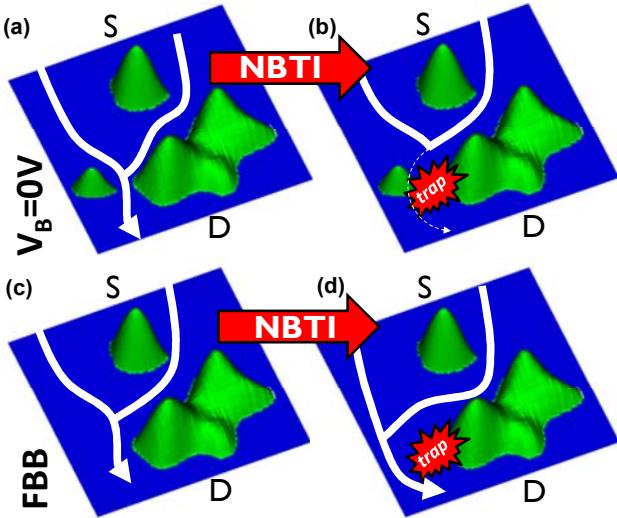


Figure 2. (a) RDD causes a non-uniform potential profile in the channel.

The carrier conduction hence proceeds through percolation paths (sketches generated via [11]). (b) In the unlucky case of a charged gate oxide defect located above the constriction point, the percolation path will be blocked off, causing a strong reduction in the current (i.e., a large  $\Delta V_{th}$  step, see Fig. 1). (c) For a reduced  $X_{dep}$  obtained by applying a FBB, fewer unscreened dopant atoms might be included in the depletion layer (d) reducing the sensitivity to the current percolation effect.

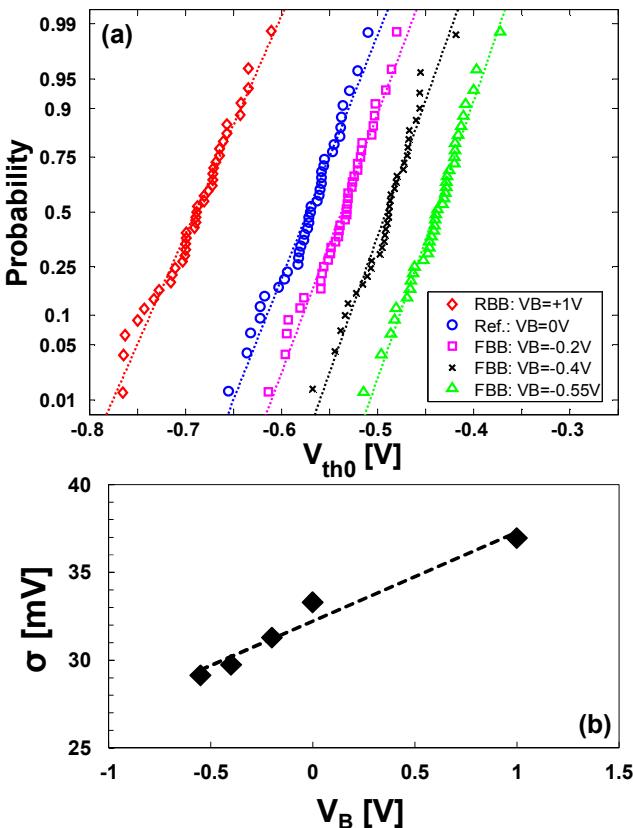


Figure 3. (a) Probability plot of the initial  $V_{th0}$ 's of a set of nanoscaled devices for different  $V_B$ 's, following normal distributions. The BB modulates both the average  $V_{th0}$  and (b) its variability, with a FBB reducing the standard deviation of the normal distribution.

The total  $\Delta V_{th}$  observed after the same NBTI stress strongly varies from device to device [3]. Individual gate oxide defect discharge events are visible in the relaxation traces, and the associated  $\Delta V_{th}$  step heights appear approximately exponentially distributed [Fig. 1 (b)] with CDF:

$$F(\Delta V_{th}, \eta) = 1 - \exp\left(-\frac{\Delta V_{th}}{\eta}\right), \quad (1)$$

where  $\eta$  is the average  $\Delta V_{th}$  step height. Note individual charged defects causing remarkable  $\Delta V_{th}$  up to  $\sim 20$ mV when charged. Such anomalous single-defect-induced  $\Delta V_{th}$ 's are ascribed to the percolative nature of the current flow in the channel yielded by the non-uniform potential profile resulting from Random Dopant Distribution (RDD) [1] in nanoscaled FETs [see Fig. 2 (a)]. A charged gate oxide defect located on top of a critical spot (i.e., the point of maximum confinement) might block off the percolation path and cause a significant current reduction [Fig. 2 (b)], observed as a large threshold voltage shift. The average  $\Delta V_{th}$  step height  $\eta$ , i.e., the average impact of a single charged defect on the FET behavior, is expected to scale inversely with the device channel area [8], and proportionally with the gate oxide thickness  $t_{ox}$  and the square root of the dopant concentration in the channel  $N_D$  [10]:

$$\eta \propto \frac{t_{ox} \sqrt{N_D}}{WL}. \quad (2)$$

The body bias (BB) technique is commonly used to modulate the channel depletion layer thickness ( $X_{dep}$ ) and therefore the  $V_{th0}$  of the MOSFET devices. A reverse body bias (RBB) increases  $X_{dep}$  and  $|V_{th0}|$  and can be exploited for low leakage applications, while a forward body bias (FBB) reduces  $X_{dep}$  and  $|V_{th0}|$ , which can be favorable for high performance applications, at the cost of increased junction leakage [12]. We found that the BB has also a significant impact on both the time-zero and the time-dependent variability of scaled devices, as discussed next.

### III. RESULTS

Measurements of the initial  $V_{th0}$ 's of a device sample set revealed normal distributions and showed that the applied BB not only modulates the average threshold voltage value but also the  $V_{th0}$ -variability, with a FBB reducing the standard deviation of the  $V_{th0}$  distribution (Fig. 3). This observation suggests that reducing the  $X_{dep}$  by means of BB might yield the same beneficial effect on the time-zero variability as reducing the channel doping level  $N_D$ . It is of interest hence to investigate the effect of BB on the time-dependent variability, specifically evaluating the impact of individual charged oxide defects on the device  $V_{th}$  for different  $V_B$ 's. Fig. 4 (a) gives NBTI relaxation traces recorded for different BB on one device manifesting a single dominant oxide trap ( $\Delta V_{th} \approx 25$ mV) [8]: the BB modulates the  $\Delta V_{th}$  step height associated with the trap charging/discharging, with a lower step height for the FBB cases and a higher step height for the RBB case. The same observation was consistently repeated on several devices manifesting such dominant gate oxide defects [Fig. 4 (b)].

Furthermore, the same trend was clearly confirmed by looking at the *entire distributions* of the single charge step heights observed on multiple devices (Fig. 5), with a reduced average  $\Delta V_{th}$  step height  $\eta$  for the FBB cases. The extraction of  $\eta$  for different BB was repeated on two different wafers (both having a Si/SiON/poly-Si gate stack but with slightly different oxide thickness) and for two different charging conditions [Fig. 6 (a)]. When normalizing the extracted  $\eta$  values to the respective  $V_B = 0V$  cases, a universal trend is found [Fig. 4 (b)], with a measured reduction in  $\eta$  down by -25% for a FBB as low as  $V_B = -0.6V$ .

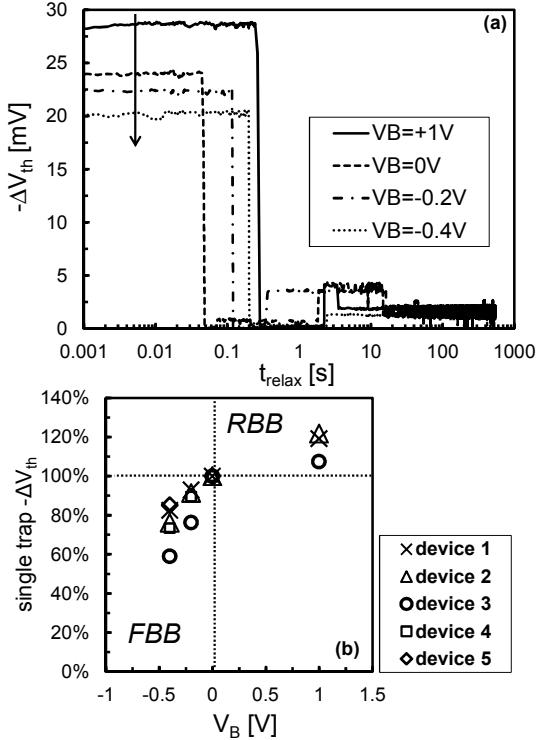


Figure 4. (a) NBTI relaxation traces recorded for different BB on one selected device showing a single dominant oxide trap ( $\Delta V_{th} \approx 25\text{mV}$ ): the BB modulates the  $\Delta V_{th}$  step height, with a FBB reducing it. (b) The same observation is consistently repeated on several such devices showing single dominant oxide traps. Previous works suggested that also the defect capture and emission times can be dependent on the BB [13]

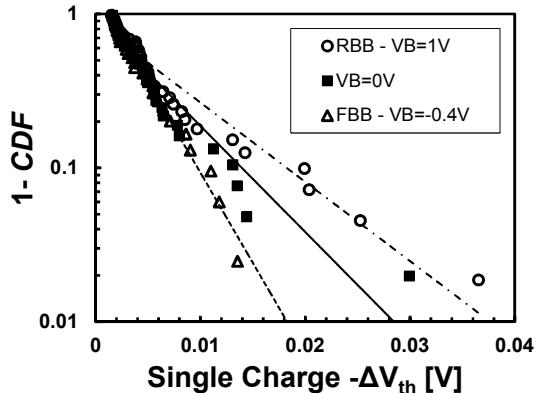


Figure 5. Exponential distributions of the single charge  $\Delta V_{th}$  step heights obtained on the same sample set for different applied  $V_B$ 's. Note the increased variance (larger  $\eta$ ) for the RBB case and the reduced variance (smaller  $\eta$ ) for the FBB case.

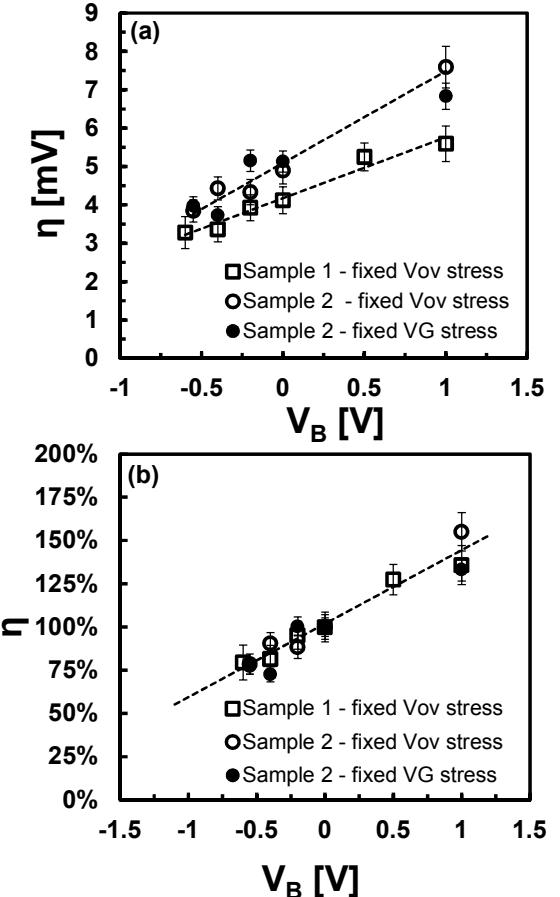


Figure 6. (a)  $\eta$  values extracted with a Maximum Likelihood fit from the distributions measured for varying BB (see Fig. 5) on two wafers with identical Si/SiON/Poly-Si gate stack and identical doping levels, but slightly different oxide thicknesses (CET 1.8~2.1nm). On Sample 2, the NBTI-like defect charging phase was performed at two different gate biases: at fixed gate overdrive stress voltage (i.e. constant inversion hole population but lower oxide electric field  $E_{ox}$  for the FBB, [14]), and at fixed gate stress voltage (i.e. same  $E_{ox}$  but varying hole population for different BB, [14]). In every case the FBB was found to reduce  $\eta$  while the RBB increased it. (b) When normalizing the  $\eta$  values to the respective  $V_B = 0V$  standard cases, a universal trend is found.

#### IV. DISCUSSION

We interpret these experimental observations as related to the BB modulation of  $X_{dep}$ . For a reduced  $X_{dep}$  (FBB), a reduced number of unscreened dopant atoms is included in the depletion layer [Fig. 2 (c), cf. (a)], reducing the sensitivity to current percolation paths [Fig. 2 (d), cf. (b)], while for a wider  $X_{dep}$  more dopant atoms can contribute to the non-uniformity of the potential profile in the channel. In other words, *reducing the  $X_{dep}$  by means of BB alleviates the RDD effects and improves the time-zero and the time-dependent variability as effectively as reducing the channel doping level*. To support this hypothesis, we calculated the average number of dopant atoms ( $n_D$ ) located within the channel depletion width as a function of the BB as:

$$n_D = WL N_D X_{dep}, \quad (3)$$

where  $W$  and  $L$  are the device width and length respectively, and  $N_D$  is the channel doping level.

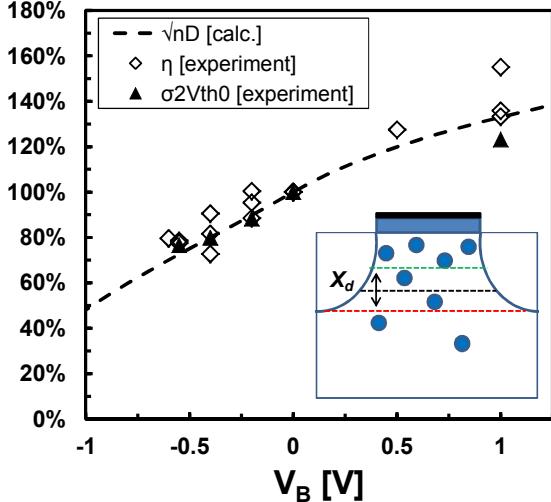


Figure 7. (Inset) The body bias modulates the channel depletion width [ $X_{dep}$ , see Eq. (4)] and therefore the average number of unscreened dopant atoms within the depletion layer [ $n_D$ , see Eq. (3)]. The average  $\Delta V_{th}$  step height ( $\eta$ ) and the variance of the  $V_{th0}$  distribution ( $\sigma^2_{V_{th0}}$ ) are expected to scale proportionally with the square root of the channel doping concentration (see Eq. (2), [10,16]). The measured modulations of  $\eta$  and  $\sigma^2_{V_{th0}}$  by BB (symbols) are excellently correlated to the calculated square root of  $n_D$  (dashed line) over the whole considered  $V_B$  range. This observation suggests BB as a flexible electrical equivalent to doping level adjustment.

The channel depletion layer thickness  $X_{dep}$  was calculated as a function of  $V_B$  according to textbook equations [15] as:

$$X_{dep} = \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{qN_D}(\phi_s + V_B)}, \quad (4)$$

$$\phi_s = V_T \ln\left(\frac{N_D}{n_i}\right), \quad (5)$$

where  $V_T$  is the thermal voltage ( $k_B T/q$ ,  $\sim 26$ mV at room temperature), and  $n_i$  the intrinsic carrier concentration ( $\sim 1.4 \times 10^{10} \text{ cm}^{-3}$ ).

Fig. 7 shows the calculated square root of  $n_D$  as a function of  $V_B$  vs. the experimental measurements of  $\eta$  as of Fig. 6 (b) and of the variance of the  $V_{th0}$  distribution ( $\sigma^2_{V_{th0}}$ ) as of Fig. 3 (note: the  $V_{th0}$ -variance is expected to follow the same technological dependences of  $\eta$  [16], cf. Eq. 2). An excellent match is found over the whole considered range of  $V_B$ 's, confirming that the improved time-zero and time-dependent variability obtained by applying a FBB are yielded by the reduced number of unscreened dopant atoms within the channel depletion region. Furthermore, 3D atomistic device simulations [17] confirm that the tail of the  $\Delta V_{th}$  step height distribution is expected to be affected by BB. These findings suggest that, from the perspective of device variability, the BB technique can be seen as a convenient and flexible electrical equivalent to doping adjustment.

The time-dependent variability in nanoscaled devices leads to a shift in our perception of reliability: deterministic lifetimes measured on large area devices have to be replaced by lifetime distributions [3]: i.e., although the average reliability of a given

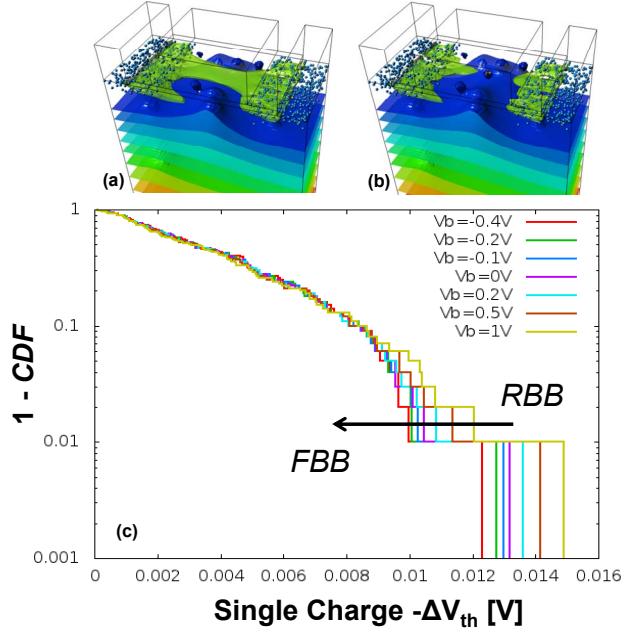


Figure 8. (a) 3D atomistic device simulation [17] showing a current percolation path in the channel due to potential non-uniformity caused by RDD; (b) The percolation path can be effectively switched off by a charged oxide defect located close to its confinement point. (c)  $\Delta V_{th}$  step height distributions obtained by multiple 3D atomistic device simulations. The body bias is confirmed to modulate the distribution, with a FBB yielding a reduction of its tail and therefore a reduced time-dependent variability.

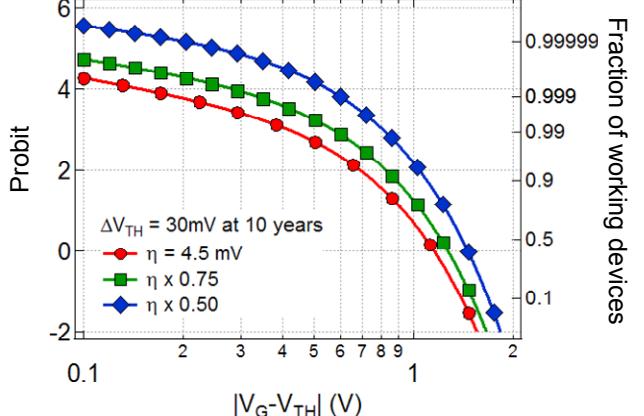


Figure 9. Fraction of working devices after 10 year of continuous operation at varying gate overdrive voltages (considered failure criterion:  $\Delta V_{th}=30$ mV), calculated according to [18] for different  $\eta$  values. The reduction in  $\eta$  offered by the FBB technique projects to a significant improvement of the lifetime distribution of realistic device population.

technology might be sufficient, a fraction of a realistic device population (typically consisting of billions of devices) can still fail. It has been found that the average step height  $\eta$  is the key parameter controlling the lifetime distribution, while the average oxide defect density is of lesser relevance [18]. In this respect, the reduction in  $\eta$  offered by the FBB technique projects to a significant improvement of the lifetime distribution of realistic device populations (i.e. billions), as shown in Fig. 9.

Finally we note that the body bias experiments highlight the existence of a correlation between the time-zero variability (spread in  $V_{th0}$ ) and the BTI-induced time-dependent variability (spread in  $\Delta V_{th}$ ). As previously shown by our group in [19], the distribution of the total  $\Delta V_{th}$  induced by NBTI in nanoscaled devices can be analytically described by a convolution of the Poisson distribution describing the number of charging traps present in each device with the exponential distribution describing the impact per each charged trap (see Fig. 1b). As shown there, the variance of the total  $\Delta V_{th}$  distribution is controlled by the parameter  $\eta$  (cf. Eq. 1-2) and increases with the stress time (i.e. the device use), or equivalently with the average induced  $\langle \Delta V_{th} \rangle$  as:

$$\sigma_{\Delta V_{th}}^2 = 2\eta \langle \Delta V_{th} \rangle. \quad (6)$$

Fig. 10 shows the standard deviation of the  $V_{th0}$  distribution measured for varying body biases as from Fig. 3, vs. the standard deviation of the BTI induced  $\Delta V_{th}$  calculated by using Eq. 6 with the experimentally extracted  $\eta$  values as of Fig. 6, for an average induced  $\langle \Delta V_{th} \rangle = 50\text{mV}$  (i.e. a typically considered device failure criterion). A correlation between the time-zero and time-dependent variability is apparent. Although the  $V_{th0}$  spread is larger than the  $\Delta V_{th}$  spread (for the considered  $\langle \Delta V_{th} \rangle = 50\text{mV}$ ,  $\sigma_{\Delta V_{th}} / \sigma_{V_{th0}} = 0.7$ ), the relative importance of the time-dependent variability is expected to increase during the device lifetime (cf. Eq. 6). Moreover, the additional circuit design margin necessary to cope with the additional variability induced by BTI might become unsustainable when combined with the margin accounting for the significant time-zero variability in nanoscaled devices. In this scenario, the combined beneficial effects of a Forward Body Bias will become crucial.

## V. CONCLUSIONS

The impact of individual charged gate oxide defects on nanoscaled pMOSFETs was studied as a function of the body bias. Modulations of both the time-zero variability and the time-dependent variability were found. These observations were explained by the modulation of the number of unscreened dopant atoms within the channel depletion region induced by the body bias. A forward body bias significantly reduces the average impact of individual gate oxide defects, and therefore constitutes a flexible electrical technique to improve the time-zero and the time-dependent variability in nanoscaled MOSFET devices without involving any technological tuning.

## ACKNOWLEDGMENT

This work was performed as part of imec's Core Partner Program. It has been in part supported by the European Commission under the 7<sup>th</sup> Framework Programme (Collaborative project MORDRED, contract No. 261868). Discussions with Dr. H. Reisinger are gratefully acknowledged.

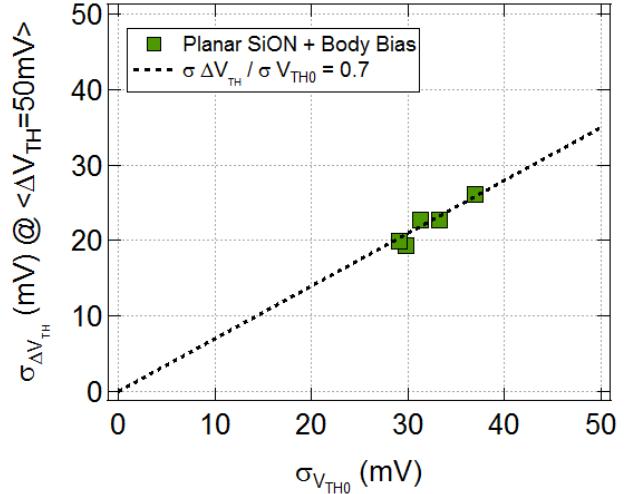


Figure 10. Spread of the initial threshold voltage distribution ( $\sigma_{V_{th0}}$ ) plotted versus the spread of the total  $\Delta V_{th}$  distribution ( $\sigma_{\Delta V_{th}}$ ) after NBTI for different body biases.

## REFERENCES

- [1] A. Asenov, R. Balasubramanian, A. R. Brown, and J. H. Davies, "RTS Amplitude in Decanometer MOSFETs: 3-D Simulation Study", in *IEEE Trans. Electron Devices*, Vol. 50, no. 3, 2003, pp. 839-845;
- [2] V. Huard *et al.*, "NBTI Degradation: from Transistor to SRAM Arrays", in *Proc. IEEE International Reliability Physics Symposium*, 2008, pp. 289-300;
- [3] B. Kaczer *et al.*, "Origin of NBTI Variability in Deeply Scaled pFETs", in *Proc. IEEE International Reliability Physics Symposium*, 2010, pp. 26-32;
- [4] M. Toledano-Luque *et al.*, "Response of a Single Trap to AC Negative Bias Temperature Stress", in *Proc. IEEE International Reliability Physics Symposium*, 2011, pp. 364-371;
- [5] V. Huard, F. Cacho, Y. Mamay Randriamihaja, A. Bravaix, "From Defects Creation to Circuit Reliability", in *Microelectronic Engineering*, Vol. 88, no. 7, 2011, pp. 1396-1407;
- [6] T. Grasser *et al.*, "Recent Advances in Understanding the Bias Temperature Instability", in *Proc. IEEE International Electron Device Meeting*, 2010, pp. 82-85;
- [7] C. Liu *et al.*, "New Observations on AC NBTI induced Dynamic Variability in Scaled High- $\kappa$  / Metal-gate MOSFETs: Characterization, Origin of Frequency Dependence, and Impacts on Circuits", in *Proc. IEEE International Electron Device Meeting*, 2012, pp. 466-469;
- [8] J. Franco *et al.*, "Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs", in *Proc. IEEE International Reliability Physics Symposium*, 2012, pp. 5A.4.1-6;
- [9] B. Kaczer *et al.*, "The Relevance of Deeply-Scaled FETs Threshold Voltage Shift for Operation Lifetime", in *Proc. IEEE International Reliability Physics Symposium*, 2012, pp. 5A.2.1-6 ;
- [10] A. Ghetti, C.M. Compagnoni, A.S. Spinelli, A. Visconti, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca-Nanometer Flash Memories", in *IEEE Trans. Electron Devices*, Vol. 56, no. 8, 2009, pp. 1746-1752;
- [11] <http://www.ibiblio.org/e-notes/Perc/contour.htm>;
- [12] A. Hokazono *et al.*, "Forward Body Biasing as a Bulk-Si CMOS Technology Scaling Strategy", in *IEEE Trans. Electron Devices*, Vol. 55, no. 10, 2008, pp. 2657-2664;
- [13] N.B. Lukyanchikova, M.V. Petrichuk, N.P. Garbar, E. Simoen, C. Claeys, "Influence of the substrate voltage on the random telegraph signal parameters in submicron n-channel metal-oxide-semiconductor field-effect transistors under a constant inversion charge density", *Appl. Phys. A*, Vol. 70, 2000, pp. 345-353;

- [14] Y. Mitani, H. Satake, and A. Toriumi, “Influence of Nitrogen on Negative Bias Temperature Instability in Ultrathin SiON”, in *IEEE Trans. Device and Material Reliability*, Vol. 8, No. 1, pp. 6-13, 2008;
- [15] N. Arora, “MOSFET Modeling for VLSI Simulation—Theory and Practice”, World Scientific Publishing Co. Pte. Ltd., ISBN 978-981-256-862-5, 1992;
- [16] K.J. Kuhn *et al.*, “Process Technology Variation”, in *IEEE Trans. Electron Devices*, Vol. 58, no. 8, 2011, pp. 2197-2208;
- [17] B. Schwarz *et al.*, “Electrostatic Properties of Single and Multiple Charged Oxide Traps in the Presence of Random Discrete Dopants”, submitted;
- [18] M. Toledano-Luque *et al.*, “From Mean Values to Distributions of BTI Lifetime of Deeply Scaled FETs through Atomistic Understanding of the Degradation”, in *Proc. VLSI Symp. 2011*, pp. 152-153;
- [19] B. Kaczer, Ph.J. Roussel, T. Grasser, and G. Groeseneken, “Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices—Application to NBTI”, in *IEEE Electron Device Letters*, Vol. 31, no. 5, 2010, pp. 411-413.