Impact of Device Parameters on the Reliability of the Magnetic Tunnel Junction Based Implication Logic Gates

H. Mahmoudi, T. Windbacher, V. Sverdlov, and S. Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria
E-mail: {Mahmoudi | Windbacher | Sverdlov | Selberherr}@iue.tuwien.ac.at

Non-volatile logic is a promising solution to overcome the leakage power issue in the off-state [1], which has become an important obstacle to scaling of CMOS technology. Magnetic tunnel junction (MTJ)-based logic has a great potential, because of the non-volatility, unlimited endurance, CMOS compatibility, and fast switching speed of the MTJ devices [2]. In our previous work [3], we have shown the realization of an intrinsic logic-in-memory architecture (also known as Stateful Logic) via material implication (IMP) (Fig. 1a), for which the MTJ devices are used simultaneously as memory elements and computing elements (logic gates). Therefore, MTJ-based IMP logic reduces the device counts by eliminating the need for CMOS-based logic elements. This is the advantage of the Stateful Logic compared to the common logic-in-memory architectures, where MTJs are used as ancillary devices for storing binary data and, therefore, the intermediate circuitry and sensing amplifiers [4] are still required. Here we study the impact of the MTJ device parameters on the reliability of the MTJ-based IMP logic gate (Fig. 1b).

The realization of the IMP logic is based on a conditional switching behavior which relies on the fact that a change in the resistance state of the source MTJ (Fig. 1b) modulates the critical current required for spin-transfer torque (STT) switching the target MTJ [3]. In fact, this state dependent modulation (SDM) opens a reliable window (RW) between the switching windows (SWs) of the desired and undesired switching events as shown in Fig. 2. The robust IMP logic behavior requires a wide enough SDM window. From a circuit point of view, for given MTJ device characteristics the value of the circuit parameters (I_{imp} and R_{G}) of the IMP gate can be optimized to minimize the error probability [3]. From a device point of view, since the resistance modulation of the MTJ is described by the tunnel magnetoresistance (TMR) ratio (TMR= (R_{AP}-R_{P})/R_{P}), we expect that the width of the SDM window increases with the TMR ratio. Fig. 3 shows that the error probability decreases with the increase of the TMR ratio, which is a dominant device parameter for the reliability. The MgO-barrier-based MTJs exhibit a very high TMR ratio (> 500%), which can be used for development of reliable implication logic gates.

According to the theoretical model [5] and the measurements [6], the switching dynamics of the MTJ can be expressed as:

$$P_{\mathrm{sw}} = 1 - \exp\left\{-\frac{t}{t_0}\exp\left[-\Delta(\mathrm{I})\left(1-\frac{I}{I_0}\right)\right]\right\} \qquad (1)$$

where Δ(I) is the thermal stability associated with the STT switching defined as Δ(I) [7], t is the pulse width, and I is the current flowing through the MTJ. Fig. 4 shows the switching dynamics of the MTJ device as a function the current for different values of Δ(I). It illustrates that a higher Δ(I) provides sharper switching dynamics (switching window). According to Fig. 2, decreasing the SWs increases the width of the reliable window (RW). Therefore, another important device parameter for the reliability is Δ(I). Fig. 5 shows the error probability of the IMP operation as a function of Δ(I). As shown in [7], although lower Δ(I) values allow easier STT switching, a minimum value of 40 is required for low write and read error rates in STT-MRAM technology. A similar trade-off is encountered in the design of the IMP logic gates.

The reliability of the IMP logic is based upon a state dependent modulation (SDM) of the critical current required for the STT switching. It has been demonstrated that the reliability increases exponentially with increasing TMR ratio as well as Δ(I). Due to non-volatility and eliminating extra charge-based logic gates, the IMP logic is expected to exhibit low power consumption, high logic density, and high speed operation simultaneously.

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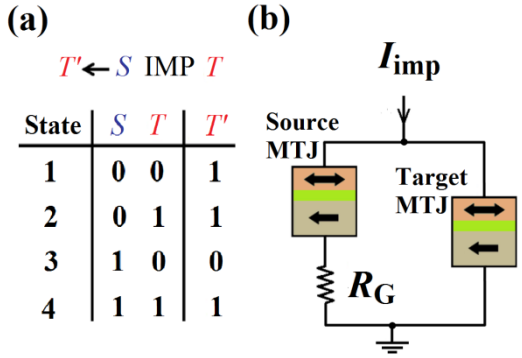

Fig. 1: The material implication (IMP) truth table (a) and the implication gate structure (b) [3]. The parallel (P) magnetization state results in a low-resistance state (R_P; logical 1) across the barrier, while the antiparallel (AP) alignment places the MTJ device in a high-resistance state (R_{AP}; logical 0).

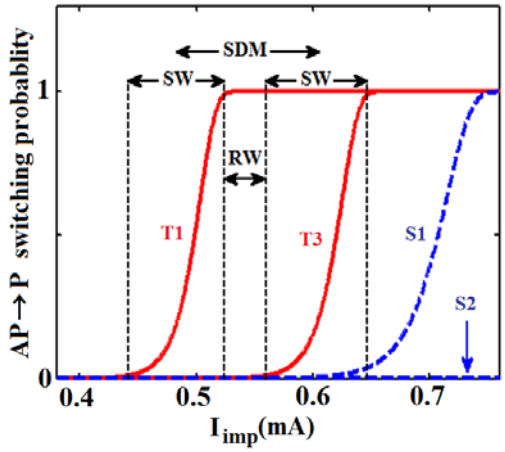

Fig. 2: AP→P switching probabilities of the source and the target MTJs (S*i* and T*i*) plotted for State *i* (*i*=1-4) with a 50 ns I_{imp} current pulse duration based on physical MTJ devices characterized in [6].

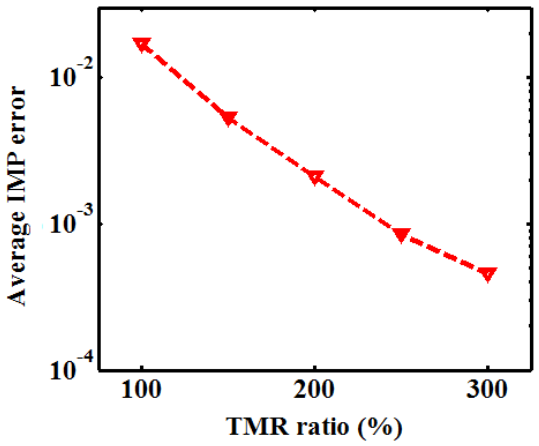

Fig. 3: The IMP average error depends on the TMR ratio plotted for Δ(I)=40 and optimized IMP gate circuit parameters (R_G and I_{imp}).

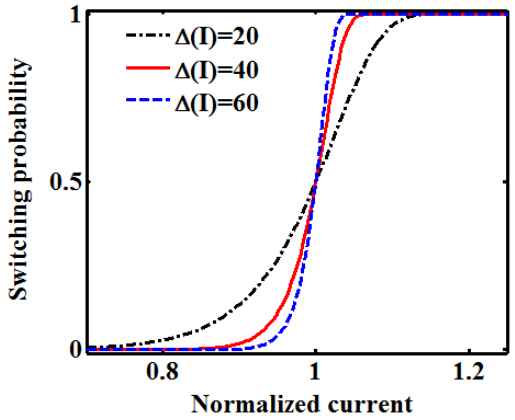

Fig. 4: Switching dynamics of the MTJ device as function of the applied current plotted for different values of Δ(I).

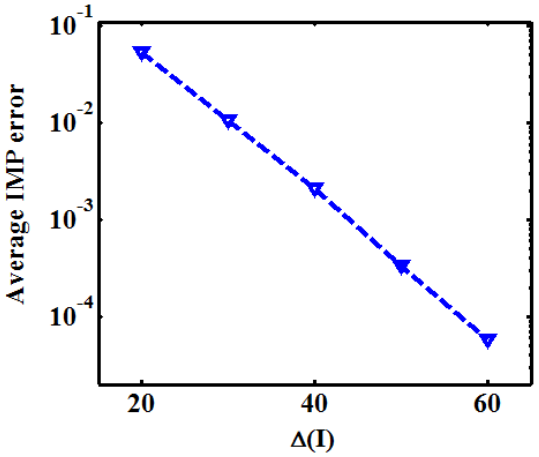

Fig. 5: The IMP average error as function of the Δ(I) plotted for TMR=200% and optimized IMP gate circuit parameters (R_G and I_{imp}).