ECS Transactions, 50 (3) 291-296 (2012)
10.1149/05003.0291ecst ©The Electrochemical Society

A Promising New n^{++}-GaN/InAlN/GaN HEMT Concept for High-Frequency Applications

V. Palankovski[a] and J. Kuzmik[a,b]

[a] AMADEA Group, Inst. for Microelectronics, TU Wien, 1040 Vienna, Austria
[b] Inst. of Elec. Engineering, Slovak Academy of Sciences, 84104 Bratislava, Slovakia

We study enhancement-mode n^{++}-GaN/InAlN/GaN high electron mobility transistors (EHEMTs) by means of two-dimensional numerical device simulation. An introduction of a highly-doped GaN cap layer, which is removed under the gate, was initially proposed for an improvement of the device performance by diminishing surface traps-related parasitic effects. Our new simulation results reveal that, unlikely to planar transistor structures, the extension of the gate depletion region with drain bias is kept restricted in the presence of an n^{++}-GaN cap layer. This highly-scaled new device concept is very promising for ultra-high frequency performance.

Introduction

Enhancement-mode operation of GaN-based HEMTs is very much desired for various electronic applications. Several different approaches have been proposed. While some rely on an additional cap layer in order to raise the conduction band [1, 2], others employ a reduction of the gate-to-channel distance by a recessed-gate technique [3, 4]. Another way for achieving it is to reduce the barrier layer thickness, which, however, has a negative impact on the access resistances [5], mainly due to the close proximity of the surface potential [6]. Compared to AlGaN/GaN structures, the InAlN/GaN HEMTs exhibit higher polarization charges even without strain in the barrier [7]. However, similarly to AlGaN/GaN, they may also suffer from parasitic effects related to surface traps. A mechanism to mitigate these effects is to use a thin n^{++}-GaN cap layer, since free carriers compensate the charge variation at the GaN trapping surface, as experimentally demonstrated in [8]. In this work we complement the experimental results with data obtained from two-dimensional numerical device simulation and we study the extension of the gate depletion region at different drain biases.

Device Description and Simulation Setup

The simulated devices are adopted from [8]. The structures consist of a 2μm GaN layer, 1nm AlN, 1nm $In_{0.17}Al_{0.83}N$, and 6nm GaN:Si cap, doped to $2x10^{20}cm^{-3}$ (see Fig.1). The gate length l_g is 0.5μm (or alternatively 0.25μm), the source-to-drain distance is 4μm, and the source-to-gate distance is 1μm. The structures are not passivated. The sum of polarization charges at the AlN interfaces equals the polarization charge ($2.8\times10^{13}cm^{-2}$) at the InAlN/GaN interface [9]. Thus, the AlN/InAlN barrier system is represented by a 2nm thick InAlN in the model. Our choice of transport model aims to achieve maximum accuracy combined with computational efficiency.

Since the drift-diffusion transport model is not able to deliver accurate results for sub-halfmicron GaN transistors, we perform hydrodynamic simulations with our two-dimensional device simulator Minimos-NT, which is well-suited for numerical analysis of GaN HEMTs using an established setup of physics-based models [10, 11]. As GaN HEMTs are unipolar devices, computational effort is reduced by neglecting the equations for holes in this work. Self-heating effects are accounted for by the lattice heat flow equation. A system of four partial differential equations: Poisson, current continuity and energy balance for electrons, and the lattice heat flow equations, is solved self-consistently. These four differential equations have material-specific parameters, such as the bandgap energy, electron mobility, thermal conductivity, etc. The dependence of these parameters on temperature, carrier energy, etc. is described by models, which are reported in previous works [10, 11].

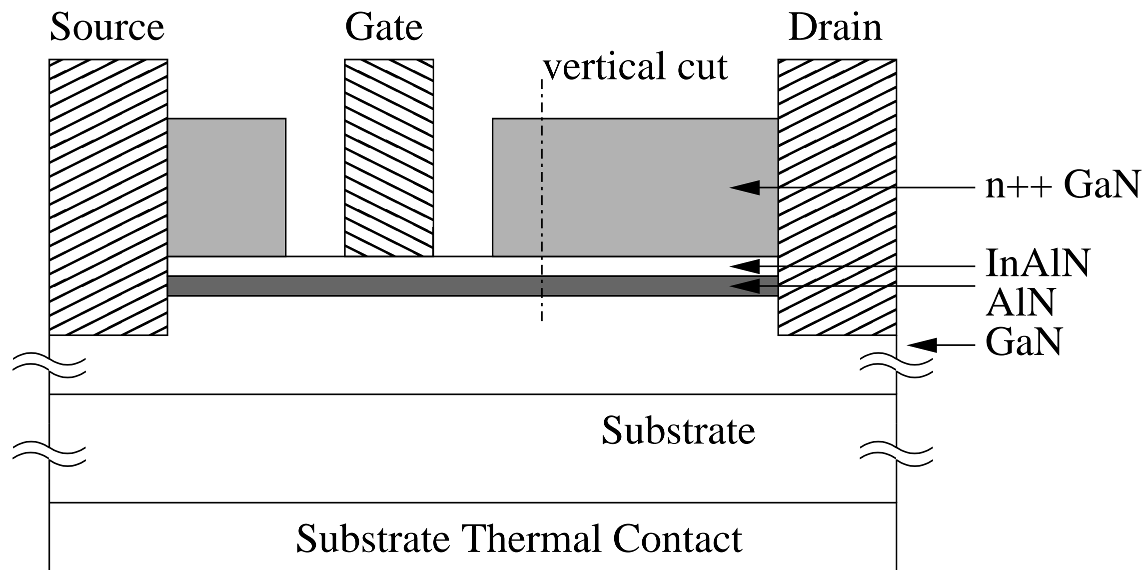

Figure 1. Schematic layer structure of GaN/InAlN/AlN/GaN EHEMT.

Simulation Results and Concusions

Excellent agreement between measured and simulated transfer characteristics and transconductances g_m of l_g = 0.5μm and l_g = 0.25μm HEMTs is obtained (see Fig.2) by using polarization charge density $2.8\times10^{13}\text{cm}^{-2}$ at the channel/barrier interface and $-2.8\times10^{13}\text{cm}^{-2}$ at the barrier/cap interface. Source and drain Ohmic contact resistivity ~1Ωmm, Schottky contact barrier height ~1.4eV, and low-field electron mobility $800\text{cm}^2/\text{Vs}$ are assumed. Fig.3 compares the simulated and the measured output characteristics of an l_g = 0.25μm device.

We further study the gate depletion region at different drain biases. It has been shown elsewhere that the extension of the depletion towards the drain is responsible for the delay in time required by electrons to cross the gate region [12]. The extension and corresponding delay was found to be invariant with the gate length. Consequently, the device speed may be substantially affected for gate lengths below 100nm [6].

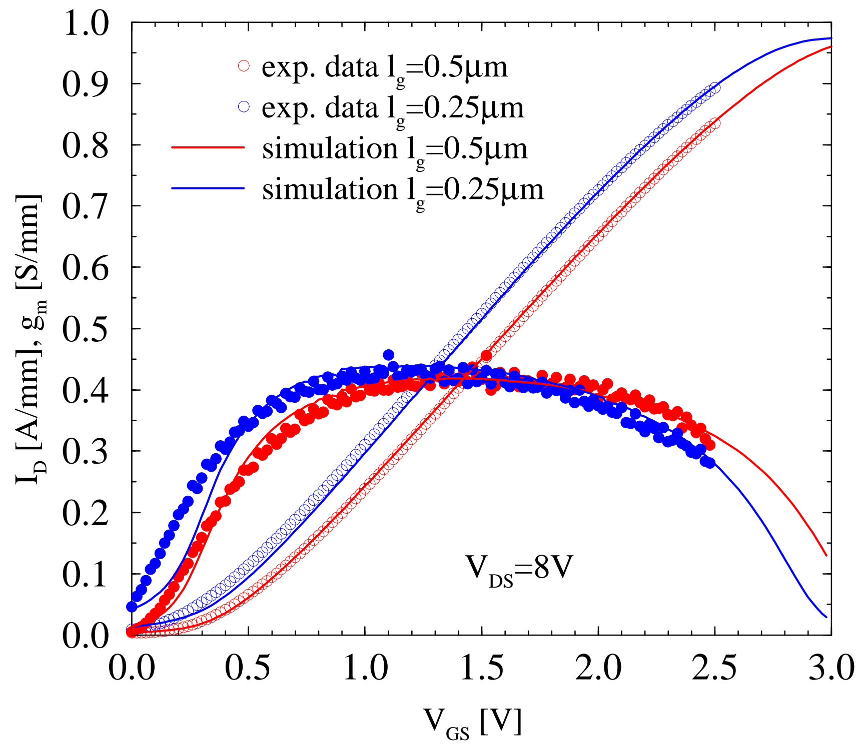

Figure 2. Comparison of simulated and measured transfer characteristics and transconductances for l_g = 0.25µm and l_g = 0.5µm EHEMTs.

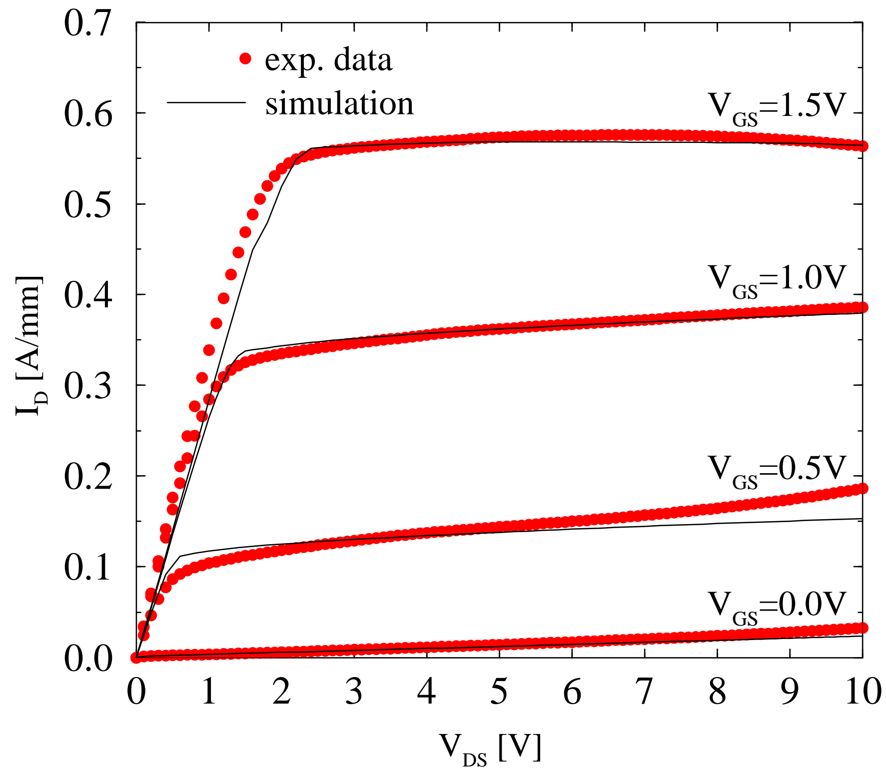

Figure 3. Comparison of simulated and measured output characteristics of a l_g = 0.25µm EHEMT.

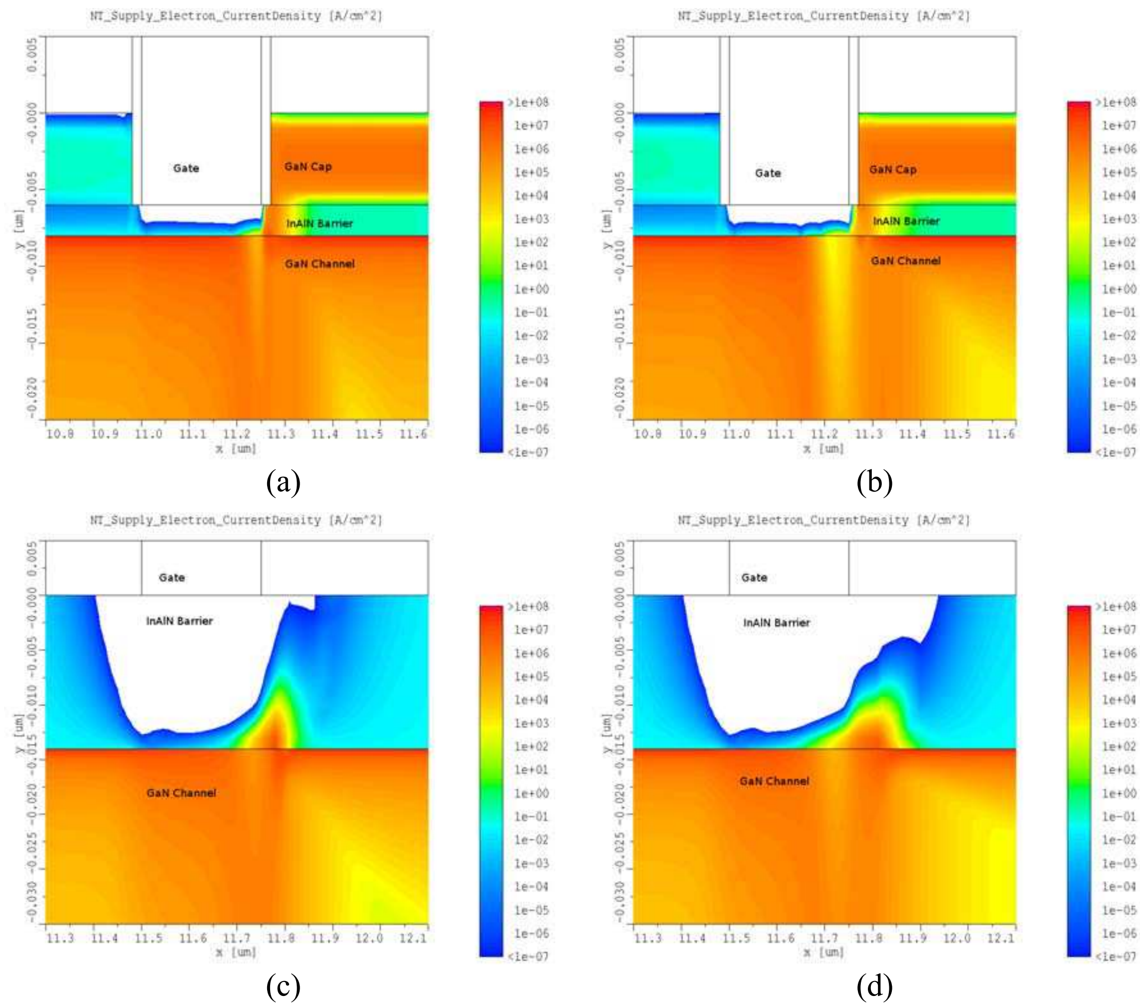

Figure 4. Electron current density [A/cm^2] in the gate regions of a n^{++}-GaN cap EHEMT (a,b) and a planar DHEMT (c,d) in on-state for V_{DS} = 8V (a,c) and V_{DS} = 20V (b,d).

To study the impact of the n^{++}-GaN cap layer on the possible increase of the gate depletion region with V_{DS}, we compare the current density and the electron concentration in the present HEMT with those in a planar depletion-mode InAlN/GaN HEMT (DHEMT) without an n^{++}-GaN cap layer. The current density contours in the InAlN barrier of the EHEMT are restricted by the edges of the n^{++}-GaN cap layers, similarly for low V_{DS} = 8V (Fig.4a) as for high V_{DS} = 20V (Fig.4b). This is unlike of a DHEMT without an n^{++}-GaN cap layer and with a 14nm barrier where the depletion region spreads significantly towards the drain contact as V_{DS} increases. Fig.4c and Fig.4d show the electron current density in the depletion mode HEMT (DHEMT) at V_{DS} = 8V and V_{DS} = 20V, respectively. The gate bias V_{GS} = −4V is chosen, so that the drain current is the same as in the EHEMT.

Fig.5 shows cross-sections in electron concentration along the channel of both DHEMT and EHEMT structures. At V_{DS} = 20V an expansion of the depletion region towards the drain by about 27nm is observed for EHEMT. This is less than a half of 62nm expansion observed for DHEMT. This reduction shows, that the combination of an n^{++}-GaN cap layer and the recessed gate may be exceptionally promising for very high-frequency devices.

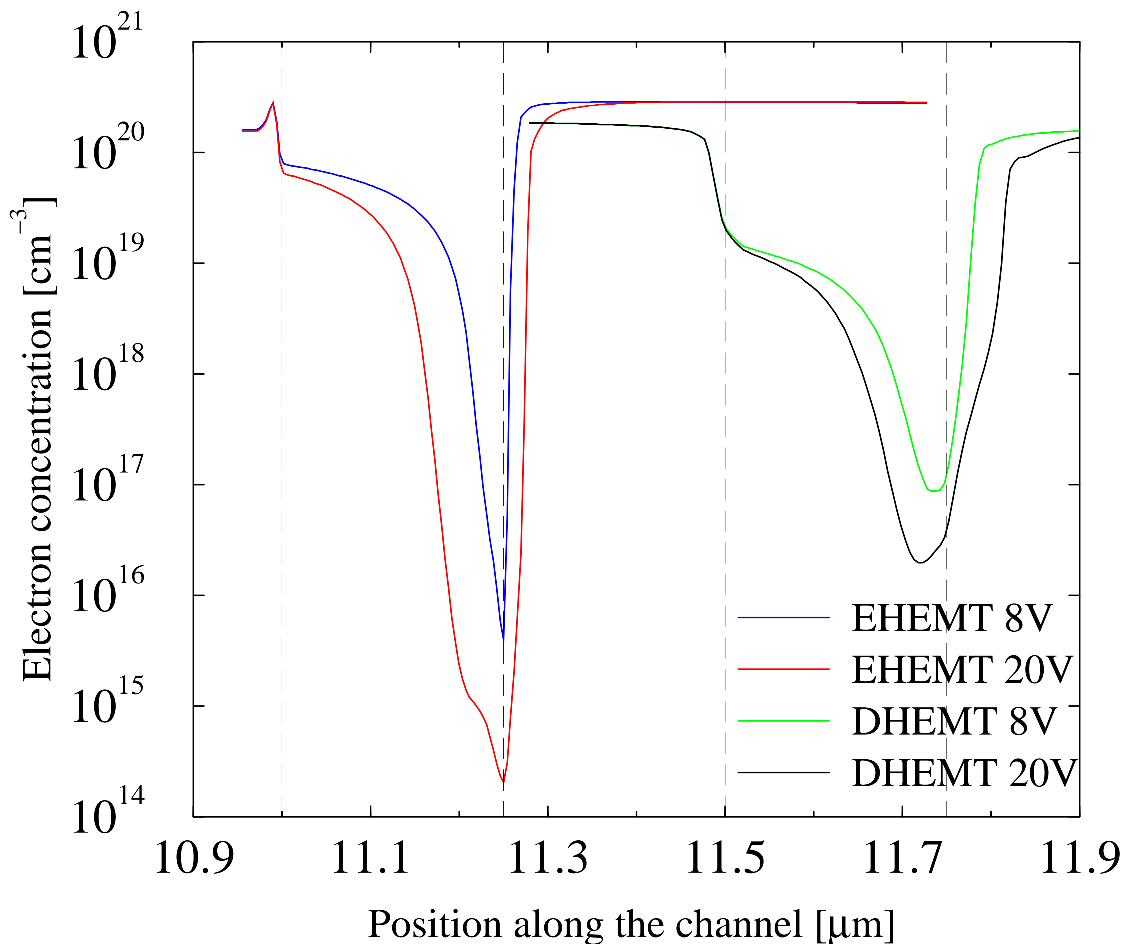

Figure 5. Comparison of electron concentration in a cut along the channels of EHEMT and DHEMT in on-state for V_{DS} = 8V and V_{DS} = 20V. Vertical dashed lines mark the positions of the respective gates.

Acknowledgments

This work was supported by the Austrian Science Funds FWF, START Project No.Y247-N13. Slovak R&D Agency Project No.APVV-0104-10 is also acknowledged.

References

1. T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, *IEEE Elec. Dev. Lett.* **28**(7), 549 (2007).
2. S. Vitanov and V. Palankovski, *Solid-State Electronics* **52**(11), 1791 (2008).
3. S. Maroldt, C. Haupt, W. Pletschen, S. Mueller, R. Quay, O. Ambacher, C. Schippel, and F. Schwierz, *Jpn. J. Appl. Phys.* **48**(4), 04C083, (2009).
4. V. Kumar, A. Kuliev, T. Tanaka, Y. Otoki, and I. Adesida, *Elec. Lett.* **39**(24), 1758 (2003).
5. Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, *Jpn. J. Appl. Phys.* **45**(44), L1168 (2006).

6. M. Higashiwaki, T. Mimura, and T. Matsui, *Phys. Stat. Solidi (a)*, **204**(6), 2042 (2007).
7. J. Kuzmik, *IEEE Elec.Dev.Lett.* **22**(11), 510 (2001).
8. J. Kuzmik, C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, J. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, Y. Douvry, C. Gaquiere, J. De Jaeger, K. Cico, K. Froehlich, K. Skriniarova, K. Kovac, G. Strasser, D. Pogany, and E. Gornik, *IEEE Tran. Elec. Dev*. **57**(9), 2144 (2010)
9. M. Gonschorek, J.-F. Carlin, E. Feltin, M.A. Py, N. Grandjean, V. Darakchieva, B. Monemar, M. Lorenz, and G. Ramm, *J. Appl. Phys.* **103**(9), 093714 (2008)
10. S. Vitanov, V. Palankovski, S. Murad, T. Roedle, R. Quay, and S. Selberherr, *IEEE Tran. Elec. Dev.* **59**(3), 685 (2012).
11. S. Vitanov, V. Palankovski, S. Maroldt, and R. Quay, *Solid-State Electronics*, **54**(10), 1105 (2010).
12. J.W. Chung, X. Zhao, Y.-R. Wu, J. Singh, and T. Palacios, *Appl. Phys. Lett.* **92**(9), 093502 (2008).