Process and Performance of Copper TSVs

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***Abstract*—The difference between the performance of TSVs manufactured using SF_6/O_2 plasma etching or a Bosch process is explored through simulations. The geometric ratio of the sample TSV is approximately 5μm:58μm. The electrical performance of the devices is explored through capacitance and resistance extraction, while the reliability is analyzed using thermo-mechanical and electromigration simulations with an applied current density of 2MA/cm^2. It is found that the plasma-etched TSV experiences higher tapering on the sidewalls, resulting in a higher TSV resistance and electromigration-induced stress.**

I. Introduction

The microelectronics manufacturing industry has aggressively scaled devices with more Moore integration over the last decades. It is expected that a physical scaling limit will be reached around the 6nm node; however, even before that limit is reached, the increased process equipment and factory costs for scaling will require other means of “more Moore” and “more than Moore” integration [1]. A major development in this direction is the through-silicon via (TSV), a three-dimensional integration technology which allows for the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced RC delay [2].

There are several processing steps which are critical to the success of the TSV fabrication, such as silicon etching, silicon dioxide deposition, and copper electroplating. The two main methods to etch the silicon layer for TSV implementation are the Bosch process and plasma etching [1]. Each process has its own flaws and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues relating to depositing layers on a scalloped wall [3]. The plasma etching of silicon results in angled sidewalls and an added wall curvature due to the via taper edge, but the rough scallops are avoided. This work compares, through simulations, the electrical and reliability properties of filled copper TSVs, when different processing technologies are implemented to etch through the silicon wafer.

II. Silicon Etching Models

The silicon etching simulations were performed using an in-house topography simulator, implemented in a Level Set framework [4] with the resulting profiles shown in Fig. 1. A 500nm layer of SiO_2 is deposited along the walls of the simulated etch profiles, followed by a 100nm layer of tantalum. The resulting aspect ratio of the TSV is approximately 5μm:58μm, which can be filled without appearing seam voids using electrochemical deposition of Cu with chemical vapor deposition of tungsten and a sputter TiW/Cu seed layer [5].

A. *TSV I: Bosch Etching using Constant Rates*

The Bosch process enables high-aspect ratio etching using alternating passivation and etching cycles and is frequently used for TSV fabrication. At the beginning of each cycle, the polymer is deposited using an isotropic rate of 10nm/second for 4 seconds. The etch parameters are listed in Table I. The simulation results in highly vertical TSV sidewalls with an angle of 89.7°. In each cycle a scallop with an approximate height of 500nm is obtained along the entire length of the TSV. The etch profile can be seen in Fig. 1(a).

B. *TSV II: Bosch Etching using Monte Carlo Simulation*

A more sophisticated transport model [6] uses the ray tracing technique in order to compute the ion and neutral fluxes at the silicon, mask, and polymer surfaces during the intermittent deposition and etching steps. The deposition step is performed in a CF_x environment with ion and neutral fluxes of $3.125 \cdot 10^{15}$atoms/(cm^2·s) and $2 \cdot 10^{18}$atoms/(cm^2·s), respectively. The parameters used during the etching cycle are listed in Table I. In Fig. 1(b), it is evident that the simulation results in a sidewall profile with scallops only near the top of the structure. After approximately 10 cycles, the sidewall becomes almost straight down to the bottom of the etched hole.

TABLE I. Etch parameters - Bosch processes.

TSV I - Constant Rates		TSV II - Monte Carlo	
Isotropic rate	40 nm/second	F flux	$1 \cdot 10^{19}$atoms/(cm^{2}s)
Directional rate	24 nm/second	Ion flux	$4.375 \cdot 10^{15}$atoms/(cm^{2}s)
	Etch time per cycle	11.2 seconds	
	Total number of cycles	110	
	Si:mask etch ratio	80:1	
	Si:polymer etch ratio	13:1 isotropic / chemical 2:1 directional / physical	

C. *TSV III: SF_6/O_2 Ion-Enhanced Plasma Etching*

Etching of silicon wafers with a SF_6/O_2 plasma has been described in [7]. The etch rate is governed by the applied bias, voltage, pressure, and the ratio of O_2 to SF_6 present in the ambient. Several tests were performed in order to deduce the best parameters for TSV etching, resulting in those listed in Table II. The simulation fluxes corresponding to the etch condition are also given, resulting in the structure in Fig. 1(c).

TABLE II. Etch parameters - SF_6/O_2 plasma.

Experimental		TSV III - Simulation	
SF_6 concentration:	35 sccm	SF_6 flux:	$4.5 \cdot 10^{18}$ atoms/(cm^{2}s)
O_2 concentration:	45 sccm	O_2 flux:	$6 \cdot 10^{17}$ atoms/(cm^{2}s)
Pressure:	25 mTorr	Ion flux:	$1 \cdot 10^{16}$ atoms/(cm^{2}s)
RF bias:	-120 V	Time:	27 minutes

III. Simulated TSV Performance

The parasitic capacitance between the copper layer and the bulk silicon for each TSV is shown in Fig. 2. Even though the TSV depths are identical and the deposited oxide thickness is 500nm for each structure, there is some variation of the low-frequency capacitance values. The extracted capacitance and TSV resistance are given in Table IV, showing that

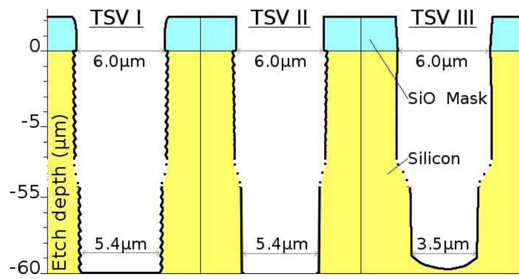


Fig. 1. Effects of the implemented etch technology on the TSV sidewall.

the increased number of scallops leads to an increased low-frequency capacitance. Due to the thinning of the plasma-etched structure, it has the highest resistance at 156mΩ, while the Bosch-etched structures have a resistance of 120mΩ.

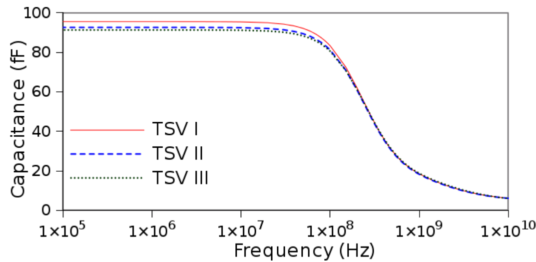
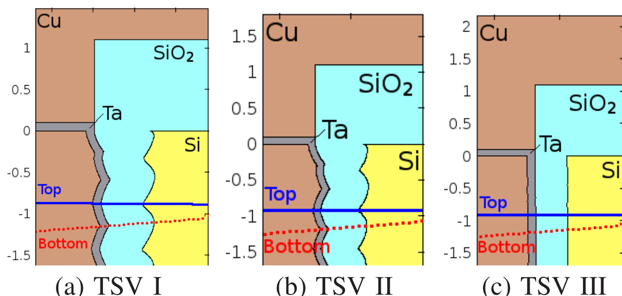


Fig. 2. Simulated frequency dependence of the TSV parasitic capacitance.

The thermo-mechanical stress was analyzed for each structure by applying a ΔT=300°C (temperature drop from 300°C to 0°C), to simulate the structure cooling after a thermal processing step, and examining the stress in the structures due to the variation in the coefficient of thermal expansion (CTE) between each material. Table III lists the resulting stresses at each material interface. The maximum stress increases with the presence of scallops, while the average stress along the interfaces remains relatively unchanged. Fig. 4 shows the stress distribution along the one-dimensional cut lines depicted in Fig. 3. The locations of the top and bottom line were chosen to reflect expected points of increased stress, where two scallops connect. The scalloped structures experience a higher stress in the silicon layer, while the plasma-etched structure has high stress in the copper layer. This higher stress arises due to the thinning of the copper line on the TSV bottom, noted in Fig. 1, allowing for less volume where the copper could compensate for the applied pressure.



(a) TSV I (b) TSV II (c) TSV III

Fig. 3. Two-dimensional view of the TSV top with materials labeled.

Electromigration (EM) analyses were performed on the structures using a model presented in [8], with the resulting maximum current density J_{max} and maximum EM-induced

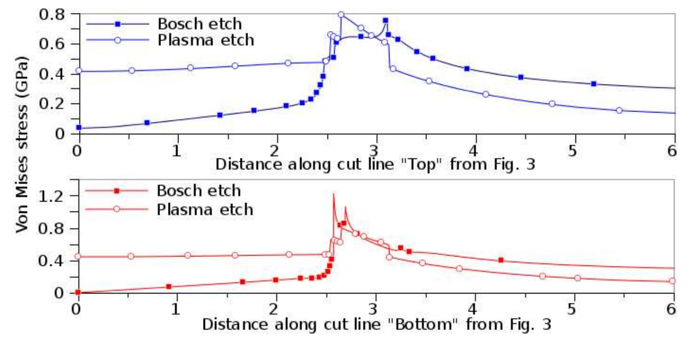


Fig. 4. Thermo-mechanical stress (Von Mises) through the TSVs.

TABLE III. THEMO-MECHANICAL STRESS AT MATERIAL INTERFACES.

	Maximum Stress (MPa)			Average Stress (MPa)		
Interface	**TSV I**	**TSV II**	**TSV III**	**TSV I**	**TSV II**	**TSV III**
Si/SiO_2	1436	1035	578	521	497	481
SiO_2/Ta	1740	1224	800	719	687	697
Ta/Cu	1410	1190	684	563	526	559

stress σ_{max} listed in Table IV. The simulations were performed to replicate device operation for 300hrs with a 2.0MA/cm^2 current density applied through the top of the structure. Due to the sloped sidewalls of the plasma-etched TSV, it experiences the highest current density at the TSV bottom, causing it to also experience the highest EM-induced stress.

TABLE IV. ELECTRICAL AND RELIABILITY RESULTS.

Parameter	TSV I	TSV II	TSV III
Resistance (mΩ)	120	121	156
Capacitance (fF)	95.6	92.6	91.3
J_{max} (MA/cm^2)	2.5	2.4	5.2
σ_{max} (MPa)	620	447	1402

IV. CONCLUSION

The performance of several TSVs has been tested through simulations. Two different methods for modeling the Bosch process and a SF_6/O_2 plasma etch model were used to simulate the resulting profile after etching through the silicon wafer. The Bosch-etched TSVs result in highly vertical, scalloped sidewalls, while the plasma-etched TSVs have a significantly tapered sidewall. The simulated topographies of the structures were imported into a finite element simulator in order to compare the performances of the different devices. The plasma-etched TSV experiences a smaller thermo-mechanical stress, but at the cost of a significantly higher electromigration-induced stress and higher TSV resistance.

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