Process and Performance of Copper TSVs

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Abstract—The difference between the performance of TSVs manufactured using SF$_6$/O$_2$ plasma etching or a Bosch process is explored through simulations. The geometric ratio of the sample TSV is approximately 5µm:58µm. The electrical performance of the devices is explored through capacitance and resistance extraction, while the reliability is analyzed using thermo-mechanical and electromigration simulations with an applied current density of 2MA/cm$^2$. It is found that the plasma-etched TSV experiences higher tapering on the sidewalls, resulting in a higher TSV resistance and electromigration-induced stress.

I. INTRODUCTION

The microelectronics manufacturing industry has aggressively scaled devices with more Moore integration over the last decades. It is expected that a physical scaling limit will be reached around the 6nm node; however, even before that limit is reached, the increased process equipment and factory costs for scaling will require other means of “more Moore” and “more than Moore” integration [1]. A major development in this direction is the through-silicon via (TSV), a three-dimensional integration technology which allows for the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced RC delay [2].

There are several processing steps which are critical to the success of the TSV fabrication, such as silicon etching, silicon dioxide deposition, and copper electroplating. The two main methods to etch the silicon layer for TSV implementation are the Bosch process and plasma etching [1]. Each process has its own flaws and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues relating to depositing layers on a scalloped wall [3]. The plasma etching of silicon results in angled sidewalls and an added wall curvature due to the via taper edge, but the rough scallops are avoided. This work compares, through simulations, the electrical and reliability properties of filled copper TSVs, when different processing technologies are implemented to etch through the silicon wafer.

II. SILICON ETCHING MODELS

The silicon etching simulations were performed using an in-house topography simulator, implemented in a Level Set framework [4] with the resulting profiles shown in Fig. 1. A 500nm layer of SiO$_2$ is deposited along the walls of the simulated etch profiles, followed by a 100nm layer of tantalum. The resulting aspect ratio of the TSV is approximately 5µm:58µm, which can be filled without appearing seam voids using electrochemical deposition of Cu with chemical vapor deposition of tungsten and a sputter TiW/Cu seed layer [5].

A. TSV I: Bosch Etching using Constant Rates

The Bosch process enables high-aspect ratio etching using alternating passivation and etching cycles and is frequently used for TSV fabrication. At the beginning of each cycle, the polymer is deposited using an isotropic rate of 10nm/second for 4 seconds. The etch parameters are listed in Table I. The simulation results in highly vertical TSV sidewalls with an angle of 89.7°. In each cycle a scallop with an approximate height of 500nm is obtained along the entire length of the TSV. The etch profile can be seen in Fig. 1(a).

B. TSV II: Bosch Etching using Monte Carlo Simulation

A more sophisticated transport model [6] uses the ray tracing technique in order to compute the ion and neutral fluxes at the silicon, mask, and polymer surfaces during the intermittent deposition and etching steps. The deposition step is performed in a CF$_4$ environment with ion and neutral fluxes of 3.125·10$^{18}$atoms/(cm$^2$·s) and 2·10$^{18}$atoms/(cm$^2$·s), respectively. The parameters used during the etching cycle are listed in Table II. In Fig. 1(b), it is evident that the simulation results in a sidewall profile with scallops only near the top of the structure. After approximately 10 cycles, the sidewall becomes almost straight down to the bottom of the etched hole.

TABLE I. ETCH PARAMETERS - BOSCH PROCESSES.

<table>
<thead>
<tr>
<th>Process</th>
<th>Isotropic rate</th>
<th>Directional rate</th>
<th>Etch time per cycle</th>
<th>Si:polymer etch ratio</th>
<th>Si:mask etch ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV I</td>
<td>40 nm/second</td>
<td>24 nm/second</td>
<td>11.2 seconds</td>
<td>2:1 isotropic</td>
<td>80:1</td>
</tr>
<tr>
<td>TSV II</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

C. TSV III: SF$_6$/O$_2$ Ion-Enhanced Plasma Etching

Etching of silicon wafers with a SF$_6$/O$_2$ plasma has been described in [7]. The etch rate is governed by the applied bias, voltage, pressure, and the ratio of O$_2$ to SF$_6$ present in the ambient. Several tests were performed in order to deduce the best parameters for TSV etching, resulting in those listed in Table II. The simulation fluxes corresponding to the etch condition are also given, resulting in the structure in Fig. 1(c).

TABLE II. ETCH PARAMETERS - SF$_6$/O$_2$ PLASMA.

<table>
<thead>
<tr>
<th>Process</th>
<th>SF$_6$ concentration</th>
<th>O$_2$ concentration</th>
<th>RF bias</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Experiment</td>
<td>35 sccm</td>
<td>45 sccm</td>
<td>-120 V</td>
<td>27 minutes</td>
</tr>
<tr>
<td>TSV III</td>
<td>45 sccm</td>
<td>35 sccm</td>
<td>6·10$^{17}$ atoms/(cm$^2$·s)</td>
<td></td>
</tr>
</tbody>
</table>

III. SIMULATED TSV PERFORMANCE

The parasitic capacitance between the copper layer and the bulk silicon for each TSV is shown in Fig. 2. Even though the TSV depths are identical and the deposited oxide thickness is 500nm for each structure, there is some variation of the low-frequency capacitance values. The extracted capacitance and TSV resistance are given in Table IV, showing that
the increased number of scallops leads to an increased low-frequency capacitance. Due to the thinning of the plasma-etched structure, it has the highest resistance at 156mΩ, while the Bosch-etched structures have a resistance of 120mΩ.

The thermo-mechanical stress was analyzed for each structure by applying a \( \Delta T = 300 \) °C (temperature drop from 300°C to 0°C), to simulate the structure cooling after a thermal processing step, and examining the stress in the structures due to the variation in the coefficient of thermal expansion (CTE) between each material. Table III lists the resulting stresses at each material interface. The maximum stress increases with the presence of scallops, while the average stress along the interfaces remains relatively unchanged. Fig. 4 shows the stress distribution along the one-dimensional cut lines depicted in Fig. 3. The locations of the top and bottom line were chosen to reflect expected points of increased stress, where two scallops connect. The scalloped structures experience a higher stress in the silicon layer, while the plasma-etched structure has high stress in the copper layer. This higher stress arises due to the thinning of the copper line on the TSV bottom, noted in Fig. 1, allowing for less volume where the copper could compensate for the applied pressure.

Electromigration (EM) analyses were performed on the structures using a model presented in [8], with the resulting maximum current density \( J_{\text{max}} \) and maximum EM-induced stress \( \sigma_{\text{max}} \) listed in Table IV. The simulations were performed to replicate device operation for 300hrs with a 2.0MA/cm\(^2\) current density applied through the top of the structure. Due to the sloped sidewalls of the plasma-etched TSV, it experiences the highest current density at the TSV bottom, causing it to also experience the highest EM-induced stress.

IV. CONCLUSION

The performance of several TSVs has been tested through simulations. Two different methods for modeling the Bosch process and a SF\(_6\)/O\(_2\) plasma etch model were used to simulate the resulting profile after etching through the silicon wafer. The Bosch-etched TSVs result in highly vertical, scalloped sidewalls, while the plasma-etched TSVs have a significantly tapered sidewall. The simulated topographies of the structures were imported into a finite element simulator in order to compare the performances of the different devices. The plasma-etched TSV experiences a smaller thermo-mechanical stress, but at the cost of a significantly higher electromigration-induced stress and higher TSV resistance.

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007–2013) agreement no. 318458 SUPERTHEME.

REFERENCES