Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO$_2$/HfO$_2$ pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks


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Abstract

We study charge trapping in a variety of Ge-based pMOS and nMOS technologies, either with Si passivation and conventional SiO$_2$/HfO$_2$ gate stack, or with GeO$_x$/high-k gate stacks. A general model for understanding this phenomenon in alternative substrate/dielectric systems is proposed. We discuss two different approaches to pursue a reduction of charge trapping in alternative material systems, which will be necessary for achieving reliable high-mobility devices.

Introduction

High mobility materials will be required for next technology nodes [1]. In particular, Ge and III-V compounds [2] are the first candidates for $p$- and $n$-type channels respectively, although a Ge CMOS integration is also considered [3]. The development of compatible dielectric stacks (i.e., preserving carrier mobilities), is currently impeded by severe border trap charging, which induces trapping already at low operating voltage and short times, consistent with literature data of $I-V$ hysteresis. We discuss two different approaches for reducing charge trapping in these gate stacks, namely defect passivation and defect energy decoupling, and we show how the latter represents the most effective way to salvage the device reliability.

Ge devices with Si passivation and SiO$_2$/HfO$_2$ stack

A. Relaxed-Ge pMOS

We have previously shown improved reliability in SiGe pMOS, ascribed to carrier-defect energy decoupling [5]. Additional energy displacement is expected for $r$- and $s$-Ge channels (Fig. 1). For different energy injection levels, representing SiGe ($\Delta E \approx 0.3eV$) and Ge ($\Delta E \approx 0.5eV$) valence bands, the same effective channel carrier-defect energy decoupling is observed depending on the considered $V_{ov}$ range, ranging from $\gamma(V_{ov})=\gamma_1$ for standard device lifetime extrapolation based on power laws with constant exponents ($\Delta V_{th}=AV_{ov}^{-\gamma}$). We propose an alternative methodology based on the defect capture time dependence on voltage [6]. By rescaling the $\Delta V_{th}(t)$ traces recorded at different $V_{ov}$ along the time axis (Fig. 3) a universal curve is obtained, clearly showing a saturating behavior. This experimental curve is perfectly described by a Cumulative Lognormal, representing the distribution of capture time constants induced by the Normal distribution of energy levels (since $t_c \approx t_0 \exp(E_d/k_B T)$, with $E_d$ being the distribution of defect energy levels [6]).

Process parameters as the channel doping level or the Si cap thickness [5] can modify the carrier-defect alignment and ‘speed up’ the charge capture process (Fig. 4).

While we and others have previously suggested the existence of such defect band based on extrapolation [5,6] or extremely harsh accelerated tests [7,8], the particular alignment of the Fermi level in the $r$-Ge channel allows for its direct observation in a measurable window. Fig. 5 shows a calculation of our defect band model [5], where the Normal parameters have been fitted to yield the typically observed voltage acceleration $\gamma\approx 3$ for Si, in the measurable $\Delta V_{th}$ range. For different energy injection levels, representing SiGe ($\Delta E \approx 0.3eV$) and $r$-Ge ($\Delta E \approx 0.5eV$) valence bands, the same defect band is expected to induce different $\Delta V_{th}(V_{ov})$ curves. A higher $\gamma$ is expected at low $V_{ov}$ with a curvature becoming apparent within the measurable window for $r$-Ge, as observed experimentally (Fig. 5c).
B. BTI Extrapolation for Alternative Material Systems

Due to the curved log(ΔVth)-log(time) evolution, standard device lifetime extrapolation based on power law acceleration models yield inconsistent results depending on the considered Vow range (Fig. 6a). In contrast, the time scaling factors needed to construct the universal degradation curve (cf. Fig. 3) show a single power law dependence of the voltage over the whole observed defect capture time range (~16 decades), independently of the curved ΔVth evolution. The exponent of this power law (\( r = V_{ow}^{-\gamma} \)) represents the convolution of the typically used time and voltage acceleration exponents (\( n \) and \( \gamma \)). A higher \( \xi \) value (\( \xi \approx 46 \) for r-Ge and \( \approx 21 \) for Si) suggests larger carrier-defect energy decoupling (cf. Figs. 5b and 16).

C. Strained-Ge pMOS

To surpass the performance of state-of-the-art Si technology, Ge channel devices will need strain engineering as well [9-10], which induces additional valence band offset [11] (cf. Fig. 1). Consistent with our model, further reliability improvement is observed in s-Ge planar and finFET [10] devices with Si passivation and SiO2/HfO2 stack (Fig. 7).

D. Relaxed-Ge nMOS

Given the superior reliability of Ge pMOS with Si passivation, the same gate stack is of interest also for nMOS. Sufficient nMOS reliability (Fig. 8), comparable with benchmark Si data [12] is indeed observed, in agreement with our model (Ge and Si conduction bands almost align [11], yielding the same carrier-defect energy coupling). However, poor electron mobility has been reported for this gate stack [14], moving research interest toward alternatives [3].

Ge channel devices with GeOx/high-k gate stacks

We studied charge trapping in p- and n- channel devices with a variety of GeOx-based gate stacks (Table I). Severe I-V hysteresis is observed, consistent with literature [3] (Fig. 9). This excessive charge trapping also affects carrier mobility (Fig. 10). As noted above, higher channel doping is consistently observed to accelerate charge trapping (Fig. 11). Fig. 12 shows a benchmark of the measured ΔVth after a pulse of constant duration and amplitude vs. the Tinv of the considered stacks. Unacceptable shifts are observed in all cases, with larger shifts for nMOS compared to pMOS. As discussed, different carrier-defect alignments in different stacks can yield different apparent voltage and time accelerations, depending on the measured Vow range (Fig. 13). Hence benchmarking different materials at fixed time and Vow conditions can be misleading. A correct benchmarking is obtained by extrapolating the maximum operating Vow of each gate stack (Fig. 14) with the method we propose (cf. Fig. 6). None of the studied alternative stacks provides sufficient reliability (max. Vow<0.5V target). nMOS show reduced reliability for scaled Tinv, while the opposite trend in pMOS suggests hole trapping sites located mainly in the GeOx IL.

Strategies for achieving reliable Ge and III-V devices

For Ge and III-V reliability improvement, two possible approaches can be pursued (Fig. 15): 1) defect density reduction, or 2) selection of a substrate/dielectric system with sufficient carrier-defect energy decoupling. While the former approach is surely beneficial (cf. experimental data w/ and w/o surface cleaning optimization in Fig. 14), the latter approach is clearly more effective. For the screening of alternative systems, the extracted values of \( \xi \) represents a powerful metric for estimating carrier-defect energy decoupling (Fig. 16).

Conclusions

Ge devices with SiO2/HfO2 dielectric offer suppressed charge trapping, owing to an effective carrier-defect energy decoupling. Based on a thorough study of this material system, we have proposed a general model for understanding of trapping in alternative substrate/dielectric systems. Finally we have introduced a universal metric to identify systems with sufficient carrier-defect energy decoupling, necessary for achieving reliable high-mobility devices.

References

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Fig. 1: Band diagram of SiO₂/HfO₂ gate stacks with Si, SiGe, r-Ge, and s-Ge channel materials. On Ge-based channels, SiO₂ is obtained by oxidation of a thin epi-Si passivation layer (not shown, i.e., fully consumed). Note the different alignments of the valence band (dashed lines) for the different materials.

Fig. 2: (a) $\Delta V_{th}$ induced by charge trapping as measured at varying gate overdrive voltage ($V_{ov}$) with the eMMS technique on r-Ge/Si/SiO₂/HfO₂ pMOS. Interface state ($\nu_{Si}$) generation at room temperature as measured with the charge pumping technique was observed to be negligible (cf. $\Delta V_{th}$, dashed lines vs. symbols). For $V_{ov}$<1.8V, the $\Delta V_{th}$ was below the detection limit (~1mV), already suggesting a very good reliability of this stack. Thanks to the low initial $\nu_{Si}$ of Ge pMOS, dielectric breakdown does not cause measurement issues for $V_{ov}$≤3.8V. Note the $\Delta V_{th}$ traces cannot be described by typical power law dependences on time and voltage (i.e., $\Delta V_{th}=C_{th}V_{ov}^{\gamma}$), since the time exponent $\gamma$ (b) the voltage acceleration exponent $\gamma$ vary significantly depending on the $V_{ov}$ range.

Fig. 3: (a) Extended $\Delta V_{th(\text{max},V_{ov})}$ dataset, with finer voltage step resolution at low $V_{ov}$, showing the monotonic decrease of the time exponent $n$ with increasing $V_{ov}$. (b) The $\Delta V_{th}$ traces measured at different $V_{ov}$, rescaled along the time axis yield a single universal degradation curve, which shows a clear saturation. The trace corresponding to $V_{ov}$=2.2V was chosen as pivot (i.e. rescaled $t_{\text{stress}}=t_{\text{stress}}$, for $V_{ov}$=2.2V). The time-rescaled experimental data are perfectly described by a Cumulative Lognormal distribution (line) multiplied for the standard deviation of the fitted distribution $\sigma=10^{-225}$ is in agreement with the values extrapolated with the Capture-Emission-Time modeling for Si/SiO₂/HfO₂. Note the experimental $\Delta V_{th}$ data going above the mean of the distribution. (c) Same data plotted on a Lognormal Probit scale.

Fig. 4: $\Delta V_{th(\text{max},V_{ov})}$ data rescaled as in Fig. 5: (a) Sketch of a defect band in the dielectric bandgap: more defects become energetically favorable for channel carrier with increasing $V_{ov}$; the saturating universal curve of Fig. 3b represents the integral of the defect band. Note different channel materials yield thickness and channel doping. A thicker different carrier energy injection levels (cf. Fig. 1). (b) Calculated $\Delta V_{th}(V_{ov})$ for a Normal distribution of defect energy levels [5]. The defect Si cap [5] and a higher doping level (cf. band parameters were fitted to yield a typically observed voltage acceleration exponent $\gamma=3$ for Si devices. Then the same parameters were Fig. 11) change the carrier energy used to calculate the expected $\Delta V_{th}$ for SiGe devices [5] (valence band offset $\Delta E-V_{h}$ for r-Ge devices ($\Delta E-V_{h}$) Note the injection level and ‘speed up’ the clearly curved $\Delta V_{th}$ evolution showing up in the measurable window (white area, i.e. $\Delta V_{th}$=0.1V) in the latter case. The simulated trends degradation, reducing the device lifetime. well describe the experimental $\Delta V_{th(\text{max},V_{ov})}$ data for Si, SiGe, r-Ge devices with identical SiO₂/HfO₂ gate stacks (lines are guides to the eye).

Fig. 5: (a) Sketch of a defect band in the dielectric bandgap: more defects become energetically favorable for channel carrier with increasing $V_{ov}$; the saturating universal curve of Fig. 3b represents the integral of the defect band. Note different channel materials yield thickness and channel doping. A thicker different carrier energy injection levels (cf. Fig. 1). (b) Calculated $\Delta V_{th}(V_{ov})$ for a Normal distribution of defect energy levels [5]. The defect Si cap [5] and a higher doping level (cf. band parameters were fitted to yield a typically observed voltage acceleration exponent $\gamma=3$ for Si devices. Then the same parameters were Fig. 11) change the carrier energy used to calculate the expected $\Delta V_{th}$ for SiGe devices [5] (valence band offset $\Delta E-V_{h}$ for r-Ge devices ($\Delta E-V_{h}$) Note the injection level and ‘speed up’ the clearly curved $\Delta V_{th}$ evolution showing up in the measurable window (white area, i.e. $\Delta V_{th}$=0.1V) in the latter case. The simulated trends degradation, reducing the device lifetime. well describe the experimental $\Delta V_{th(\text{max},V_{ov})}$ data for Si, SiGe, r-Ge devices with identical SiO₂/HfO₂ gate stacks (lines are guides to the eye).

Fig. 6 (left): (a) Standard lifetime extrapolation based on power laws with constant voltage and time exponents ($\eta$ and $n$) yields different maximum operating $V_{ov}$ depending on the measured voltage window for Ge devices. (b) The time-scaling factor as used in Fig. 3b show a power law dependence on $V_{ov}$ in the whole range of the curve $\Delta V_{th}$ evolution, allowing for sound lifetime extrapolation based on a single constant exponent $\xi$. (c) Maximum $V_{ov}$ values for 4 Si wafers extrapolated with the proposed method and with the standard power laws to confirm ‘backward compatibility’. Note the lower $\xi$ value measured for Si w.r.t. r-Ge pMOS devices (~21 vs. ~46).

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further reliability improvement in compared to Si [12] and SiGe [5] baselines. Note the Ge (planar) and SiGe strain relaxed buffer (inset) [9,10].

Fig. 9: Hysteresis data of GeOx (a) nMOS and (b) pMOS plotted vs. the oxide thickness compare well to state-of-the-art device literature data (assumed measurement conditions: $V_{th}=0.7V$, $t_{sense}=10s$) [3].

Fig. 10: Correlation of charge-trapping-induced $\Delta V_{th}$ for GeOx p- and nMOS. A stronger correlation in the latter case is noted. Severe charge trapping might induce incorrect split-CV mobility extraction as suggested in [15].

Fig. 11: Charge-trapping-induced $\Delta V_{th}$ at fixed time (20ms) and $V_{ov}$ (0.5V) condition for several GeOx (a) pMOS and (b) nMOS gate stacks (cf. Table I) with two different channel doping levels. A higher doping level yields enhanced charge trapping, especially for nMOS.

Fig. 12: Charge-trapping-induced $\Delta V_{th}$ at fixed time (20ms) and $V_{ov}$ (0.5V) condition for GeOx-based pMOS (open) and nMOS (solid) vs. $T_{inv}$. All the gate stacks considered showed excessive charge trapping, above the typical reliability target. Note the weaker $T_{inv}$ (GeOx thickness, cf. Fig. 9) dependence for pMOS suggesting hole trapping sites located mainly in the GeOx, as opposed to electron trapping sites mainly located in the high-k layer (i.e., enhanced trapping in nMOS for scaled GeOx).

Fig. 13: A variety of voltage and time acceleration exponents ($\gamma$ and $n$) are observed on the various GeOx gate stacks depending on the measured range, jeopardizing any power law based lifetime extrapolation. Correct extrapolation should be based on the proposed voltage-time acceleration (cf. Fig. 6b), which yield a constant, gate stack dependent, $\xi$ exponent (cf. Fig. 16).

Fig. 14: Maximum operating $V_{ov}$ extracted with the proposed method (cf. Fig. 6b) on various GeOx-based nMOS and pMOS gate stacks. No gate stack with sufficiently low charge trapping has been identified so far. A surface preclean optimization yielded some reliability improvement, possibly due to reduced defect density (cf. Fig. 15, ‘Scenario 1’), which however is not sufficient to salvage the poor reliability of these alternative gate stacks. Note the maximum $V_{ov}$ scaling with $T_{inv}$ for nMOS gate stacks but not for pMOS.

Fig. 15: (a) Charge trapping might be suppressed by reducing the dielectric defect density (‘Scenario 1’), or by selecting a given substrate-dielectric combination which yields beneficial carrier-defect energy decoupling as for the case of (Si)Ge/SiOx/HfO2 gate stacks (‘Scenario 2’). (b) Calculated $\Delta V_{th}$ assuming a 10x $Q_{def}$ reduction by process improvement, or a constant defect density but introducing a 0.5eV energy decoupling. The latter case clearly yields a significantly higher relief at low operating $V_{ov}$.

Fig. 16: Benchmark plot of the $\xi$ exponent values extracted on a variety of CMOS technology. Higher $\xi$ values are observed for gate stacks providing good carrier defect energy decoupling (e.g., s-Ge, r-Ge, SiGe PMOS with SiO2/HfO2 dielectrics, or Si nMOS with rare earth-doped HfO2 as compared to undoped high-k [13]). Note the very low $\xi$ values extracted for all the GeOx gate stacks. The parameter $\xi$ introduced in this work can be used as a solid $T_{inv}$-independent benchmark for carrier-defect decoupling when screening alternative substrate/dielectric systems. A minimum reliability target can be set to the level of Si pMOS, i.e. $\xi \leq 20$. 

Table I: RMG Ge CMOS gate stacks

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<th>Gate Stacks</th>
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Fig. 7: Maximum $V_{ov}$ for 10-year device lifetime for r-Ge (planar) and s-Ge (planar and finFET) pMOS compared to Si [12] and SiGe [5] baselines. Note the further reliability improvement in s-Ge thanks to larger carrier-defect energy decoupling (cf. discussion about $\xi$, Fig. 16). The s-Ge channel was grown on a SiGe strain relaxed buffer (inset) [9,10].