Process and Reliability of SF$_6$/O$_2$ Plasma Etched Copper TSVs

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Abstract

The formation of a TSV for three-dimensional interconnects using SF$_6$/O$_2$ plasma is explored. Adjusting the O$_2$ gas concentration to 45 sccm, while the SF$_6$ concentration is set to 35 sccm, produced the best combination of chemical and physical etching to provide sidewall angles of 88°. Three TSV aspect ratios are etched (5/58, 10/100, and 20/100 μm) and subsequently analyzed using the finite element method. The TSVs' series resistance, current density, thermo-mechanical stress, and electromigration induced stress after 300 hours of operation at a 2MA/cm^2 current density are analyzed. An additional comparison to ideal TSVs with sidewall angles at 90° is performed.

1. Introduction

The major focus of the semiconductor industry over the last decades has been to continue integrated circuit (IC) miniaturization along with Moore's law. It is expected that a physical scaling limit will be reached around the 6nm node; however, even before that limit is reached, the increased process equipment and factory costs for scaling will require other means of "more Moore" and "more than Moore" integration [1]. A major development in this direction has been the through silicon via (TSV), which allows for vertical integration through three-dimensional (3D) stacking of ICs. The main advantages of 3D integration is the reduction of RC delay for submicron circuits, reduced power consumption, and the ability for heterogeneous integration of chips [2].

The two main methods to etch the silicon layer for TSV implementation are plasma etching and the Bosch process [1]. Each process has its own flaws and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues relating to depositing layers on a scalloped wall [3]. The plasma etching of silicon results in angled sidewalls and an added wall curvature due to the via taper edge [3]; however, the rough scallops are avoided. This work examines by means of simulation the potential of using an SF$_6$/O$_2$ plasma in order to etch TSV structures and compares their thermal and electrical performance to an ideal cylindrical TSV.

2. Silicon Etching

The etching of silicon wafers with a SF$_6$/O$_2$ plasma has been described in [4]. The etch rate is mainly governed by the applied bias voltage, pressure, and the ratio of O$_2$

to SF$_6$ in the ambient. To test the RF bias, the pressure, and the SF$_6$/O$_2$ ratio effects on the etch, each parameter is varied while the others remained constant. The constant values are set to -20V RF bias, 25mTorr pressure, and an SF$_6$/O$_2$ ratio of 1. [4]. The observations, shown in Fig. 1, lead to the conclusion that the fastest etch rate can be reached with an RF bias of -120V, pressure of 25mTorr, and an SF$_6$/O$_2$ ratio of 1. However, when etching through silicon as a step in the manufacture of TSVs, the sidewall angle is an important aspect which must not be overlooked, even at the cost of a reduced etch rate.
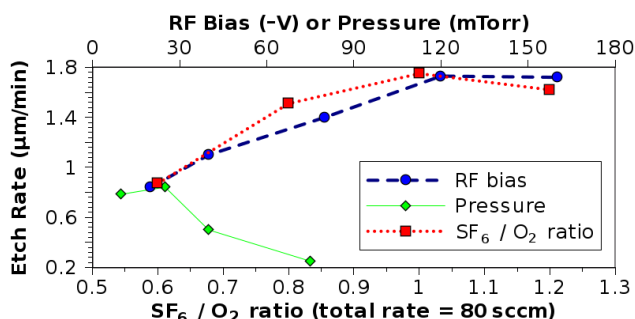

Figure 1.   Effects of process parameters on the Si etch rate. When testing the effects of one parameter on the rate, the other two are kept constant.

It has previously been determined that the effect of O$_2$ on the SF$_6$ plasma is a dramatic increase in the F atom concentration and a subsequent decrease in lateral etching [5]. Controlling the F atom concentration is essential to generating desired sidewall angles. Therefore, an etching simulation is performed for several desired TSV diameters while varying the O$_2$ concentrations, resulting in the profiles shown in Fig. 2. Table 1 describes the etch conditions for profiles A–D. From Fig. 2, it is evident that varying the O$_2$ concentration results in the variation of the lateral extents of the etched hole, but also in a variation of the overall etch rate. Increasing the presence of O$_2$ results in an overall reduction of the etch rate, both in the lateral and vertical directions.

A. Silicon Etching Model

The model for Si etching is described in [6] and it has been implemented in a level set environment, as described in [7]. From the observed profiles from Fig. 2, it is evident that the O$_2$ concentration plays a major role in determining the lateral etching and subsequent TSV sidewall angle. By increasing the O$_2$ concentration, lateral etching is

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Table 1. Experimental parameters for the simulation results
shown in Fig. 2.

Parameter	A	B	C	D
SF_6 concentration	45 sccm	40 sccm	35 sccm	30 sccm
O_2 concentration	35 sccm	40 sccm	45 sccm	50 sccm
Pressure		25mTorr		
Total gas flow rate		80 sccm		
RF bias voltage		-120V		
Wafer temperature		5°C		
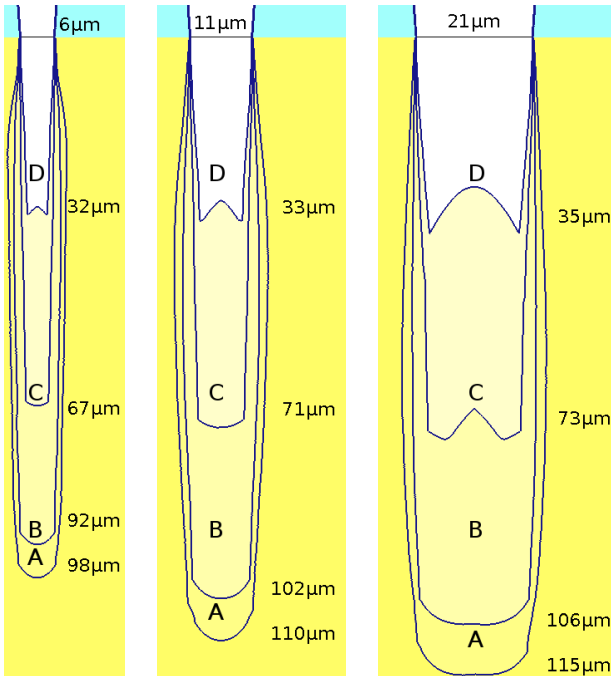
Figure 2. Etch profiles after a 30-minute etch in SF_6/O_2 plasma. The etch profiles are prepared for (left) a 5μm TSV diameter, (middle) a 10μm TSV diameter, and (right) a 20μm TSV diameter. The additional 1μm in diameter length is required in order to deposit an insulating layer of SiO_2 and a tantalum liner, prior to copper deposition. The processes (A–D) are described in Table 1.

reduced; however, at the cost of a reduced etch rate. For the purposes of TSV etching, option C with an O_2/SF_6 ratio of 1.3 is selected. The three TSV geometries tested have a diameter/depth ratio of 5μm/58μm (27 minute etch), 10μm/100μm (43 minute etch), and 20μm/100μm (43 minute etch). The resulting profiles, including the copper (Cu), tantalum (Ta), silicon dioxide (SiO_2), and silicon (Si) layers are shown in Fig. 3. The SiO_2 and Ta layers have been deposited using constant rates to obtain the desired thicknesses (400nm for SiO_2 and 100nm for Ta). The resulting hole can then be filled with copper.

The TSVs with the chosen aspect ratios can all be filled without appearing seam voids. For the 5μm/58μm TSV filling can be performed using electrochemical deposition of Cu with chemical vapor deposition of tungsten and a sputtered TiW/Cu seed layer [8]. The TSVs with the other aspect ratios can be filled using electroplating with an added 50ppm of chloride ions, as suggested in [9]. The presence of seam voids or poor sticking of the individual
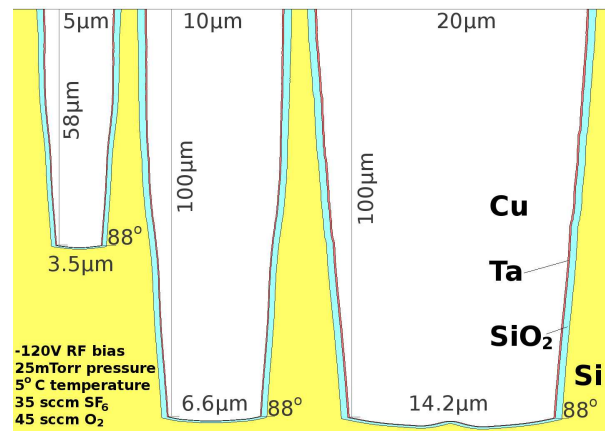

Figure 3. TSV structures after Si etching and SiO_2/Ta deposition. 5μm/59μm, 10μm/100μm, and 20μm/100μm are the TSV profiles.

materials can lead to delamination under increased stress conditions. The stress can be due to a large temperature drop which occurs during structure cooling after a thermal processing step. An additional source of stress for the structure which is analyzed is the electromigration-induced stress.

3. TSV Characterization

The TSVs are characterized according to several electrical parameters and stress distributions. It is expected that a TSV with a smaller radius will have an increased resistance. Additionally, etched structures experience some tapering (about 88°), which results in copper thinning along the depth of the TSV. This thinning is expected to increase the overall TSV resistance and the current density on the TSV bottom, when compared to an ideal cylindrical geometry. The simulated parameters are compared to the ideal cylindrical TSVs in order to estimate the effects of SF_6/O_2 etching for Cu TSVs. In addition, the thermo-mechanical and electromigration-induced stress distribution in the structure is analyzed.

Thermo-mechanical simulations of the TSVs are carried out in order to calculate the von Mises stress. This stress serves as a yield criterion for mechanical reliability and is caused by the subsequent chip cooling after an annealing step from a high temperature ($\sim$300°C) down to room temperature. The variation in the coefficient of thermal expansion (CTE) between the Cu, Ta, SiO_2, and Si layers causes the Si layer to experience tensile stress. The main concern is the CTE mismatch between Cu and Si, while the Ta liner is ignored in many studies due to its thickness being negligible compared to the SiO_2 liner. In this study, all materials which comprise the TSV structure are included in the analysis.

In addition to thermo-mechanical stress, the electromigration (EM) induced stress can be a cause for concern. EM can trigger a chip failure because of the formation and growth of voids in a metal line, such as a TSV

structure. Whether or not a void will nucleate depends on how much stress develops on the Cu line in the presence of a high current density. This current causes a movement of vacancies which are concentrated at material interfaces and grain boundaries. The stress is calculated using the model described in [10], dealing with vacancy accumulation at material interfaces.

4. Results

The TSV structures from Fig. 3 were placed between layers of tantalum (100nm) and copper and the finite element method (FEM) is used to calculate the TSVs' electrical parameters, thermo-mechanical stress, and EM induced stress.

A. Electrical Performance

The electrical performance of the TSVs is analyzed by observing the current density and resistance of the final structures. Fig. 4 shows the difference in the current density distribution through an ideal cylindrical TSV and an etched TSV. It is evident that the etched TSV, due to the tapered sidewalls, experiences an increased electric current density through the thinned Cu region.
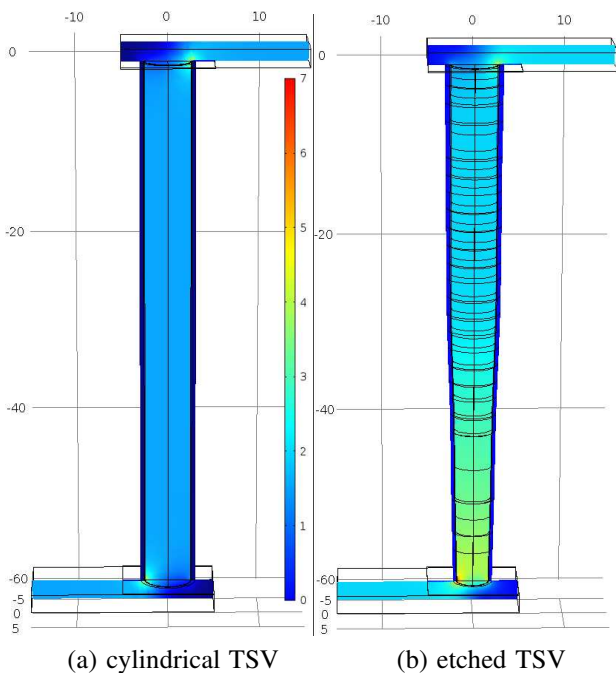

(a) cylindrical TSV   (b) etched TSV

Figure 4. Current density distribution in the 5μm/58μm TSV. The increased current density in the etched TSV is expected to result in an increased electromigration-induced stress.

Table 2 lists several characteristics of the tested TSVs. The TSV resistance is directly related to the Cu volume, while the maximum Cu and SiO_2 stresses are increased with increasing TSV diameter. The resistances of etched TSVs are also approximately 1.3–1.4 times higher than the resistances of the ideal TSVs. This difference is also noted in the approximate reduction in volume that the etched TSVs experience due to sidewall tapering.

Table 2. Simulation results for the TSVs.
5/58, 10/100, and 20/100 refer to the TSV aspect ratios.

	Volume (μm^3)			Resistance ($m\Omega$)		
	5/58	10/100	20/100	5/58	10/100	20/100
Ideal	1128	7788	31150	109	47.5	11.93
Etched	614	6080	24450	140	65.1	15.61

	Max Cu stress (GPa)			Max SiO_2 stress (GPa)		
	5/58	10/100	20/100	5/58	10/100	20/100
Ideal	1.50	1.70	1.80	1.32	1.53	1.69
Etched	1.80	1.89	2.07	1.73	1.81	2.11

B. Thermo-Mechanical Stress

The thermo-mechanical stress is an indication of the effects of device cooling after a thermal processing steps. Table 2 lists the maximum stress experienced by the copper and silicon dioxide layers for the ideal and etched TSV structures. It can be concluded that larger structures experience an increased thermal stress. This is due to a larger contact area between materials with varying CTE values. Therefore, it is important to note that, although larger TSVs allow for higher current densities and have a smaller overall resistance, they experience a higher thermal stress. In Fig. 5 the stress distribution along the top of the TSV is shown. The von Mises stress is concentrated near the Ta/SiO_2 and SiO_2/Si interfaces, while the stress is significantly reduced at a distance of approximately 5μm from the SiO_2/Si interface, through the silicon. Fig. 6 shows the thermo-mechanical stress through the silicon layer, moving away from the interface. The etched and ideal TSVs show only a slight variation, while an increased TSV size results in a higher von Mises stress through the silicon. The maximum stress in the Cu and SiO_2 for the etched TSVs is also slightly higher than that of the ideal cylindrical TSV.

(a) Top Geometry   (b) Von Mises Stress

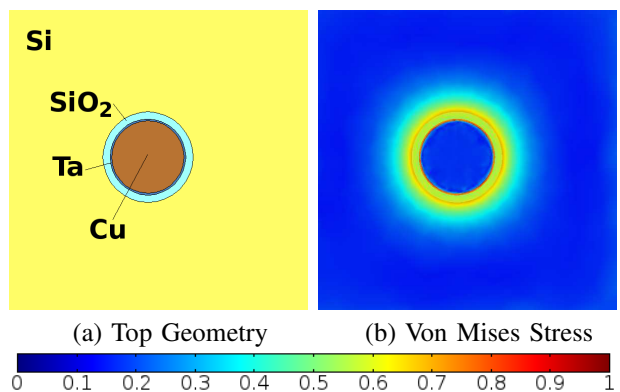0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

Figure 5. Normalized stress distribution at the top of the TSV structure. (a) Top view of the TSV with materials labeled, (b) The von Mises stress distribution (Maximum stress is about 1GPa)

C. Electromigration-Induced Stress

Electromigration is a major reliability issue for modern integrated circuits. It normally triggers a chip failure due
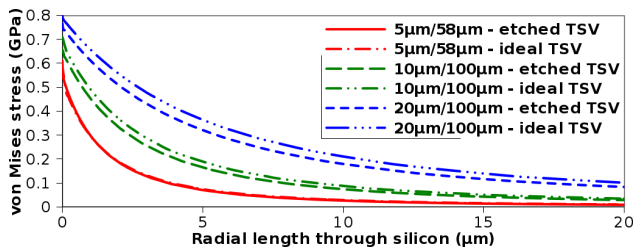
Figure 6. Maximum thermo-mechanical stress through silicon. Radial length of $0\mu m$ refers to the SiO_2/Si interface.
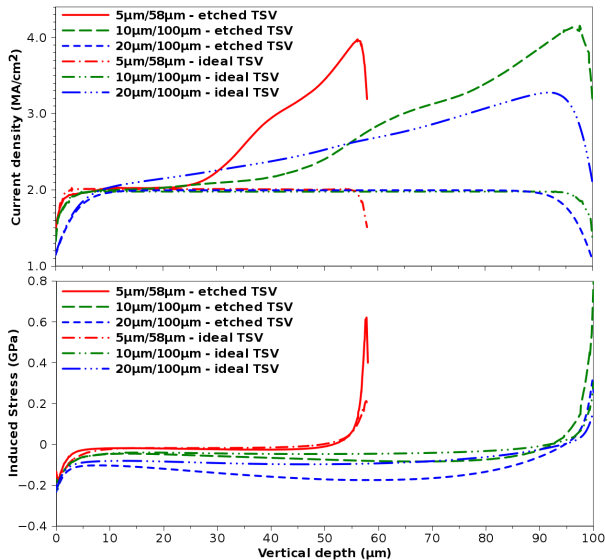

Figure 7. Current density and EM induced stress through the center of the TSV.

to formation and growth of voids in a metal line of an interconnect structure [10]. The model which is used for this study measures the stress generated in a structure prior to void formation. When the stress reaches a critical level, a small flaw could potentially be nucleated to form a void. The void formation is the first step towards void growth, resistance increase, and eventually device failure. The model used to analyze the induced stress in presented in [10].

In Fig. 7 the distribution of the current density and the EM induced stress through the center of each TSV is shown. The simulations were performed to show the level of current density and stress induced after introducing a $2MA/cm^2$ current through the top of the structure for approximately 300 hours. The link between copper thinning, and hence the current density increase, and the induced stress is evident. Fig. 8 shows the maximum stress build-up in the structure over time. The increased stress in the etched structures is noticeable; however, the smallest

structure experiences the highest stress increase. Although all etched TSVs experience approximately the same stress level, the maximum electromigration-induced stress in the smallest ideal TSV ($5\mu m/58\mu m$) is significantly lower.
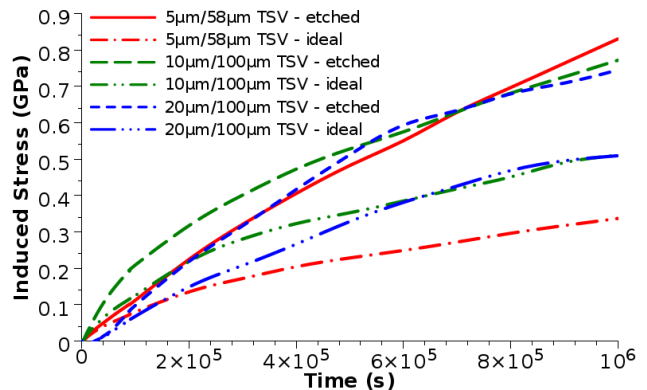

Figure 8. Current density and EM induced stress through the center of the TSV.

5. Conclusion

In this work several TSV geometries have been generated using an SF_6/O_2 plasma model, implemented in a level set framework. The resulting structures were then extracted and electrical parameters, thermo-mechanical stresses, and electromigration induced stresses were simulated. A comparison between the etched TSV and ideal cylindrical TSVs has been performed. With this work, a direct link between simulations related to TSV processing and TSV thermo-mechanical stress and reliability is realized.

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