Bias-Temperature Instability in Single-Layer Graphene Field-Effect Transistors: A Reliability Challenge

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Abstract: We present a detailed analysis of the bias-temperature instability (BTI) of single-layer graphene field-effect transistors (GFETs). We demonstrate that the dynamics can be systematically studied when the degradation is expressed in terms of a Dirac point voltage shift. Under these prerequisites it is possible to understand and benchmark both NBTI and PBTI using models previously developed for Si technologies. In particular, we show that the capture/emission time (CET) map approach can be also applied to GFETs and that recovery in GFETs follows the same universal relaxation trend as their Si counterparts. While the measured defect densities can still be considerably larger than those known from Si technology, the dynamics of BTI are in general comparable, allowing for quantitative benchmarking of the graphene/dielectric interface quality.

Introduction: Graphene has recently attracted a lot of attention due to its unique physical and electrical properties [1], making it a promising material for advanced device structures. Several successful attempts to fabricate graphene-based FETs have been undertaken so far [2, 3]. However, only a few attempts have been made at trying to understand their reliability with respect to bias-temperature instabilities [4–7], one of the key reliability issues in conventional Si MOSFETs [8, 9]. In the following, we perform a detailed study of BTI on the high-k top gate of double-gated GFETs.

Devices: Double-gated GFETs with Al_2O_3 as a top gate insulator and SiO_2 as a back gate insulator have been used, see Fig. 1, with dimensions $L = 1-4\,\mu$m and $W = 4-80\,\mu$m. The devices were fabricated by first thermal oxidation of a Si substrate using a standard lithography process [10]. The graphene layer was deposited by chemical vapor deposited (CVD) and then transferred from copper foil to the device using a well-developed standard wet graphene transfer process [3].

Experiment: The measurements were performed in vacuum (10^{-6} torr) to avoid the detrimental impact of the environment [7]. Initially, the basic device characteristics were investigated, which correspond to those published previously [4], see Fig. 2. In particular, we observe a modulation of the Dirac point voltage V_{Dirac} by the back gate bias V_{BG} as well as a hysteresis related to charging/discharging of fast oxide traps. The output characteristics measured at different top gate biases V_{TG} show a rather strong saturation at high drain bias V_{d} in some devices, see Fig. 2. Also, some kinks related to ambipolar channel effects are visible for negative V_{TG}.

Next, the impact of bias stress on the top gate transfer characteristics was examined. During top gate voltage stress, V_{BG} and V_{d} were set to zero to avoid additional shifts by e.g. hot carrier degradation. After this the evolution of the transfer characteristics during recovery was monitored for several hours/days. The experiments were repeated on the same device using increasing stress times ($t_{\mathrm{s}} = 1$, 10, 100 and 1000 s) at the same V_{TG} and at two different temperatures: $T = 25\,^{\circ}$C and $T = 75\,^{\circ}$C.

Results and discussions: Fig. 3 shows the typical impact of NBTI stress on the top gate transfer characteristics, which results in both a vertical and horizontal shift of the Dirac point, expressed by the Dirac point voltages and currents, V_{Dirac} and I_{Dirac}, respectively. These effects are most likely related to a change in the concentration of charged border traps which affect electrostatics and mobility. The presence of a vertical drift makes the frequently used (but somewhat arbitrary) definition [5–7] of the threshold voltage V_{th} as the gate bias at which $I_{\mathrm{d}} = (I_{\mathrm{dmax}} + I_{\mathrm{dmin}})/2$ questionable, as I_{d} also depends on other factors such as the contact resistance. Furthermore, it is essential to use a narrow voltage sweep interval to avoid additional degradation during the measurements.

The experimental results illustrating the time evolution of the transfer characteristics after NBTI stress are shown in Fig. 4 for $T = 25\,^{\circ}$C and $T = 75\,^{\circ}$C. As expected, a longer NBTI stress causes a stronger shift of V_{Dirac} towards the left. Significant drifts are recorded even at very low stress voltages, corresponding to about 1 MV/cm (compare to the typically used 4 – 8 MV/cm stress in Si technologies). During the recovery, V_{Dirac} returns back to its initial position with both degradation and recovery proceeding faster at higher temperature. The vertical drift, expressed by $\Delta I_{\mathrm{Dirac}}$, appears more pronounced for longer stress times and higher temperatures, although in most cases it contains some random component.

In Fig. 5 we analyze the recovery traces of the drain current shift measured with respect to the values at the Dirac point for fresh devices. From Fig. 4 we extract the raw drain current shift $\Delta I_{\mathrm{d}}(V^0_{\mathrm{Dirac}})$, the drain current shift at the Dirac point $\Delta I_{\mathrm{Dirac}}$ and the corrected drain current shift $\Delta I^*_{\mathrm{d}}(V^0_{\mathrm{Dirac}})$ which represents the sum of the two quantities. One can see that the raw I_{d} shift appears unsystematic (lower degradation after longer stress), a symptom removed in the corrected I_{d} shift by eliminating the unsystematic $\Delta I_{\mathrm{Dirac}}$ shift. However, even the corrected I_{d} shift depends on the shape of the transfer characteristics through the impact of the contact resistance. We thus conclude that $\Delta V_{\mathrm{Dirac}}$ should be used for data analysis as it depends in a simple way on the trapped charges, thereby directly exposing the most likely culprit of the degradation.

The experimental $\Delta V_{\mathrm{Dirac}}$ recovery traces obtained for four different stress times are fitted with the simulation results obtained using the CET map model [11] in Fig. 6, where the right axis corresponds to a shift of the charged trap density which can be roughly estimated as $\Delta N_{\mathrm{T}} = \Delta V_{\mathrm{Dirac}} C_{\mathrm{ox}}/2q$. The CET map model assumes that BTI is the collective response of independent defects which exchange charges with the channel following a first-order non-radiative multiphonon process. Confirmed by extensive Si datasets, the essential ingredients of the model are the widely distributed and correlated capture and emission times, which can be well described using bivariate Gaussian distributions. The top plots illustrate a fit of the model to NBTI data at two different temperatures. Clearly, the degradation at higher temperature is stronger and the recovery proceeds faster, in good agreement with the model prediction. In the bottom plot the results for PBTI stresses of different magnitudes at the same temperature are shown. Again, after a stronger stress the degradation is stronger and the recovery is slower, in agreement with the model [11]. *Contrary to Si technologies, however, device-to-device variations and the overall degradation level are found to be much larger in GFETs*. As these effects are not considered in the CET map model, simultaneous fits of data for different stress conditions and on different devices were often difficult to obtain. For example, the two sets of data shown for the NBTI case in Fig. 6 were nicely consistent, while the PBTI case was not. The extracted CET maps underlying the fits are shown in Fig. 7, which are very similar to those extracted for Si technologies [11]. One major difference is that BTI in GFETs can be described by a single Gaussian and a contribution from a more permanent component typically associated with dangling bonds at the Si interface (P_{b} centers) is absent. This is consistent with previous results and a potential strength of the 2D graphene sheet. Overall, we therefore conclude that the CET map model can be successfully applied to GFETs as well.

For a final comparison with Si technology, Fig. 8 illustrates that the BTI recovery normalized to the extrapolated recovery with zero delay also follows the universal relaxation relation [12, 13], $f(\xi) = 1/(1+B\xi^{\beta})$, where $\xi = t_{\mathrm{r}}/t_{\mathrm{s}}$ is the normalized relaxation time and B and β are empirical fitting parameters. Moreover, the parameters given in the middle plot are very similar to those obtained from Si data, *confirming the similarity in the underlying physical degradation processes*. Again, no permanent ('dangling bond') component needed to be taken into account during the extraction.

Conclusions: We have performed a detailed analysis of BTI in GFETs and compared those findings to Si technology. Despite their early stage of development, it has been demonstrated that when degradation and recovery are analyzed in terms of a Dirac point voltage shift, which is directly related to the trapped charge concentration, the dynamics are fully compatible with what is observed in Si technologies. While the measured trap densities appear to be two orders of magnitude larger, we have established a systematic method for benchmarking these exciting new technologies.

References

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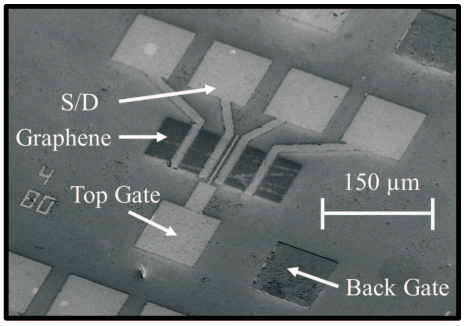

Figure 1: Scanning-electron microscopy (SEM) image of the investigated double-gated GFETs. The aluminum oxide is used as a top gate dielectric and SiO_2 as a back gate dielectric. The top gates are made of TiAu and the back gates of Al.

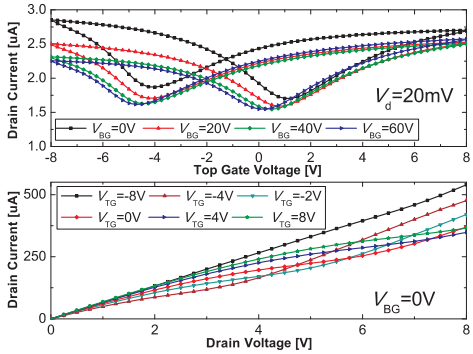

Figure 2: Top: The top gate transfer characteristics of the double gate GFET. In agreement with literature [4], we observe a hysteresis due to charging/discharging of fast traps as well as a modulation of Dirac point position by V_{BG}. **Bottom**: The output characteristics of the GFET show signs of saturation at high V_d and some kinks related to ambipolar channel effects at negative V_{TG}.

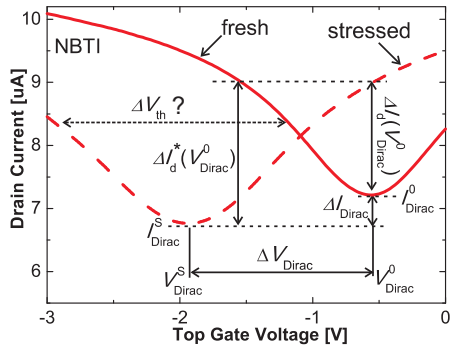

Figure 3: BTI stress results in a horizontal shift of the Dirac point V_{Dirac} and a modulation of the drain current I_d. Thus, the frequently used definition of V_{th} at which $I_d=(I_{dmax}+I_{dmin})/2$ [5–7] will see a mixture of electrostatics, mobility degradation, and contact resistance. For a correct estimate of the trapped charge density we suggest to use the shift of V_{Dirac}, $\Delta V_{Dirac}=|V^0_{Dirac}-V^S_{Dirac}|$.

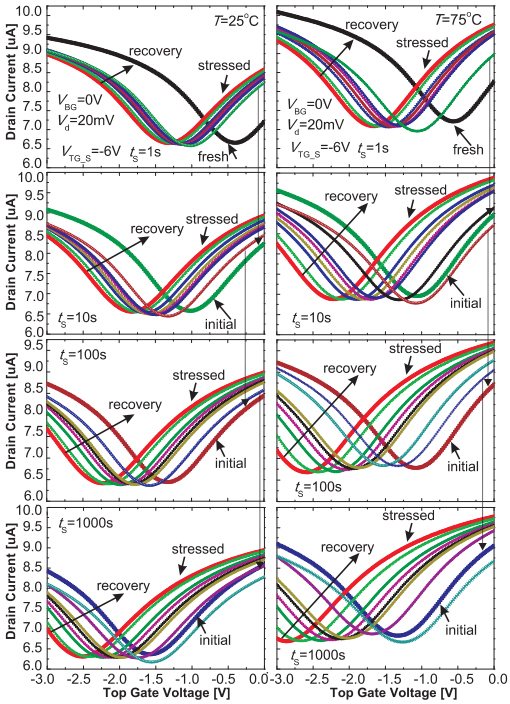

Figure 4: Time evolution of the top gate transfer characteristics after NBTI stress (1s, 10s, 100s, and 1ks) with constant stress bias. **Left**: $T=25\,^{\circ}C$. **Right**: $T=75\,^{\circ}C$. The degradation magnitude and the recovery rate strongly correlate with the stress time and the temperature of the sample.

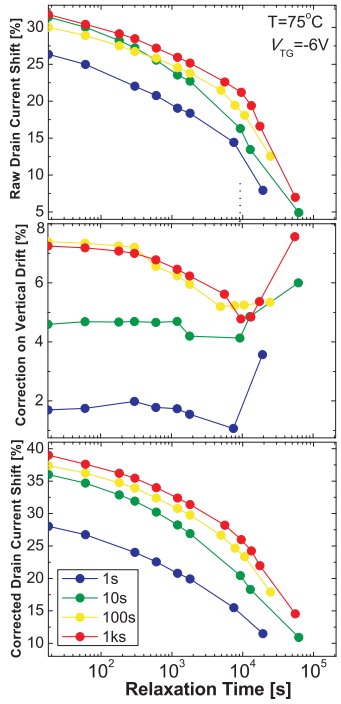

Figure 5: The recovery traces of the drain current shift relative to ΔI^0_{Dirac} after NBTI stress (see Fig. 3). **Top**: Raw drain current shift $\Delta I_d(V^0_{Dirac})$ relative to the values at the Dirac point for a fresh device (black lines, Fig. 4 top). **Center:** The drain current shift at the Dirac point $\Delta I_{Dirac}=\Delta I^0_{Dirac}-\Delta I^S_{Dirac}$. **Bottom**: The corrected drain current shift given as $\Delta I^*_d(V^0_{Dirac})=\Delta I_d(V^0_{Dirac})+\Delta I_{Dirac}$. This quantity is related to the horizontal shift of V_{Dirac}.

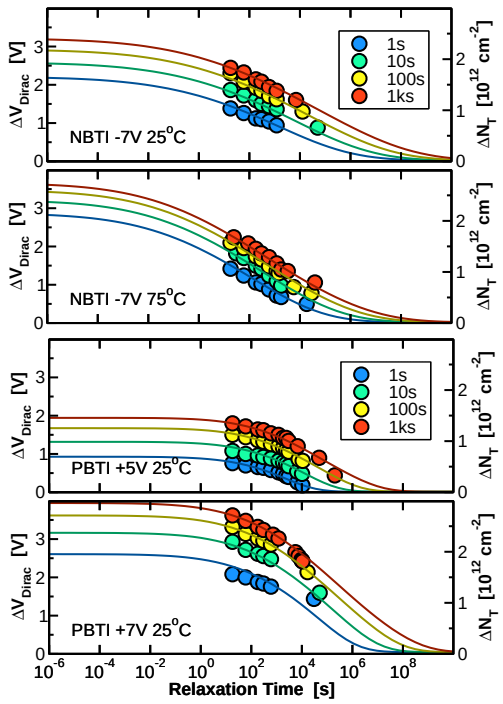

Figure 6: The recovery of ΔV_{Dirac} after four different stress times can be nicely captured using our CET map model previously suggested for silicon technologies [11] (**Top**: NBTI, **Bottom**: PBTI). As the time delay of our measurements is approximately 10s, the true degradation (i.e. at $t_r \rightarrow 0$s) of ΔV_{Dirac} has to be extrapolated. This indicates that our slow measurement misses a considerable fraction of the degradation. Note that we did not attempt to capture the traps responsible for the fast component which cause the hysteresis.

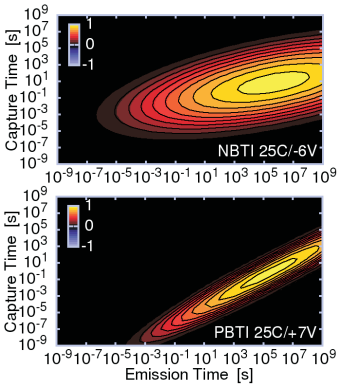

Figure 7: In our CET map model [11], the capture/emission times are described by bivariate Gaussian distributions fitted to the data as shown in Fig. 6. This allows for smoothing and extrapolation outside the measurement range. The extracted distributions (**Top**: NBTI, **Bottom**: PBTI) closely resemble those of Si technologies [11].

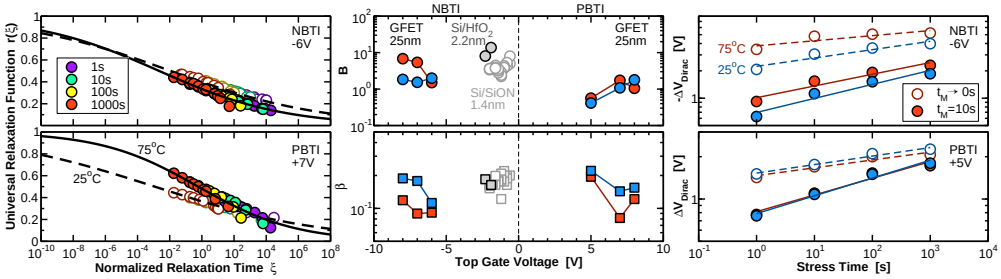

Figure 8: In Si technologies, it has been observed that the normalized BTI recovery follows a universal relaxation relation [12, 13] $1/(1+B\xi^{\beta})$. As shown in the left figures, this is also the case for BTI recovery in GFETs. Quite remarkably, the parameters (middle) are very similar to those required to fit silicon data, indicating a similarity in the underlying physical degradation processes. As with the CET map model, the universal recovery relation allows for back-extrapolation to zero measurement delay, as shown in the right. The lines are simple power law fits, the closed symbols are ΔV_{Dirac} measured with a delay of 10s, while the open symbols are the extrapolations to zero delay.