Compact Modeling of Memristive IMP Gates for Reliable Stateful Logic Design

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Extended Abstract

Introducing non-volatility into CMOS circuits is a promising solution to overcome the standby power dissipation due to leakage, which has become a major challenge of today's VLSI. Stateful logic inherently realizes non-volatile logic-in-memory circuits with zero-standby power and opens the door for going beyond the Von Neumann architecture. Recently, it has been shown that a fundamental Boolean logic operation called material implication (Fig. 1a) is naturally realized using titanium dioxide (TiO_2)-based memristive switches and enables stateful logic by using the memristive devices simultaneously as latches and logic gates [1]. Because of unlimited endurance and CMOS compatibility, the spin-transfer torque magnetic tunnel junction (STT-MTJ) has been proposed as a very favorable device for stateful IMP logic [2]. It has been shown that the easy integration of MTJs on top of a CMOS circuit allows for generalization of the MTJ logic gates to large-scale non-volatile circuits [3]. In addition, unlike the TiO_2-based gate (Fig. 1b), due to the magnetic bistability the STT-MTJ-based stateful logic gates (Fig. 1c and Fig. 1d) do not show any state drift error accumulation. As a result, the need for refreshing circuits in stateful logic circuits is eliminated.

In the IMP logic gates, the logic operation is performed by simultaneous application of two negative voltage pulses, V_{SET} and V_{COND}, to the non-common terminals of the source (S) and target (T) memory elements (Fig. 1b and Fig. 1c) or by applying the current pulse IIMP to the gate (Fig. 1d). This provides a conditional switching in the T memory element, which depends on the initial resistance states of T and S. To ensure a correct logic behavior in all input patterns, the reliability of the conditional switching in the stateful logic gates is the most important design objective. In this work the goal is to efficiently calculate the reliabilities in TiO_2-based and spintronic stateful implication (IMP) logic gates with the aid of compact but sufficiently accurate device models. It is demonstrated that for avoiding a one-bit error in the TiO_2-based IMP gate, refreshing is required after a certain number of logic steps (10–20 steps) as the state drift errors accumulate. It is shown that a modified SPICE model of the STT-MTJ fits the experimental data well and hence is able to calculate the switching probabilities required for modeling and optimization of the circuit parameters of the stateful gates.

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References

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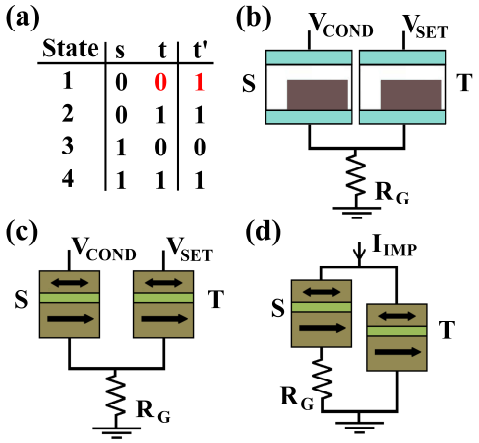

Fig. 1. (a) Material implication (IMP) truth table. (b) TiO_2-based and (c) STT-MTJ-based voltage-control stateful IMP gates. (d) STT-MTJ-based current-control stateful IMP gate.