UDK 621.3:(53+54+621+66), ISSN 0352-9045 Informacije MIDEM 20(1990)4, Ljubljana

IMPACT OF THE NON-DEGENERATE GATE EFFECT ON THE PERFORMANCE OF SUBMICRON MOS-DEVICES

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KEY WORDS: MOS-device, numerical simulation, implanted gate, non- degenerate gate

ABSTRACT: In order to analyze implanted polysilicon-gate devices our simulator MINI-MOS has been extended to solve the basic semiconductor equations also in the poly-gate area self- consistently. Heavy doping effects in the gate have been taken into account. The impact of the activated impurity concentration in the gate near the oxide and the charge at the gate / oxide interface on the performance of deep submicron (thin oxide) MOSFETs is studied by means of numerical simulation.

VPLIV NEDEGENERIRANE KRMILNE ELEKTRODE NA DELOVANJE SUBMIKRONSKIH MOS TRANZISTORJEV

KLJUČNE BESEDE: MOS tranzistor, numerična simulacija, implantirana krmilna elektroda, nedegenerirana krmilna elektroda

POVZETEK: MINI-MOS simulator smo razširili na reševanje osnovnih polprevodnih enačb v področju same polisilicijeve krmilne elektrode s čimer smo omogočili analizo tranzistorjev s krmilno elektrodo dopirano z implantacijo. Pri razširitvi smo upoštevali efekte močnega dopiranja v krmilni elektrodi. Z numerično simulacijo smo študirali vpliv aktiviranih dopantov v elektrodi blizu oksida in vpliv naboja na meji elektroda / oksid na delovanje submikronskih MOSFET tranzistorjev s tankim krmilnim oksidom.

1. Introduction

Implanted gate MOS-devices have become common in submicron technologies. Usually, N-gates are used in N-channel and P-gates in P-channel devices[1, 2, 3]. Due to the segregation of phosphorus and arsenic at grain boundaries in polysilicon[4], the activation of the impurities in N-gates can be very low after annealing (which depends on the technological process e.g. type of impurity, grain size, annealing cycle[5]). In P-gates the chemical concentration at $1 - 2 \cdot 10^{19}cm^{-3}$ in polysilicon for $TaSi_2$/polysilicon gate structures has been reported in[6]. Moreover, the temperature for the annealing of P-gates gas to be limited (in order to avoid the boron penetration[7]. In spite of the absence of the boron segregation at grain boundaries[4], the final activated impurity concentration in P-gates can be low, too.

A shift of the high-frequency C-V curve[1] as well as the degradation of (the inversion part of) the quasi-static C-V curve[2,3] has been experimentally observed in implanted poly-gate devices. The latter effect suggests a reduction of the drain current of implanted gate devices in comparison with their degenerate-gate counterparts. Consequently, the driving capabilities of devices and the speed of circuits are reduced. These experimental findings have been related to a non-degenerate position of the Fermi level in poly-gate and depletion in the poly-gate due to the penetration of the electric field into the gate. An additional severe effect in P-gates is boron penetration[7]. The implanted poly-gate can no longer be assumed an aquipotential area, especially in modeling of thin oxide devices. An analytical model of thin oxide devices, which accounts for the potential drop in poly-gate, has been presented elsewhere[(8) and its references]. In this paper, the numerical modeling of the poly-gate effect is presented, and this enables us to account for realistic doping profiles and 2D effects in submicron devices.

2. Physical model

The simulator MINIMOS 5 has been extended to solve self- consistently the basic semi-conductor equations also in the poly- gate area (including fully non-planar devices). Poisson's eqution is solved in the total simulation area (from y_t until y_B - Fig.1.).

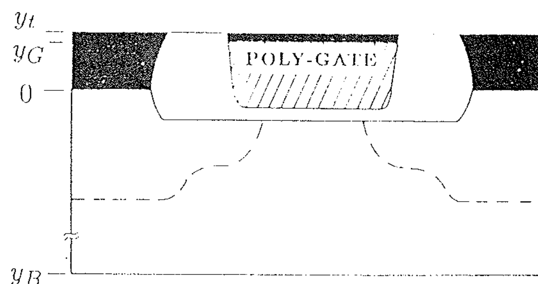

Figure 1: Simulation area

For the continuity equations two approaches have been implemented[9]. In the first one, both discretized continuity equations are solved in the poly-gate simulta-

neously with the bulk area (from y_G until y_B - Fig.1.). This approach is interesting for the transient simulation, however a proper modeling of mobility and generation-recombination phenomena in polysilicon (e.g. grain boundary recombination) is necessary. We restrict ourselves to steady-state condition in this paper. The poly-gate, is then in thermodynamic equilibrium (net recombination vanishes and leakage currents are negligible). A unique and constant Fermi level exists in the poly gate, which enables the carrier concentrations to be calculated analytically as a function of the local potential Ψ. In such an approach the discretization error of the continuity equation (specially at the non-planar gate/oxide interface - Fig.1) is avoided. This approach permits that band gap narrowing and Fermi-Dirac statistics can be implemented in a simpler way than in the first. A rigid-parabolic-band model is assumed to hold at the doping concentrations of interest. It follows then

$$n(\Psi) = N_c F_{1/2}\left\{\frac{\Psi - \Psi_G + \Phi_{fc} + \delta E_c - \delta E_{cG}}{U_T}\right\}$$

$$p(\Psi) = N_v F_{1/2}\left\{\frac{\Psi_G - \Psi + \Phi_{vf} + \delta E_v - \delta E_{vG}}{U_T}\right\}$$

where N_c, N_v are the effective density of states for conduction and valence band, and δE_c, δE_v are the local shift of the conduction and valence band due to band gap narrowing. The index G denotes the quantities at the gate/polysilcon contact (y_G at Fig.1.). It holds

$$\Phi_{fc} + \Phi_{vf} = -(E_{go} - \delta E_{gG}),$$

where E_{go} is the ideal band gap, and δE_g is the total band gap narrowing. The quantities Φ_{fc} and Φ_{vf} can be calculated by

$$\Phi_{fc} = U_T F_{1/2}^{-1}\,(N_{gG}/N_c),$$

$$\Phi_{vf} = U_T F_{1/2}^{-1}\,(N_{gG}/N_v)$$

for N-type and P-type gates, respectively. N_g is the activated impurity concentration in the gate. The neutral majority carrier concentration (which equals the activated impurity concentrarion) is assumed at the gate

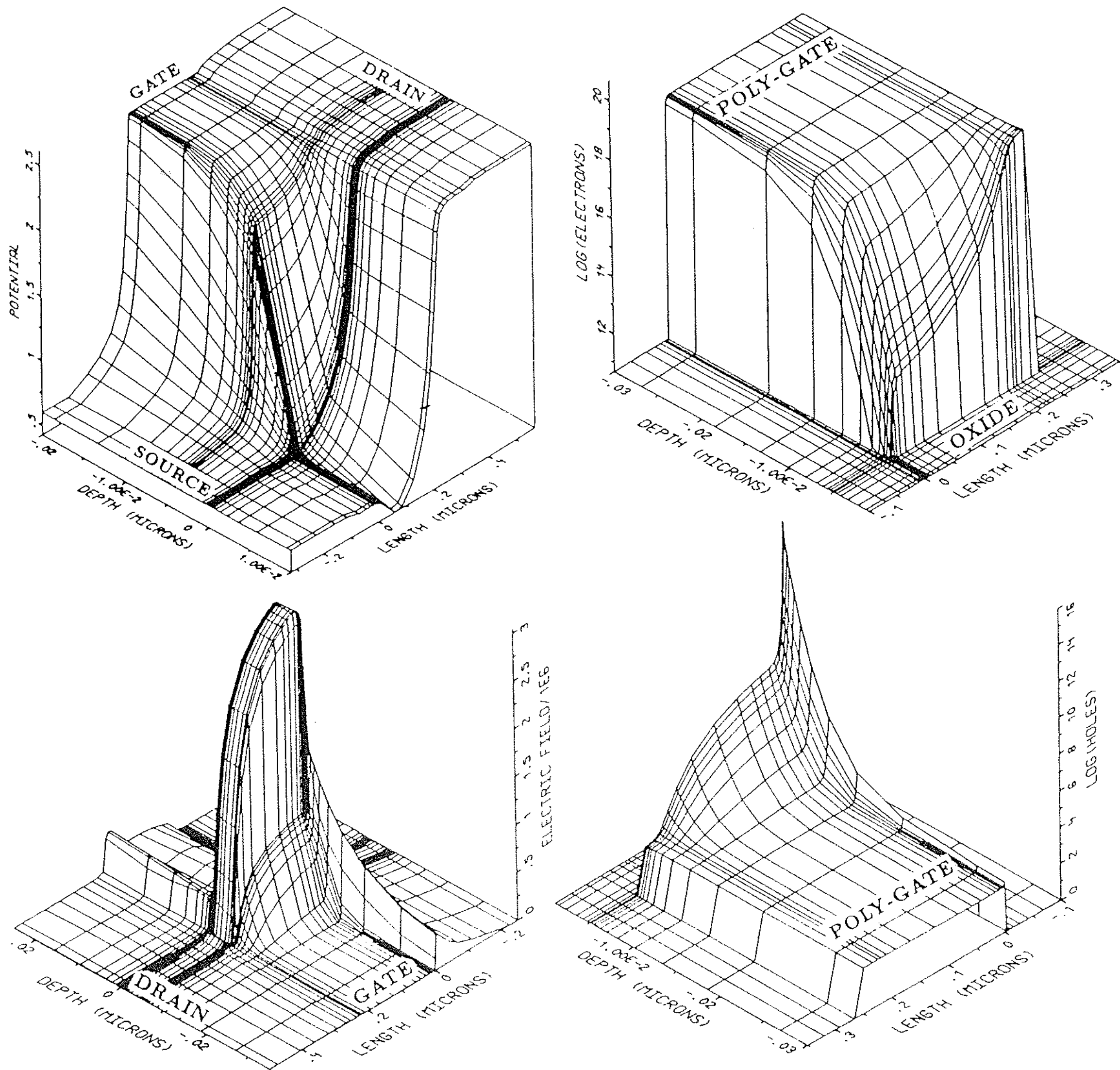

Figure 2: *Potential, field, electron and hole distributions. N-gate / N-channel device:* t_{ox} *= 5nm,* $L = 0.25\mu m$, $N_g = 10^{19} cm^{-3}$, $U_{DS} = 2V$, $U_{GS} = 2V$

contact (usually silicide/polysilicon). The top gate potential with respect to the Fermi level in the source (boundary condition) is given by

$$\Psi_G = \Phi_{fc} - \delta E_{cG} + U_{GS} + (E_{co} - E_{io})$$

where U_{GS} is the terminal voltage and E_{co}, E_{io} denote the conduction band edge and the intrinsic level in the ideal silicon band. The previous equations account properly for a position dependent band gap narrowing, and ensure that the potential Ψ is continuous in the total simulation area (from y_t until y_B - Fig.1). The Fermi integral $F_{1/2}$ and its inverse can be calculated both accurately and efficiently by analytical approximations[10].

The strong influence of the charge at the polysilicon /oxide interface on the field penetration into the gate, and therefore on the flat-band and threshold voltage, gas been demonstrated by a 1-D analytical model in reference 8. There is not much information about the nature of this charge in the literature. Since the polysilicon is deposited over oxide, it is believed that the gate/oxide interface is worse than the interface between thermally grown oxide and bulk-silicon. A positive total interface charge of order $\approx 10^{12} cm^{-2}$ has been obtained experimentally in[11]. The acceptor type interface traps have been speculated in[12], and fixed charge, traps and dipole layer gave been proposed for heavy doped gates in[13]. We have incorporated fixed oxide and interface trapped charge (with both donor and acceptor nature) in our simulations. The traps at the grain boundaries in the polysilicon have not been taken into account in the present model. If the doping is several times higher than the equivalent volume trap density in polysilicon N_{tvol} (surface trap density at grain boundary/grain size), the trapped charge is negligible compared to the space sharge due to impurity ions. A value $Nt_{vol} \approx 10^{18} cm^{-3}$ has been reported for small grain size polysilicon[(14) and its references]. Note that no accurate experimental data are available about the grain size in gates within the first few extrinsic Debye length (max $\approx$ 30nm) from the oxide.

3. Some results and discussion

The impact of the poly-gate depletion on the characteristics of thin oxide submicron MOSFETs is discussed next. Quarter-µm planar devices are analyzed. The devices have 5nm oxide thickness, threshold voltage ±0.25V, and are designed for room temperature operation. Multiple implanted source/drain profiles (Fig.1) are reconstructed from the data in literature[e.g.(1,3,15,16)]. For the P-gate device we assume that there is not boron penetration. Fig. 2 shows the distribution of the potential, field and electron and hole concentrations in the gate of the N-channel/N- gate device. Due to thin oxide, medium ionized impurity concentration at the gate/oxide interface ($10^{19} cm^{-3}$) and high gate bias (2V), a remarkable potential drop occurs in the gate. The gate-drive is reduced about 20% at the source channel-end. Note that for this device the inversion in the poly-gate takes place (beginning at the source channel-end) at $U_{GS} \approx 3.7V$, leading to the recovery of the transconductance (experimental finding in[2]). The inversion in the poly-gate produces a recovery of the quasistatic C-V curve, too (obtained experimentally in[2,3], and calculated analytically in[8]).

The threshold voltage and the potential drop in poly-gate at the threshold versus ionized impurity concentration near the gate/oxide interface N_g are shown for the P-gate/P-channel device in Fig.3. The charge at the gate/oxide interface Q_{go} (here assumed as fixed) has a strong influnce on the voltage drop in the poly-gate and therefore on the threshold voltage. Assuming Q_{go} to be a positive charge, the voltage drop in the gate is increased for a P-gate/P-channel device, while in a N-gate/N- channel device a positive Q_{go} has a screening effect.

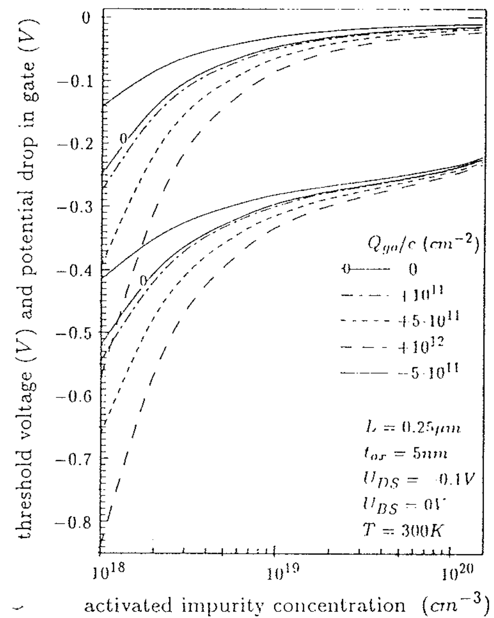

Figure 3: Threshold voltage of P-gate/P-channel device. Parameter Q_{go} is fixed charge density at gate / oxide interface.

The fall-off of the drain current in the saturation region with N_g as parameter is shown in Fig.4. For common values Q_{go} has a minor influence, and N_g is the main parameter in determination of the drain current degradation. In order to suppress totally the reduction of the gate drive, the activated impurity concentration near the gate/oxide interface must be at least $4 \cdot 10^{19} cm^{-3}$ for the analyzed 5nm-oxide devices.

The relative ratio of the effective and the terminal gate-source voltage is given roughly by (assuming solely depletion in the gate)

$$\frac{2}{1 + \sqrt{1 + 2\epsilon_{ox}^2 U_{GS} / (e\, \epsilon_{pg} t_{ox}^2 N_g)}}$$

where ϵ_{ox} and ϵ_{pg} are the permittivities in oxide and polysilicon-gate, respectively. Applying different scaling rules on t_{ox} and U_{gs} the poly-gate effect becomes more or less severe by miniaturization. E.g., for the device at Fig.4 the reduction of the current at the gate and drain

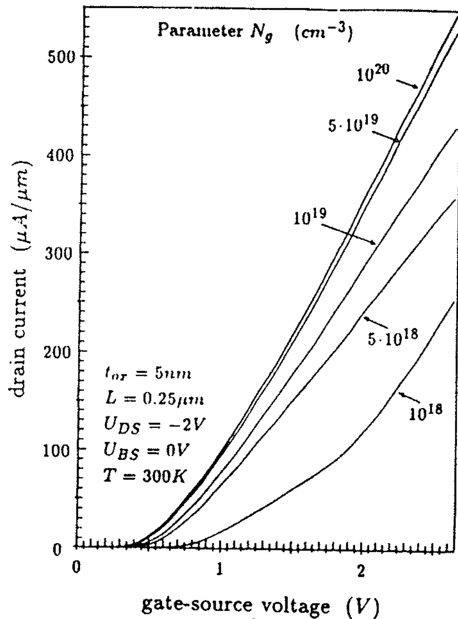

Figure 4: Transfer characteristics in the saturation for P-gate/P- channel device. The absolute values are shown.

supply voltage of - 2V is 20% at $N_g = 10^{19} cm^{-3}$, while for a simulated 10nm-oxide (0.5µm) device the corresponding reduction was 12% at -5V. Note that the recent development shows a tendency to reduce the oxide thickness under the established 5nm limit, but to keep the supply voltage high: a 3.5nm-oxide subquarter-µm CMOS technology with 2V supply has recently been presented in[15] (compared to 5nm-oxide quarter-µm device with 1V supply discussed in[16]).

Acknowledgement - Our work is considerably supported by the research laboratories of Digital Equipment Corporation at Hudson U.S.A.

References

(1) C.Y.Wong, J.Y.-C.Sun, Y.Taur, C.S.Oh, R.Angelucci and B.Davari: Doping of N⁺ and P⁺ Polysilicon in a Dual-Gate CMOS Process, in IEDM-88 Tech. Dig. p.238.

(2) C.-Y.Lu, J.M.Sung, H.C.Kirsch, S.J.Hillenius, T.E.Smith and L.Manchanda: Anomalous C- V Characteristics of Implanted Poly MOS Structure in n^+/p^+ Dual-Gate CMOS Technology, IEEE Electron Device Letters 10(5) p.192, 1989.

(3) R.A.Chapman, C.C.Wei, D.A.Bell, S.Aur, G.A.Brown and R.A.Haken: 0.5 Micron CMOS for High Performance at 3.3V, in IEDM- 88 Tech. Dig. p.52.

(4) M.M.Mandurah, K.C.Saraswat and C.R.Helms: Dopant segregation in polycrystalline silicon, J. Appl. Phys. 51(11) p.5755, 1980.

(5) Y.-C.J.Sun, R.Angelucci, C.Y.Wong, G.Scilla and E.Landi: Rapid Thermal Processing of Arsenic-Implanted Polysilicon on Very Thin Oxide, Proc. ESSDERC'88 Conf. (Journal de physique C4(9) p.401).

(6) U.Schwalke,C.Mazure and F.Neppl: Redistribution of boron implanted into $TaSi_2$/poly-Si gates, Mat. Res. Soc. Symp. Proc. 106 p.187, 1988.
C.Mazure, U.Schwalke, F.Neppl, Eichinger and M.Metzger: Influence of the fabrication conditions on the p^+- $TaSi_2$/poly-Si gate quality, Proc. ESSDERC'88 Conf. (Journal de physique C4(9) p.401).

(7) F.K.Baker, J.R.Pfiester, T.C.Mele, H.-H.Tseng, Ph.J.Tobin, J.D.Hayden, C.D.Gunderson and L.C.Parrillo: The Influence of Fluorine on Threshold voltage Instabilities in P^+ Polysilicon Gated P-Channel MOSFETs, in IEDM-88 Tech. Dig. p.443.
A.J.Walker and P.H:Woerlee: The Use of Boron Doped Polysilicon in PMOS Devices, Proc. ESSDERC'88 Conf. p.29.

(8) P.Habaš and S.Selberherr: On the effect of non-degenerate doping of polysilicon gate in thin oxide MOS-devices - Analytical Modeling, to be published in Solid-State Electronics.

(9) P.Habaš and S.Selberherr: Numerical Simulation of MOS-Devices with Non-Degenerate Gate, in Proc. ESSDERC'90 Conf., Nottingham, Sept. 1990.

(10) X.Aymerich-Humet, F.Serra-Mestres and J.Millan: An analytical approximation for the Fermi-Dirac integral $F_{3/2}$, Solid-State Electronics 24 (10) p.981, 1981.
N.G.Nilsson: Empirical approximations for the Fermi energy in a semiconductor with parabolic bands, Appl. Phys. Lett. 33(7) p.653, 1978.

(11) G.Yaron and D.Frohman-Bentchkowsky: Capacitance voltage characterization of poly $Si-SiO_2-Si$ structures, Solid-State Electronics 23 p.443, 1980.

(12) N.Lifshitz and S.Luryi: Influence of a Resistive Sublayer at the Polysilicon/Silicon Dioxide Interface on MOS Properties, IEEE Trans. on Electron Devices 30(7) p.833, 1983.

(13) T.W.Hickmott and R.D.Isaac: Barrier heights at the polycrystalline silicon-SiO_2 interface, J. Appl. Phys. 52(5) p.3464, 1981.

(14) D.M.Petković: Effect of grain size on completely dopleted grains in doped polycrystalline silicon thin films, Proc. of MIEL'89 Conf.Niš, Elsevier Advanced Technology, p.209, 1989.

(15) Y.Okazaki, T.Kobayashi, M.Miyake, T.Matsuda, K.Sakuma, Y.Kawai, M.Takahashi and K.Kanisawa: High-Performance Subquarter- Micrometer Gate CMOS Technology, IEEE Electron Device Letters 11(4) p.134, 1990.

(16) G.Baccarani, M.R.Wordeman, R.H.Dennard: Generalized Scaling Theory and Its Application to 1/4 Micrometer MOSFET Design, IEEE Trans. on Electron Devices ED-31(4) p.452, 1984.

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Prispelo: 18.10.90.   *Sprejeto: 20.11.90.*