Accurate High Temperature Measurements Using Local Polysilicon Heater Structures

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***Abstract*—Conventionally, measurements of temperature-dependent device parameters and degradation are performed using thermo chucks or dedicated test-furnaces. With such an equipment, the available temperature range is limited (typically to a maximum of $300\,^{\circ}\mathrm{C}$) and reliable temperature switches are rather slow, i.e. in the range of minutes to hours. We refine the recently suggested use of polycrystalline silicon wires – so-called poly-heaters – embedded directly on the chip next to a semiconductor device under test, to allow for fast, accurate and reliable local temperature control. Based on our previous experience with such structures, we extend the use of the poly-heater to even higher temperatures using a simple methodology. For this we determine the temperature of the device by the electrical power dissipated in the heater wires where we take the temperature dependency of the thermal resistances of the materials surrounding the heater and the device into account. With this approach we obtain convincing agreement for comparisons with experimental data and a three-dimensional electrothermal FEM simulations.**

I. Introduction

NEARLY all parameters of a semiconductor depend strongly on the temperature of the material. These dependencies have a strong impact on the performance of semiconductor devices and their reliability. In particular, in metal-oxide-semiconductors field effect transistors (MOSFETs) temperature strongly impacts virtually all reliability limiting mechanisms, including the bias temperature instability (BTI) [1–4], random telegraph noise [5, 6], hot carrier degradation [7, 8] and time-dependent dielectric breakdown (TDDB) [9, 10]. In order to investigate device performance and reliability issues with respect to temperature, fast and accurate control of the device temperature is thus highly desirable.

Usually, the device temperature is controlled by thermo chuck systems (for measurements directly on the wafer) or by dedicated furnaces equipped with electrical connections for diced devices under test. Both approaches have the drawback that reliable changes of the device temperature are rather slow (i.e. in the range of minutes to hours). For wafer-level test systems it is usually not possible to maintain the bias applied to the junctions of the device during temperature switches because the thermal expansion of the needles may push them off the pad. Furthermore, the experimental effort increases considerably in the temperature range above $\approx 300\,^{\circ}\mathrm{C}$ because the whole experimental setup needs to be built from materials which can sustain such temperatures mechanically [11].

The poly-heater [12–18] is a simple local heating structure which overcomes the limitations described above. It consists of two poly-crystalline silicon wires which closely surround the device under test directly on the chip (cf. [14, 17, 18] for layouts and cross sections of the poly-heater). When power is supplied to the poly-heater, the wires and the device in thermal contact become hot due to Joule heating. The underlying idea dates back to the year 1992, when on-chip heaters were first built from polycrystalline silicon and placed in the close vicinity of a MOSFET or a bipolar transistor [12].

Such poly-heaters are often used for fast wafer level reliability monitoring of process influences [17]. However, they have so far only rarely been used in degradation research or device development. This might be due to the disadvantage that the device temperature versus heater power characteristic usually has to be calibrated for every single device under test before use. As such, the various possibilities for testing the performance and reliability of semiconductor devices conveniently at temperatures above $300\,^{\circ}\mathrm{C}$ are still largely unexplored [2, 18].

In order to prepare the use of the poly-heater for research and development, also for temperatures beyond $300\,^{\circ}\mathrm{C}$, we suggest a reliable, accurate and easy-to-use method to determine the temperature of the device under test. Compared to the conventional calibration method, our methodology reduces the experimental effort to a single electrical calibration step per technology. This calibration gives three coefficients which characterize the change of the thermal resistance of the substrate with temperature. These coefficients can then be used to directly calculate the device temperature from the power dissipated in the poly-heater with a simple formula.

II. Determination of the device temperature

The main reason why the poly-heater has only been rarely used in the scientific community might be related to doubts regarding the actual device temperature given a certain electrical power supplied to the poly-heater. The temperature of the poly-heater itself can be determined straightforwardly with the change of its electrical resistance, since the relative change of the poly-silicon resistivity is usually known to manufacturers or can be determined experimentally. But as there is a temperature difference between the Joule heated

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poly-heater wires (hottest point) and the heat sink at the backside of the wafer (coldest point) [18], the temperature of the device under test can be significantly different from the temperature of the poly-heater and must be determined independently. As such, the temperature is usually determined using the temperature dependency of a device terminal current. The use of a device current as a temperature sensor prohibits to perform an arbitrary electrical experiment on the device during poly-heater use. Therefore, a relation of the device temperature versus the power dissipated in the poly-heater must be found prior to the experiment. If the target temperature of the experiment is within the range of the preceding calibration with a thermo chuck or a furnace, the device temperature can be easily determined by interpolation. However, if temperatures above the temperature range of thermo chucks or furnaces are targeted – and this is one of the main benefits of the poly-heater [2] – a *calibrated* extrapolation method for the device temperature as a function of the poly-heater power is needed. In the following we will describe a simple but still very accurate and reliable extrapolation method based on the temperature dependency of the thermal resistance of the semiconductor substrate.

A. Device temperature measurement

Already in the first reported uses of the poly-heater the forward current of a p-n junction within the semiconductor was used to estimate the temperature of the whole device [13]. For example, the source-drain to bulk diode was typically used for MOSFETs [13, 14, 17]. Even though this approach ignores the temperature difference between the active MOSFET interface and the body diode, which can become significant for large heater powers or large area devices, the method has been used predominantly [13, 14, 17, 19]. To resolve this issue, the output resistance R_{on} [15, 16] or the drain current I_{D} [18] have been used to determine the temperature of the device interface.

We also base our method for the determination of the device temperature on the temperature dependency of the drain current of the transistor. For this it is required to measure the transfer characteristics at several temperatures over the whole temperature range of the external heating system. From the transfer characteristics at different T_{chuck} the drain current temperature dependency $I_{\mathrm{D}}(T)$ can be extracted at an operating point (V_{G}, V_{D}) different from the temperature compensation point [20]. This dependency $I_{\mathrm{D}}(T)$ can be interpolated to map every change of the drain current with poly-heater power to an according device temperature change. This concept is explained in more detail in Fig. 1. Naturally, this method can only be used as long as the target temperature is within the range of the external heating system.

B. Experimental issues

We remark that the thermal capacitances of the materials surrounding the device and the heater may require a wait time of up to approximately 10 s after a temperature switch for the whole setup to reach thermal equilibrium [18]. For the rather small steps of the sweep of the poly-heater power in Fig. 1, a wait time of roughly a second is sufficient for all investigated poly-heater technologies.

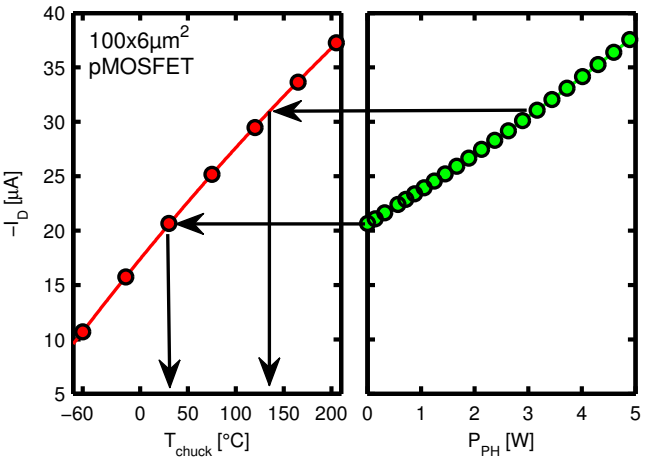

Figure 1. On the left hand side the temperature dependency of the drain current I_{D} at a suitably chosen operating point (V_{G}, V_{D}) is depicted. This dependency allows to map the increase of the drain current with increasing poly-heater power supply (right) to an increase in temperature. The increase of the drain current is independent of the biasing polarity to the heater and fully reversible and repeatable.

The increase of the drain current with heater power is independent of the actual current flow direction through the heater and fully reversible and repeatable. This proves that our electrical setup is such that the large currents (several 100 mA) and voltages (up to 40 V) needed for the heater power supply do not lead to voltage drops in the connection cables which may cause a ground shift. This indicates further that the parasitic electromagnetic fields which accompany the heater power supply do not alter the device performance. Another strong indication that the increase of the drain current when using the poly-heater is only due to a device temperature increase, can be given when using a strongly temperature dependent degradation mechanism like negative bias temperature instability (NBTI). To do so, we supplied the stress temperature either by the thermo chuck or by the poly-heater and measured the resulting degradation of a pMOSFET. We observed the same amount of degradation in both cases, which allows us to conclude that the poly-heater indeed increases and impacts only the device temperature [21].

Further, the placement of two polycrystalline silicon wires in the close vicinity of the device did not lead to any measurable differences in either the virgin characteristics or the degradation behavior of the device.

We remark that all the comments on potential experimental issues mentioned in this section apply only to the devices used and might not be transferable to other test structures, especially if they include a whole circuit of USLI technology.

III. Device temperature extrapolation

If the target device temperature is above the maximum temperature of the available external heat source, one would need to extrapolate $I_{\mathrm{D}}(T)$ to extend the method described above. This extrapolation needs to be done with a TCAD device simulation with calibrated material parameters valid

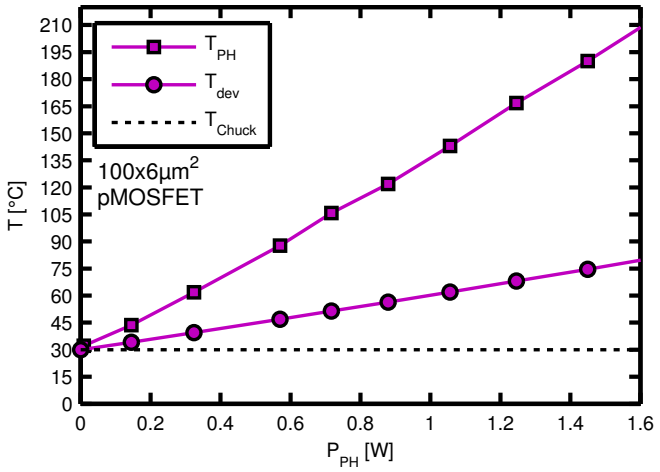

Figure 2. Change of the device and poly-heater temperature over power supply to the heater. The difference of the two temperatures is due to a vertical gradient of the temperature within the device stack, as can also be seen in the temperature distribution calculated with a three-dimensional electrothermal FEM simulation depicted in Fig. 6.

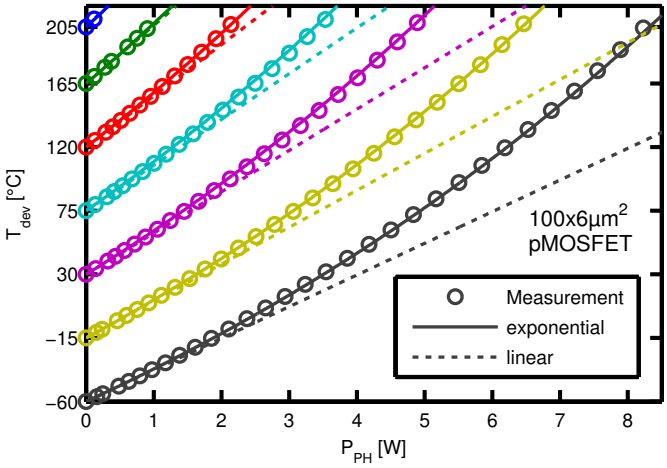

Figure 3. Device temperature T_{dev} over poly-heater power supply P_{PH} in the range of the thermo chuck between $-60\,^{\circ}\text{C}$ and $205\,^{\circ}\text{C}$. A linear extrapolation from the first $10\,^{\circ}\text{C}$ change in device temperature would lead to serious errors for large powers. In comparison, the exponential extrapolation (5) can reproduce the rise in temperature more accurately.

also in the high temperature regime. Such material parameters are rather difficult to characterize, especially when exceeding the point where the semiconductor becomes intrinsic [11, 19]. Furthermore, at such high temperatures already the low bias required to measure the temperature dependent drain current can lead to degradation of the device. To avoid those issues and to develop a method which has the potential to work up to arbitrary temperatures, we extrapolate the functional dependency of the device temperature instead of the drain current over power dissipated in the heater.

A. Linear extrapolation

With increasing power supply to the poly-heater the differential electrical resistance of the poly-heater and the drain current of the transistor increase. Both changes are mapped to a poly-heater temperature T_{PH} and a device temperature T_{dev}, respectively, cf. Fig. 2. The reason for the difference in the temperatures of the heater and the device are the finite thermal resistances of the materials between the heater wires and the device (mainly oxide, represented as $R^{\text{th}}_{\text{FOX}}$) and between the device and the chuck (usually a semiconducting or insulating substrate, represented by $R^{\text{th}}_{\text{sub}}$). Note that the thermal resistances also include the three-dimensional heat spreading in a phenomenological fashion. From the difference in the thermal conductivity of Si and SiO_2 (Si has ≈ 100 times lower R^{th} than SiO_2) and their thickness relation ($\approx 200\,\mu\text{m}$ Si to $\approx 0.5\,\mu\text{m}$ SiO_2) one would expect that $R^{\text{th}}_{\text{FOX}}$ is roughly four times smaller than $R^{\text{th}}_{\text{sub}}$. The measurement shows that it is the other way round, meaning that $R^{\text{th}}_{\text{FOX}}$ is even larger than $R^{\text{th}}_{\text{sub}}$. This discrepancy is due to the completely different heat spreading in these two layers, as shown later with the help of the FEM simulation. If these thermal resistances were independent of temperature, the device temperature would depend linearly on P_{PH}. However, this is only true for small changes in temperature as the ones depicted in Fig. 2. The increase of the device temperature with power soon deviates from a linear relationship for larger temperature differences, as depicted in Fig. 3. From this follows that for larger temperature differences the temperature dependency of the thermal resistances have to be considered in order to accurately determine the device temperature.

B. Exponential extrapolation

The electrical power P_{PH} dissipated in the poly-heater is transformed through Joule heating to an equivalent amount of heat flow $\dot{Q}$. This heat flows mainly towards the chuck because at the top surface the heat may only transfer out of the solid through radiation or convection. Radiation from directly the die surface as well as adjacent areas for larger temperature switches is estimated by the Stefan–Boltzmann law to be negligibly small ($\dot{Q} < 1\,\text{mW}$ if $T < 500\,^{\circ}\text{C}$). Convection is estimated from Newton's law of cooling with a heat transfer coefficient of air at atmospheric pressure of about $20\,\text{Wm}^{-2}\text{K}^{-1}$ to $30\,\text{Wm}^{-2}\text{K}^{-1}$ to be on the order of some $10\,\text{mW}$ for the small area of a semiconductor test structure. As such, virtually all of the heat generated by the dissipated electrical power of up to $10\,\text{W}$ flows towards the chuck.

To measure the thermal resistance of the substrate $R^{\text{th}}_{\text{sub}}(T_{\text{chuck}})$ we record the relationship $T_{\text{dev}}(P_{\text{PH}})$ at various different chuck temperatures. The thermal resistance is then given by

$$R^{\text{th}}_{\text{sub}}(T_{\text{chuck}}) = \frac{T_{\text{dev}}(P_{\text{PH}}) - T_{\text{chuck}}}{P_{\text{PH}}} \text{ for } P_{\text{PH}} \longrightarrow 0. \quad (1)$$

This value can be practically estimated by calculating the differential thermal resistance measured in a small power sweep of the poly-heater and taking the value at $0\,\text{W}$ of a first order fit of the data in a small temperature range, e.g. $10\,^{\circ}\text{C}$.

As depicted in Fig. 4, the change of the thermal resistance with temperature can reasonably well be approximated by the linear relationship

$$R^{\text{th}}_{\text{sub}}(T) = R^{\text{th}}_{\text{sub},0}\,(1 + \alpha(T - T_0)) \quad (2)$$

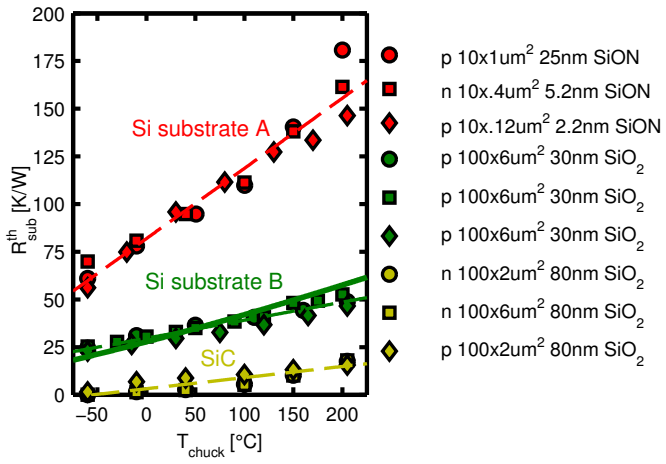

Figure 4. Dependence of the effective thermal resistance $R^{\text{th}}_{\text{sub}}$ on the chuck temperature. In the legend, n and p refer to n- or pMOSFET, respectively, the micro meter dimensions are the width times the length of the MOSFET,respectively, followed by the thickness and type of the gate oxide. The increase of the thermal resistance with temperature can be reasonably well approximated by linear functions for every technology (dashed lines). The thick solid line is the theoretical thermal resistance of silicon with $\propto T^{1.324}$ after [22] for the area of the poly silicon wires and the actual substrate thickness.

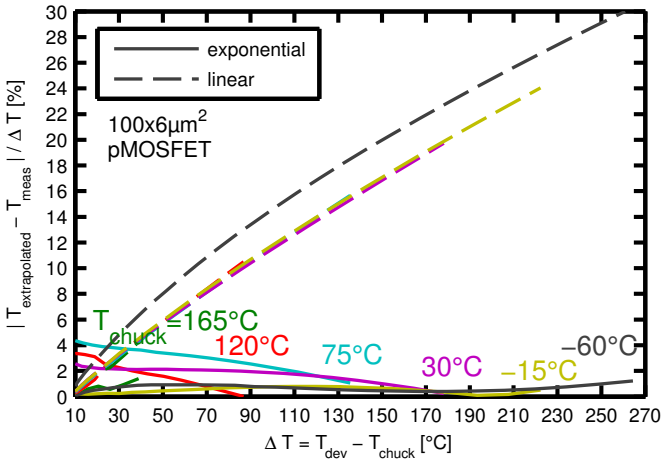

Figure 5. Comparison of the relative error of the linear and exponential extrapolation method from the first 10 °C temperature rise of the data of Fig. 3. The relative error increases with the temperature difference between the device and the chuck when taking the thermal resistances to be independent of the temperature ("linear"). When we consider a change of the thermal resistance of the substrate by using (5), the relative error stays below a few percent ("exponential").

with three constants $R^{\text{th}}_{\text{sub},0}$, T_0 and α. The first parameter $R^{\text{th}}_{\text{sub},0} = R^{\text{th}}_{\text{sub}}(T_0)$ is thereby not only due to the substrate material but includes also a temperature independent thermal resistance of the interface between the wafer and the chuck or the materials between the diced device and the heat sink of the package. If suitable test structures were available, we measured the thermal resistance on nMOSFETs or pMOSFETs, also for different device oxide thicknesses in the range of 2.2 nm to 30 nm. We observe that $R^{\text{th}}_{\text{sub}}$ depends mostly on the type and thickness of the substrate material.

The thermal resistance is defined through the change of the temperature T with heat flow $\dot{Q}$. For Joule heating, $\dot{Q}$ is equivalent with the dissipated electrical power P. We can therefore deduce

$$R^{\text{th}} = \frac{\mathrm{d}\,T}{\mathrm{d}\,\dot{Q}} \equiv \frac{\mathrm{d}\,T}{\mathrm{d}\,P} = T'(P), \tag{3}$$

which we have to base on the differential thermal resistance rather than the more commonly used absolute thermal resistance. With the assumption that the change of the thermal resistance with temperature can be approximated by a linear relationship we find the ordinary first order differential equation

$$T'(P) = R^{\text{th}}_{\text{sub},0}\left(1 + \alpha\left(T(P) - T_0\right)\right), \tag{4}$$

With the condition that T must equal the chuck temperature T_{chuck} when there is no heater power applied we obtain the solution

$$T(P) = T_0 - \frac{1}{\alpha} + \left(\frac{1}{\alpha} + T_{\text{chuck}} - T_0\right)\exp\left(\alpha R^{\text{th}}_{\text{sub},0} P\right) \tag{5}$$

or, if $\alpha = 0$

$$T(P) = T_{\text{chuck}} + R^{\text{th}}_{\text{sub},0} \times P. \tag{6}$$

This means that the temperature of the device rises exponentially with heater power. If there were no temperature dependency of $R^{\text{th}}_{\text{sub}}$ ($\alpha = 0$) then $T_{\text{dev}}(P_{\text{PH}})$ would be linear. The method therefore includes the conventional approach to extrapolate $T_{\text{dev}}(P_{\text{PH}})$ linearly.

C. Calibrated exponential extrapolation

The combination of (1), (2) and (5) is our main result: by small power sweeps at various chuck temperatures we measure $R^{\text{th}}_{\text{sub}}(T_{\text{chuck}})$ using (1) and then approximate the relationship of this curve by the linear regression (2). The device temperature is then estimated from (5) without any further fitting procedure. Thus, instead of estimating a $T_{\text{dev}}(P_{\text{PH}})$ relation for every device and chuck temperature, which cannot be substantially supported by measured data points at the upper end of the thermo-chuck temperature range, we rather search for the $R^{\text{th}}_{\text{sub}}(T_{\text{chuck}})$ relation (2) which is much more robust in its linearity and readily measured on a large temperature range with corresponding high regression quality. As such, the T_{dev} extrapolation method is calibrated by the linear $R^{\text{th}}_{\text{sub}}$ measurement.

The correctness of the exponential extrapolation method is verified within the chuck temperature range −60 °C to 205 °C through a comparison with experimental data, see Fig. 5. The relative error of this method is smaller than a few percent for the whole temperature range of the thermo chuck. This justifies the use of the exponential formula (5) within the range of the thermo chuck.

For temperatures outside the calibration temperature range, the method thus allows for a straightforward calculation of the device temperature. However, this extrapolation relies on the linear temperature dependency of $R^{\text{th}}_{\text{sub}}(T_{\text{chuck}})$, which cannot be directly validated above a certain maximum temperature. When extrapolating using (5), it is implicitly assumed due to (2) that the temperature dependency of the thermal resis-

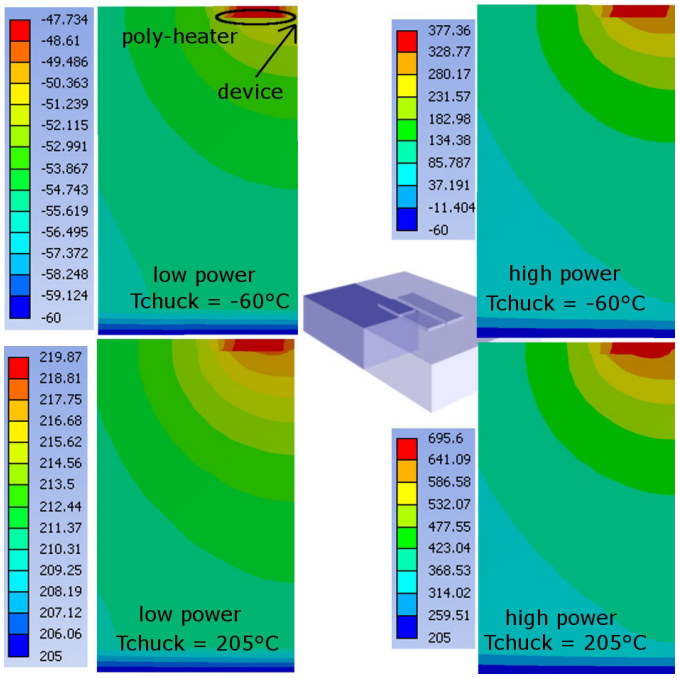

Figure 6. We performed a three-dimensional Ansys® electrothermal simulation of the lateral poly-heater structure. The symmetry of the geometry allowed to simulate only a fourth of the heater structure (see sketch in the middle). Depicted are four temperature distributions in a vertical cut in the center of the half poly-heater. Only the nearby region around the heater wires of the full model is shown, which itself extends far towards the left to account for the large heat distribution in the semiconductor. Different chuck temperatures or heater power supplies cause roughly the same temperature distribution.

tance does not deviate from its linear relationship at temperatures above 205 °C. This assumption is rather safe considering that the theoretical temperature dependency of the thermal resistance for semiconductors is $\propto T^{\gamma}$ between $\approx 100\,\mathrm{K}$ and the melting or sublimation point [22–24]. For example, in silicon $\gamma = 1.324$, and T^{γ} can be approximated with good accuracy by a linear relationship between $-60\,^{\circ}\mathrm{C}$ and $205\,^{\circ}\mathrm{C}$. With this approximation the relative error is only 9 % at $500\,^{\circ}\mathrm{C}$ (see thick line in Fig. 4). The differential equation (4) which leads to (5) can also be solved for values of $\gamma \neq 1$ which, however, makes (5) less compact and does not considerably increase the accuracy of the extrapolation.

The validity of our assumption that the thermal resistance of the whole volume underneath the device is due to the temperature of the device T_{dev} is not quite obvious. Although the substrate temperature is highly inhomogeneous from top (device) to bottom (chuck), we still observe convincing agreement between the estimated and measured device temperature with $R^{\mathrm{th}}(T_{\mathrm{dev}})$. This is because the effective thermal resistance of the substrate is determined by a small increase of the device temperature ($\approx 10\,^{\circ}\mathrm{C}$) with poly-heater power. As confirmed in the next section via numerical simulation, see Fig. 6, this small temperature difference induces approximately the same *relative* temperature distribution within the stack as a large temperature difference. The temperature is the highest in the region close to the device. Since the thermal resistance rises with increasing temperature a bottleneck forms which mainly impacts the thermal resistance of the substrate. This bottleneck influences consequently also the rise of the device temperature during poly-heater use. Since we use the same $R^{\mathrm{th}}(T_{\mathrm{dev}})$ values in both cases we consistently estimate the device temperature when using the poly-heater.

IV. Finite-element-method simulation

In order to further verify the extrapolation method (5) we have performed finite element method (FEM) simulations using Ansys®. A first approach with a two dimensional (2D) thermal simulation did not lead to satisfactory results. We needed to arbitrarily change the thermal conductivity material data of silicon in order to obtain reasonable qualitative agreement between simulation and measurement [14]. The main shortcoming of the 2D simulation approach was that the poly-heater is represented as a quasi-infinitely long device and that the influence of the electrical parameters on the temperature distribution are ignored. This is consistent with literature results [14] and confirms the 3D nature of our problem. We have therefore extended the simulation to a 3D electrothermal simulation, where we obtain a satisfying agreement.

A. Three dimensional electrothermal simulation

The simulation geometry is sketched in Fig. 6. The numerical simulation calculates the current flow through the heater wires and converts the dissipated electrical power to a corresponding heat. The temperature dependent electrical material data of the polycrystalline silicon have been acquired from polycrystalline test structures on the same wafer. We use Neumann boundary conditions (adiabatic boundary conditions, no heat flow) at all borders of the model except for the bottom surface. There we have introduced a $20\,\mu\mathrm{m}$ thick layer with a temperature independent thermal conductivity of $0.5\,\mathrm{W\,m^{-1}\,K^{-1}}$ to emulate the thermal resistance between the wafer and the chuck. The bottom surface of this layer has Dirichlet boundary conditions and is set to the chuck temperature. The value for the thermal resistance of the wafer to chuck interface is consistent with previous reports [25, 26]. The thermal conductivity of the silicon substrate has been determined in a reference measurement on an unprocessed raw wafer to be significantly lower than standard silicon [22, 23] because of a high doping level [24, 27]. Also for the numerical simulation we have reduced the power law coefficient of the temperature dependency of the thermal resistance of silicon to $\gamma = 1$ because our experimental data suggests such a dependency on the temperature (c.f. Fig. 4) and a variation of γ between 0.6 and 1.2 in our simulation did not improve the accuracy of the model.

The simulation model includes the exact dimensions of the silicon, the poly silicon and the intermediate oxide layers but misses the surrounding pads and other devices in the vicinity. This is justified because we found the cooling impact of a $20\,\mu\mathrm{m}$ thick metal plate close to the heater to be very small in a cross-check simulation. The area of the substrate material in the simulation had to be increased to $4\,\mathrm{mm}\times 4\,\mathrm{mm}$, to cover the large spread of the temperature distribution, visible in a small increase of the temperature at the lateral outside borders of the substrate block. The device temperature was estimated by

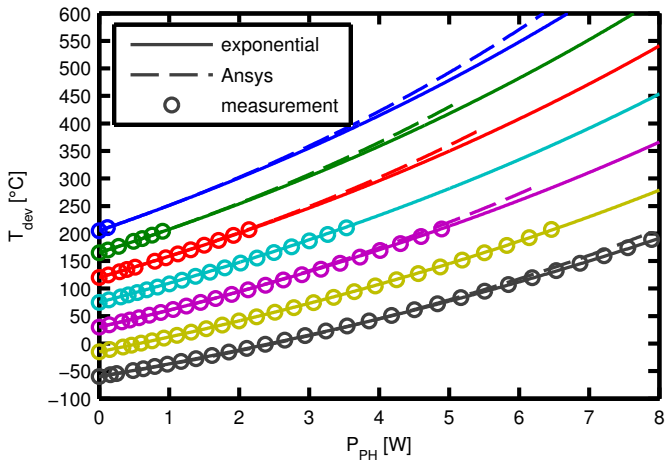

Figure 7. Extrapolation of the device temperature over heater power obtained from a three-dimensional electrothermal Ansys® simulation. Also shown is the exponential function (5). Both methods reproduce the measurement data reasonably well and give equivalent extrapolations to the high temperature regime $> 300\,°C$.

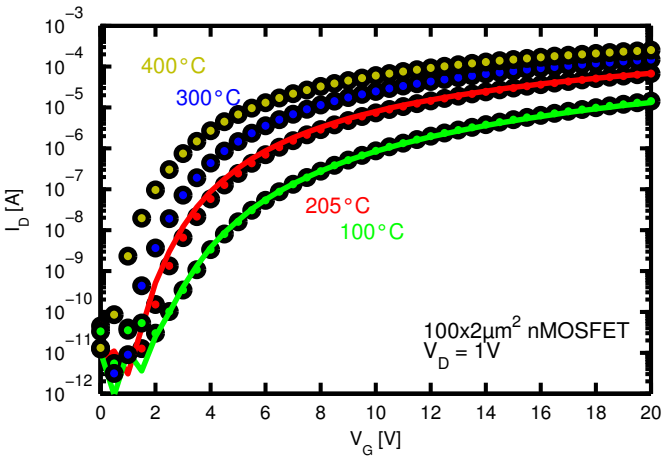

Figure 8. The poly-heater allows for effortless characterization of devices at temperatures beyond conventional chuck systems. To demonstrate this, we recorded the transfer characteristics of a silicon carbide nMOSFET at high temperatures using either the thermo chuck (lines) or the poly-heater (symbols). For the poly-heater measurements the wafer was thermally decoupled from the chuck and $4.77\,W$, $9.67\,W$, $13.0\,W$ and $15.9\,W$ were applied to the poly-heater to elevate the device temperature to $100\,°C$, $205\,°C$, $300\,°C$ and $400\,°C$, respectively.

averaging the few degree Celsius temperature variation along the plane at the Si–SiO_2 interface at the exact position of the device. As depicted in Fig. 7, both the exponential model (5) as well as the 3D electrothermal simulation can reproduce the measurement data very well. The simulation predicts a few percent higher temperature than the measurement data and the exponential extrapolation method. This is presumably a consequence of the neglect of cooling parts, such as the surrounding pads or devices, or the reduction of the substrate area to $4\,mm \times 4\,mm$ instead of the whole wafer diameter of $200\,mm$.

Of particular interest is the extrapolation of the device temperature of both methods to larger powers. There, the two methods follow different assumptions to calculate temperatures beyond $205\,°C$. The Ansys® simulation solves the heat equation with position and temperature dependent thermal conductivity values which largely represents the "real" situation. The exponential method (5) reduces the complexity by a 1D approximation and uses mainly the assumption that the change of the thermal resistance with temperature will not loose its linear dependency at temperatures $> 205\,°C$. Since both methods give very similar results we conclude that the exponential extrapolation method (5) is a valid reduction of the complexity of the problem and may efficiently be used to extrapolate to high device temperatures.

V. Applications

As a particular example, we demonstrate the use of the poly-heater to effortlessly test and operate wide band gap devices at high temperatures. In Fig. 8 transfer characteristics of a SiC nMOSFET up to $400\,°C$ are depicted. Measuring at these high temperatures usually involves a significant experimental effort [11]. With the poly-heater, characterization at these high temperatures can be achieved with standard semiconductor parameter analyzers without additional equipment [19]. The maximum achievable device temperature is only given by the power source and the breakdown electric field of the oxide between the polycrystalline silicon wires and the semiconductor. The maximum device temperature can therefore be in principal increased to values much above $400\,°C$.

In addition, poly-heaters open a range of new possibilities for device reliability and characterization. For example, it has recently been shown that negative bias temperature stress and recovery can be accelerated at higher temperatures [2]. However, the maximum temperature a fully processed device can sustain in an oven is fairly limited. The poly-heater, in contrast, creates the heat much closer to the dielectric layer and allows therefore to achieve much higher temperatures, which gives two major possibilities. First, as it is known that complete recovery through temperature treatment is possible [28, 29], the poly-heater allows one to recover from previous damage in a minimum amount of time. This idea has already been exploited to increase the lifetime of flash memory cells [30], by heating the word lines of the memory cells. Second [2], by accelerating the degradation with temperature, considerably improved lifetime estimations as well as the determination of the maximum drift of a device are possible.

Finally, because the poly-heater is a rather simple structure having temperature sensors within the semiconductor, it can also be used to determine thermal material data by matching it with a consistent simulation. Even thermal capacitances can be determined when investigating abrupt temperature switches as the ones documented in e.g. [18].

VI. Conclusions

We have presented a simple method to extend the temperature range of local poly-heater structures. The method conveniently yields the power supply needed to increase the temperature of the device to a desired target temperature. It is based on an exponential function of the electrical power

which is a direct consequence of temperature dependent thermal resistances of the semiconductor materials. We have compared the accuracy of the method within the accessible chuck temperature range with experimental data and FEM simulations. For temperatures higher than the maximum chuck temperature we compared the extrapolation of our model with a 3D electrothermal simulation. All mentioned comparisons show vanishingly small discrepancies, making the poly-heater a powerful tool for research and development as well as for reliability testing. A particular advantage of our method is given by the fact that the calibration procedure of the poly-heater has to be performed only once for each technology rather than for every single device under test.

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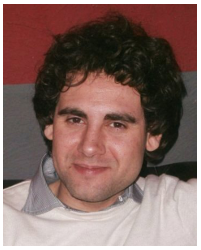

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