Reliability Analysis and Comparison of Implication and Reprogrammable Logic Gates in Magnetic Tunnel Junction Logic Circuits

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Non-volatile logic is a promising solution to overcome the leakage power issue which has become an important obstacle to scaling of CMOS technology. Magnetic tunnel junction (MTJ)-based logic has a great potential, because of the non-volatility, unlimited endurance, CMOS compatibility, and fast switching speed of the MTJ devices. Recently, by direct communication between spin-transfer-torque-operated MTJs, several realizations of intrinsic logic-in-memory circuits have been demonstrated for which the MTJ devices are used simultaneously as memory and computing elements. Here, we present a reliability analysis of the MTJ-based logic operations and show that the reliability is an essential prerequisite of these MTJ-based logic circuits. It is demonstrated that for given MTJ device characteristics, the implication logic architecture, a new kind of logic based on material implication, significantly improves the reliability of the MTJ-based logic as compared to the reprogrammable logic architecture which is based on the conventional Boolean logic operations AND, OR, etc. Implementing the implication gates in spin-transfer torque magnetic random access memory arrays provides pure electrical read/write and logic operations and also allows fan-out to multiple outputs.

***Index Terms*—Fan-out, logic-in-memory, magnetic tunnel junction (MTJ), material implication (IMP), non-volatile logic, spin-transfer torque (STT).**

I. Introduction

SPIN-TRANSFER TORQUE (STT) [1], [2] magnetic tunnel junction (STT-MTJ) technology combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability [3], [4], [5]. Therefore, STT-MTJ technology is attractive for building logic configurations which combine non-volatile memories and logic circuits (so-called logic-in-memory architecture) to overcome the leakage power issue [6], [7]. Furthermore, logic-in-memory architecture allows to shift away from the Von Neumann architecture to shorten the interconnection delay by eliminating the need to transfer data into separate memory and logic units [8]. However, in previous CMOS/MTJ hybrid computing architectures the MTJs are mostly used as ancillary devices for storing binary data [9]. Therefore, CMOS-based logic units and/or sensing amplifiers [10] are required to provide the next logic stage with an appropriate voltage or current signal as input. Furthermore, the computations are highly localized which limits the feasibility of performing logic operations between data stored in MTJs of different gates. Therefore, in the state of the art, large-scale integration of complex logic functions is difficult or may be even impossible by using the non-volatile logic-in-memory concept due to the hard linking between different gates and the need for sensing amplifiers and intermediate circuitry.

Recently, it has been demonstrated that direct communication between STT-MTJs can intrinsically enable logic-in-memory architectures (also known as "stateful" logic [11]), for which the non-volatile memory elements are used as the main devices for logic computations [12], [13], [14]. In [14], MTJ-based implication logic circuits [Fig. 1(a) and (b)] are used to realize a fundamental Boolean logic operation called material implication. In [12] and [13], MTJ-based two- and three-input reprogrammable logic circuits [Fig. 1(c) and (d)] are presented to realize the conventional Boolean logic operations including AND, OR, NAND, NOR, and Majority. Since in these MTJ-based circuits the logic (resistance) state of the input MTJs provide a state dependent (conditional) STT switching behavior on the output MTJs, the need for adding conventional logic gates and sensing amplifiers is eliminated. This allows to reduce the device count, power consumption, and interconnection delay. However, the reliability of the realized logic operations is an essential prerequisite as shown in this paper. In fact, all three-input operations and the two-input OR and NOR operations suffer from reliability issues. Here, we demonstrate that the implication-based logic architecture significantly improves the reliability of the MTJ-based logic as compared to the reprogrammable gates.

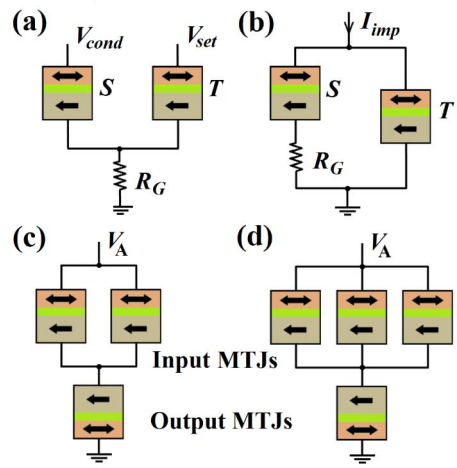

Fig. 1 MTJ-based voltage-controlled (a) and current-controlled (b) implication logic gates. Two-input (c) and three-input (d) reprogrammable logic gates. The target (T) and the source (S) MTJs act as the inputs and the final logic state of the target MTJ is the logic output of the implication gates.

Manuscript received January 08, 2013; revised April 29, 2013; accepted July 31, 2013. Date of publication August 15, 2013; date of current version November 20, 2013. Corresponding author: H. Mahmoudi (e-mail: mahmoudi@iue.tuwien.ac.at).

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Digital Object Identifier 10.1109/TMAG.2013.2278683

TABLE I
THE REALIZED CONDITIONAL SWITCHING BEHAVIOR EQUIVALENT TO THE OPERATIONS NIMP (LMPLICATION GATE), AND, OR, NAND, AND NOR (REPROGRAMMABLE GATE) OPERATIONS. THE FINAL VALUES CORRESPONDING TO THE DESCRIBED SWITCHINGS ARE SHOWN IN BLUE. REGARDING THE POLARITIES OF APPLIED CURRENT ($I_{\rm imp}$) OR VOLTAGE ($V_{\rm A}$), SOME UNDESIRED SWITCHINGS MAY BE ENFORCED WHICH ARE SHOWN IN RED. THE LOGIC INPUTS s AND t ARE CORRESPONDING TO THE RESISTANCE STATES (LRS $\equiv$ 0 AND HRS $\equiv$ 1) OF THE SOURCE AND TARGET (INPUT) MTJS OF THE IMPLICATION (REPROGRAMMABLE) GATE

			Implication output		Reprogrammable gate output							
Input			$t' \leftarrow t$ NIMP s		$y'' \leftarrow s$ AND t		$y'' \leftarrow s$ OR t		$y'' \leftarrow s$ NAND t		$y'' \leftarrow s$ NOR t	
State	s	t	s'	t'	y'	y''	y'	y''	y'	y''	y'	y''
1	0	0	0	0	1	0	1	0	0	1	0	1
2	0	1	0	1	1	0	1	1	0	1	0	0
3	1	0	1	0	1	0	1	1	0	1	0	0
4	1	1	1	0	1	1	1	1	0	0	0	0

II. STT-MTJ-BASED NON-VOLATILE LOGIC GATES

A MTJ device consists of a fixed and a free ferromagnetic layer separated by a non-conductive tunneling barrier. The magnetization of the fixed layer is pinned, while the magnetization of the free layer can be switched freely using an external magnetic field or the STT effect. The STT-MTJ exhibits pure electrical switching and better scalability than conventional MTJs switched by magnetic field. Using the STT switching technique, the direction of the applied switching current determines whether the magnetization directions of the layers become parallel (P) or antiparallel (AP). The electrical resistance of the device depends on the relative orientation of the magnetization directions of the ferromagnetic layers. The parallel alignment results in a low-resistance state (LRS; $R_{\rm P}$) across the barrier, while the antiparallel alignment places it in a high-resistance state (HRS; $R_{\rm AP}$). The MTJ resistance modulation is described by the tunnel magnetoresistance (TMR) ratio, defined as $\mathrm{TMR} = (R_{\rm AP} - R_{\rm P})/R_{\rm P}$. The most obvious application for the MTJ is non-volatile memory to store binary data via its low and high resistance states. However, recently the realization of MTJ-based intrinsic logic-in-memory architectures has been demonstrated for which the MTJ devices are used simultaneously as the memory elements and the main computing elements (logic gates) to execute material implication [14] and the conventional Boolean logic operations using reprogrammable logic circuits [12], [13].

A. Implication Logic Gates

Material implication (s IMP t) is a Boolean logic operation (reads "s implies t" or "if s, then t") which is equivalent to "(NOT s) OR t". Although it is one of the four fundamental Boolean logic operations including AND, OR, NOT, and IMP [15], it has been seldomly discussed in modern digital electronics. In fact, Shannon introduced switching algebra based on the other three logic operations [16], since they form a computationally complete logic basis and also can be easily realized using switching devices. Recently, the realization of the IMP operation has been demonstrated [11] in a voltage-controlled circuit topology [Fig. 1(a)] using $\mathrm{TiO_2}$ memristive switches [17]. However, the $\mathrm{TiO_2}$-based implication logic provides low speed and requires a different fabrication platform than the existing cost-effective silicon process. In contrast to [11], we used MTJs as the memory elements to build spintronic implication gates [14]. In addition, we proposed a new topology driven by a current source [current-controlled implication gate shown in Fig. 1(b)], which offers a more energy-efficient and reliable implementation [14]. Therefore, in this paper we employ the current-controlled implication gate in the analyses and to reduce repetition, we will henceforth avoid writing "current-controlled".

Implication logic gate realizes a logic operation based on a conditional switching behavior in the target MTJ (T) depending on the initial resistance (logic) states of the source and the target MTJs. This conditional switching behavior relies on the changes in the logic states of the source MTJ (S) which modulate the current required for STT switching in T. Due to a structural asymmetry caused by the resistor $R_{\rm G}$, the current flowing through S is lower than the level required for STT switching. Therefore, S remains unchanged for all possible combinations of the initial logic states (State 1–State 4 shown in Table I). The variables s and t represent the logic (resistance) states of S and T, respectively. The initial resistance states of S and T are logic inputs (s and t) and the final resistance state of T corresponds to the output of the implication gate (t'). According to the definitions for the resistance states, LRS $\equiv$ logic "1" and HRS $\equiv$ logic "0" or vice-versa, the realized conditional switching by the implication gate is corresponding to the IMP or NIMP (negated IMP) operation [14]. To be consistent with [13], here we use the convention of Shannon (LRS $\equiv$ 0 and HRS $\equiv$ 1). Therefore, the output of the implication logic gate corresponds to "t NIMP s" as shown in Table I. It is important to note that "t NIMP s" is equivalent to "t AND (NOT s)". In combination with the TRUE operation (SET; writing logic "1"), NIMP forms a complete logic basis to compute any Boolean function.

In order to better understand the operation of the implication gate, Fig. 2(a) shows the switching probabilities of S ($P_{\rm s}$) and T ($P_{\rm t}$) as a function of the current level applied to the implication gate ($I_{\rm imp}$) for all possible combinations of s and t (shown in Table I). The current direction of $I_{\rm imp}$ is fixed, so that only high-to-low resistance switchings (logic "1" to logic "0") are feasible in both MTJs for any input combination. When both MTJs are initially in the high resistance state ($s = t = 1$; State 4), low $I_{\rm imp}$ values (≈ 0.4 mA) can not enforce any switching, because the currents flowing through both MTJs are below the required switching current. For a correct implication logic behavior, T (S) must (not) switch to low resistance. Thus, $I_{\rm imp}$ has to be chosen in a way that T exhibits a high switching probability and S remains unchanged (within the reliable gap (RG)). This gap is provided by $R_{\rm G}$ as it limits the current flow through S. $R_{\rm G}$ is limited by the required current modulation in State 2. In State 2, although T is in the high resistance state ($t = 1$), $I_{\rm imp}$

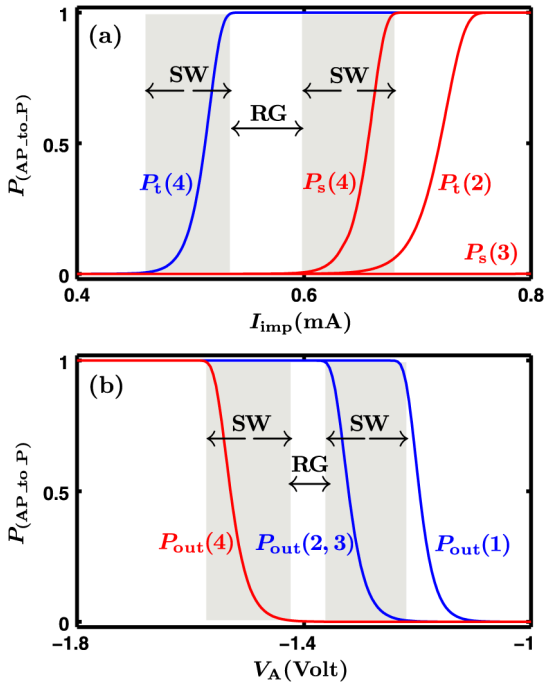

Fig. 2 Antiparallel-to-parallel switching probabilities of T and S in the current-controlled implication gate (a) and the output MTJ ($M_{\rm out}$) in the two-input reprogrammable gate according to the applied current/voltage pulses to the gate. The pulse durations (t) are 50 ns and the MTJ devices are characterized as $R_{\rm P} = 1.8$ kΩ, TMR $= 250\%$, $\Delta = 50$, and $I_{\rm CO}(AP \rightarrow P) = 325\ \mu A$. $R_{\rm G}$ is optimized to maximize the reliable gap (RG) in (a) and is equal to 0.8 kΩ.

does not switch T ($P_{\rm t}(2) \simeq 0$) since S is in the low resistance state. This requires a high enough S resistance modulation (high TMR) and also limits $R_{\rm G}$. In State 3, S is in the high resistance state ($s = 1$) and the current flowing through S is lower than the value required for STT switching due to $R_{\rm G}$ and the low resistance state of T. When both MTJs are in the low resistance state (State 1), there is no possible switching event as the direction of the $I_{\rm imp}$ is fixed.

B. Reprogrammable Logic Gates

Fig. 1(c) and (d) show the two- and three-input MTJ-based reprogrammable logic gates, respectively [12], [13]. These gates can realize conventional Boolean logic operations in two steps including a proper preset operation (TRUE or FALSE) in the output MTJ and then applying a certain voltage level ($V_{\rm A}$) to the gate. As shown in Table I, depending on the logic states of the input MTJs, the preset state of the output MTJ (y'), and the applied voltage level a conditional switching behavior is provided on the output MTJ (y'') which is corresponding to a particular logic operation. Input MTJs are left unchanged as the current flowing through the output MTJ divides between the inputs.

As an example, Fig. 2(b) shows the high-to-low switching probabilities ($P_{\rm out}$) of the output MTJ ($M_{\rm out}$) as a function of $V_{\rm A}$ applied to the two-input reprogrammable gate for implementing the AND operation with all possible input combinations ($s, t \in \{0, 1\}$). In Table I, s and t are the logic states of the input MTJs and y is the logic state of the output MTJ. First, a low-to-high resistance switching (logic operation TRUE) is performed in $M_{\rm out}$ ($y' = 1$) as preset step. Then, a negative voltage ($V_{\rm A} < 0$) is applied to the gate to perform desired high-to-low switching events ($y'' \leftarrow 0$) in $M_{\rm out}$ depending on the resistance state of the input MTJs. For a voltage level optimized within RG (shown in Fig. 2b), there are three allowed switching events ($P_{\rm out}(1-3) \simeq 1$) in $M_{\rm out}$ corresponding to the State 1–State 3 (Table I). The reliable gap RG is opened between the probabilities of the desired ($P_{\rm out}(2,3) \simeq 1$) and the undesired switching even ($P_{\rm out}(4) \simeq 0$) due to a current modulation in $M_{\rm out}$ caused by the resistance modulation at the inputs corresponding to the different logic input states. In fact, as both input MTJs are in the high resistance state ($s = t = 1$) in State 4, the current flowing through $M_{\rm out}$ is not enough for STT switching. Similar discussion can be applied to the other logic operations implemented using the reprogrammable gate.

III. Reliability Analysis

As mentioned before, by applying the current pulse $I_{\rm imp}$ to the implication logic gate [Fig. 1(b)], a high-to-low resistance switching event (logic "1" to logic "0") is enforced in the target MTJ only, when both source and target MTJs are in the high resistance state ($s = t = 1$). According to Table I, the high-to-low switching in State 4 ("$t' \leftarrow 0$") is a desired switching event in T to realize '$t' \leftarrow 1$ NIMP 1". As the current pulse $I_{\rm imp}$ tends to enforce an undesired high-to-low resistance switching event also in S, its switching probability has to be taken into account for the reliability analysis. Therefore, the reliability of the NIMP operation in State 4 is proportional to the multiplication of the probability of the desired switching in T ($P_{\rm t}(4)$) and the term $1 - P_{\rm s}(4)$ which $P_{\rm s}(4)$ is the probability of the undesired switching in S. Thus, we obtain the error probability (P_{err}) for State 4 as

$$P_{err}(4) = 1 - P_{\rm t}(4)[1 - P_{\rm s}(4)] \simeq [1 - P_{\rm t}(4)] + P_{\rm s}(4). \quad (1)$$

For a correct logic behavior $P_{\rm t}(4)$ and $P_{\rm s}(4)$ must go to unity and zero, respectively [Fig. 2(a)]. Regarding the direction of the $I_{\rm imp}$, a high-to-low resistance switching may happen in S (T) in State 3 (State 2). Therefore, when the MTJs are initially in State 3 (State 2), the error probability of the NIMP operation is given by

$$P_{err}(3) = P_{\rm s}(3), \quad P_{err}(2) = P_{\rm t}(2). \quad (2)$$

When both MTJs are in the low resistance state (State 1), there is no possible switching event, thus the error probability is equal to zero ($P_{\rm err}(1) = 0$). It is clear that for any logic operation, the correct logic behavior is ensured only when the logic gate exhibits correct logic functionality for all possible combinations in the inputs. Therefore, as equal probabilities of all input patterns can be assumed, we define the average error probability of the NIMP operation as

$$\overline{P}_{\rm err}(NIMP) = \frac{1}{4}\sum_{i=1}^{4} P_{\rm err}(i) \simeq \frac{1}{4}\{P_{\rm t}(2) + P_{\rm s}(3) + P_{\rm s}(4) + [1 - P_{\rm t}(4)]\}. \quad (3)$$

As mentioned before, the reprogrammable gates [Fig. 1(c) and (d)] rely on a conditional switching behavior in the output MTJs depending on the logic states at the input. Therefore, similar to the NIMP operation, for each reprogrammable-based logic operation we calculate the error probabilities for all possible input combinations. Table I shows how the operations AND, OR, NAND, and NOR are performed using a two-input reprogrammable gate in two steps. For example, the OR operation involves a preset in the output MTJ ($y' \leftarrow 1$) and then applying a proper voltage level ($V_{\rm A} < 0$) to the gate, which enforces a (desired) high-to-low resistance switching in $M_{\rm out}$ (logic "1" to logic "0"; $y'' \leftarrow 0$) only when the inputs are in the low resistance state (State 1). Therefore, the error probability of the OR operation in State 1 is obtained as

$$P_{\rm err}(1) = 1 - P_{\rm out}(1)[1 - P_{\rm in}(1)]^2 \simeq 1 - P_{\rm out}(1). \quad (4)$$

It is important to note that the input and output MTJs are arranged in a way that the fixed ferromagnetic layers of all MTJs are coupled to each other [Fig. 1(b)]. Thus, when $V_{\rm A} < 0$ the current flowing through the output MTJ tends to enforce a high-to-low (low-to-high) resistance switching. Therefore, $P_{\rm out}$ ($P_{\rm in}$) is the probability of a high-to-low (low-to-high) resistance switching event at output (input) MTJ. However, as the current flowing through the output MTJ divides between the input MTJs, it can be shown that the probability of an undesired switching event in an input MTJ is negligible as compared to the output MTJ ($P_{\rm in} \ll P_{\rm out}$). For input states that at least on of the input MTJs is in the high resistance state (States 2-State 4), the current flowing through the output MTJ is lower than the current required for the STT switching. Therefore, the output MTJ is left unchanged. However, in State 2 and State 3 we have

$$P_{\rm err}(2) = P_{\rm err}(3) = 1-(1-P_{\rm out})(1-P_{\rm in}) \simeq P_{\rm out}(2,3) \quad (5)$$

where due to the circuit symmetry $P_{\rm out}(2) = P_{\rm out}(3) = P_{\rm out}(2,3)$. In State 4, the only possible switching is a high-to-low resistance switching event at output MTJ. Therefore, we have

$$P_{\rm err}(4) = P_{\rm out}(4). \quad (6)$$

Compared to the OR operation, the AND operation requires a higher voltage level of $V_{\rm A}$ as a switching event ($y'' \leftarrow 0$) has to be enforced when only one of the inputs is in the high resistance state (State 2 and State 3 in Table I). It should be noted that the switching "$y'' \leftarrow 0$" in State 2 and State 3 is a desired switching event for the AND operation, while it is an undesired event for the OR operation. Therefore, for the AND operation the error probabilities in State 2 and State 3 are obtained as

$$P_{\rm err}(2) = P_{\rm err}(3) = 1 - P_{\rm out}(1 - P_{\rm input}) \simeq 1 - P_{\rm out}(2,3). \quad (7)$$

Similar to the NIMP operation, the average error probabilities of the OR and AND operations are given by

$$\begin{aligned} \overline{P}_{\rm err}(OR) &\simeq \frac{1}{4}\{[1 - P_{\rm out}(1)] + 2 \times P_{\rm out}(2,3) + P_{\rm out}(4)\} \\ \overline{P}_{\rm err}(AND) &\simeq \frac{1}{4}\{[1 - P_{\rm out}(1)] + 2 \\ &\quad \times [1 - P_{\rm out}(2,3)] + P_{\rm out}(4)\}. \end{aligned} \quad (8)$$

For performing the NOR and the NAND operations, similar subsequent steps are also executed in which the preset step is "$y' \leftarrow 0$" and $V_{\rm A} > 0$.

According to the theoretical model [18] and the measurements [19] in the thermally-activated switching regime (switching time $t > 10$ ns), we calculate the switching probability of each MTJ using

$$P = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta\left(1 - \frac{I}{I_{\rm C0}}\right)\right]\right\}. \quad (9)$$

Δ is the thermal stability factor and is equal to $E/k_{\rm B}T$ where E is the energy barrier between the parallel and the antiparallel magnetization states of the MTJ, $k_{\rm B}$ is the Boltzmann constant, and T is the operating temperature. I is the current flowing through the MTJ, t is the current pulse duration, $\tau_0 \sim 1$ns, and $I_{\rm C0}$ is the critical high-to-low (or low-to-high) resistance switching current extrapolated to τ_0 [20]. In order to calculate the current flowing through the MTJs, we use the voltage-dependent effective TMR model [21], which is important to determine the $R-V$ characteristics of the MTJs in the high resistance state:

$$R_{\rm AP} = (1 + {\rm TMR}_{\rm eff})R_{\rm P} = \left(\frac{1 + {\rm TMR}_0}{1 + \frac{V_{\rm h}^2}{V_{\rm h}^2}}\right) R_{\rm P}. \quad (10)$$

${\rm TMR}_0$ and ${\rm TMR}_{\rm eff}$ are the TMR ratio under zero and non-zero bias voltage (V) on the MTJ device, respectively, and $V_{\rm h}$ is the bias voltage equivalent to ${\rm TMR}_{\rm eff} = {\rm TMR}_0/2$.

From a circuit point of view, for given MTJ device characteristics the value of the circuit parameters ($I_{\rm imp}$ and $R_{\rm G}$ in the implication gate and $V_{\rm A}$ in the reprogrammable gates) can be optimized to minimize the error probability $\overline{P}_{\rm err}$ for each operation. An example of such an optimization for the implication gate is presented in our previous work [14]. Fig. 3 shows the average error probabilities ($\overline{P}_{\rm err}$) for different logic operations with two- and three-input reprogrammable gates as a function of $V_{\rm A}$. It illustrates that for each operation there is an optimal $V_{\rm A}$ and for both two- and three-input gates the operations AND and NAND offer higher reliability as compared to the other logic operations. In fact, as it is shown in Table I, the operations AND and NAND exhibit undesired switching when the inputs (s and t) are in high-resistance state (State 4), but a desired switching when one of the inputs is in the low-resistance state (State 2 or State 3); and the operations OR and NOR exhibit a desired switching when the inputs (s and t) are in the low-resistance state (State 1) but undesired switching when one of the inputs is in the high-resistance state (State 2 or State 3). It can be shown that the change in resistance at the input ($R_{\rm in}$) is higher when we have a modulation between State 4 and State 2 (or 3) rather than a modulation between State 1 and State 2 (or

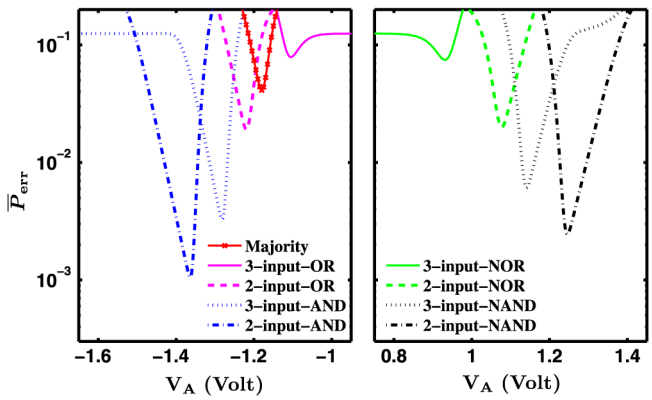

Fig. 3 The average error probabilities for different logic operations implemented with two- and three-input reprogrammable gates as a function of V_A plotted for the pulse durations $t = 50$ ns and the physical MTJ device characterized as $R_P = 1.8$ kΩ, TMR = 250%, $\Delta = 40$, $I_{C0}(AP \rightarrow P) = 325$ μA, and $I_{C0}(P \rightarrow AP) = 425$ μA.

3) ($R_{in(4)} - R_{in(2,3)} > R_{in(2,3)} - R_{in(1)}$). Therefore, AND and NAND operations provide a higher current modulation on the output as compared to the OR and NOR operations.

According to Fig. 3, for the same operation, the three-input gate has a higher error probability than the two-input gate. This is caused by a lower current modulation provided at the output of the three-input gate, due to a smaller change in resistance at the input when the number of MTJs is increased. As a result, the three-input majority, OR, and NOR operations suffer from major reliability issues. In the next section we will compare the reliabilities of the implication and two-input reprogrammable gates.

IV. Results and Discussion

As discussed in the previous section, reliable MTJ-based logic behavior requires high state dependent current modulations on the output MTJs. This modulations are caused by the resistance changes at the input for different initial logic states. According to (10), the resistance modulation between the logic 1 (high-resistance) and the logic 0 (low-resistance) states is proportional to the TMR ratio of the MTJs. Therefore, from a device point of view, we expect that for all MTJ-based operations the error probability decreases with increasing the TMR ratio which is the most important device parameter for the reliability.

Fig. 4 shows the error probabilities ($\overline{P}_{err}$) of the implication and two-input reprogrammable logic gates as a function of the TMR ratio with optimized circuit parameters (I_{imp}, R_G, and V_A) at each point. It shows that the error decreases exponentially with increasing TMR and for the same device characteristics, the implication gate exhibits a more reliable logic behavior as compared to the reprogrammable gate. It has to be mentioned that these results are obtained in the MTJ thermally-activated switching regime ($t = 50$ ns), which is extremely slow for logic applications. However, as the MTJ-based logic mainly relies on a current modulation required for STT switching, the superior reliability of the implication gate is independent of the switching regime as it is demonstrated in Fig. 5.

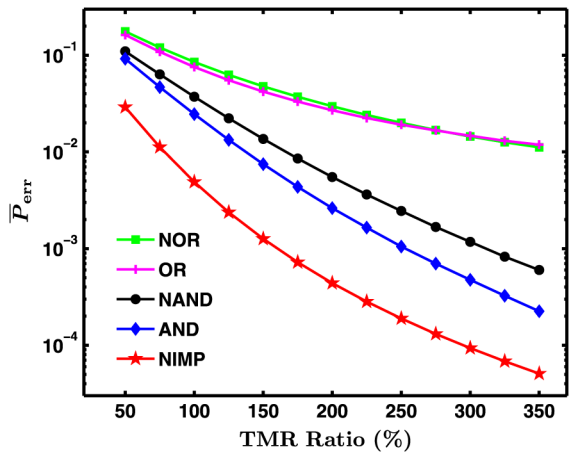

Fig. 4 The average error probabilities for the implication and two-input reprogrammable logic gates as a function of the TMR ratio. The circuit parameters are optimized to minimize the errors and the MTJ device parameters are given as $R_P = 1.8$ kΩ, $\Delta = 40$, $I_{C0}(AP \rightarrow P) = 325$ μA, and $I_{C0}(P \rightarrow AP) = 425$ μA.

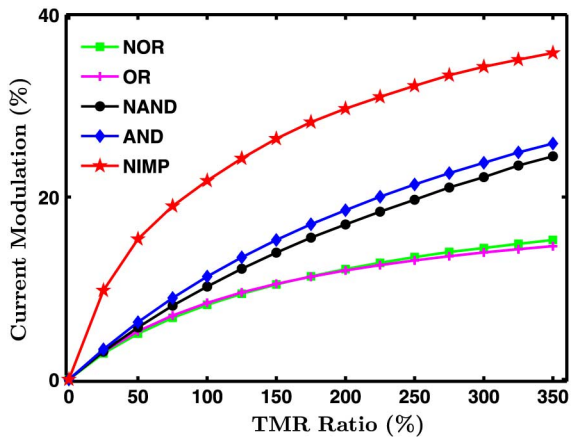

Fig. 5 Maximum current modulation $(I_d - I_u)/I_d$ in implication and two-input reprogrammable logic gates as a function of the TMR ratio. I_d is the minimum current required for a desired resistance switching and I_u is the maximum current which can enforce an undesired resistance switching. The same circuit and device parameters used in Fig. 4 are supposed.

Fig. 5 compares the maximum current modulations $(I_d - I_u)/I_d$ for each MTJ-based operation as a function of the TMR ratio. I_d is the minimum current required for a desired resistance switching and I_u is the maximum current which can enforce an undesired resistance switching as shown in Table I. For example, in implication gate I_d (I_u) is the current flowing through T (S) in State 4. For reprogrammable-based AND operation I_d (I_u) is the current flowing through M_{out} in State 4 (State 2 and State 3). As shown in Fig. 5, the implication gate allows higher current modulations compared to the highest modulation by the reprogrammable-based AND operation. Therefore, it opens a wider gap between desired and undesired switching events shown in Fig. 2 and thus inherently enables a more reliable logic behavior. In fact, with the implication logic gate (Fig. 1b), R_G provides one more degree of freedom for the circuit parameters' optimization. Therefore, the basic logic operation by the implication logic gate exhibits five times more reliable behavior as compared to the most reliable operation (AND)

TABLE II
ERROR PROBABILITIES ($E(f)$) OF 7 DISTINCT BINARY BOOLEAN FUNCTIONS FOR IMPLICATION AND REPROGRAMMABLE LOGIC GATES USING (11) AND THE ERROR VALUES SHOWN IN Fig. 3 FOR $TMR = 250\%$. REPROGRAMMABLE* SHOWS THE RESULTS FOR OPTIMAL DESIGNS BASED ON AND AND NAND OPERATIONS. PERFORMING THE NOT OPERATION REQUIRES ONE NIMP [25] (NAND [13]) OPERATION USING THE IMPLICATION (REPROGRAMMABLE) LOGIC GATE

	Reprogrammable	Reprogrammable*	Implication
AND	$\simeq 1.6 \times 10^{-3}$	$\simeq 1.6 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
OR	$\simeq 2.2 \times 10^{-2}$	$\simeq 1.1 \times 10^{-2}$	$\simeq 8.4 \times 10^{-4}$
NAND	$\simeq 3.6 \times 10^{-3}$	$\simeq 3.6 \times 10^{-3}$	$\simeq 8.4 \times 10^{-4}$
NOR	$\simeq 2.4 \times 10^{-2}$	$\simeq 8.8 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
NOT	$\simeq 3.6 \times 10^{-3}$	$\simeq 3.6 \times 10^{-3}$	$\simeq 2.8 \times 10^{-4}$
IMP	$\simeq 2.6 \times 10^{-2}$	$\simeq 8.8 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
NIMP	$\simeq 5.2 \times 10^{-3}$	$\simeq 5.2 \times 10^{-3}$	$\simeq 2.8 \times 10^{-4}$

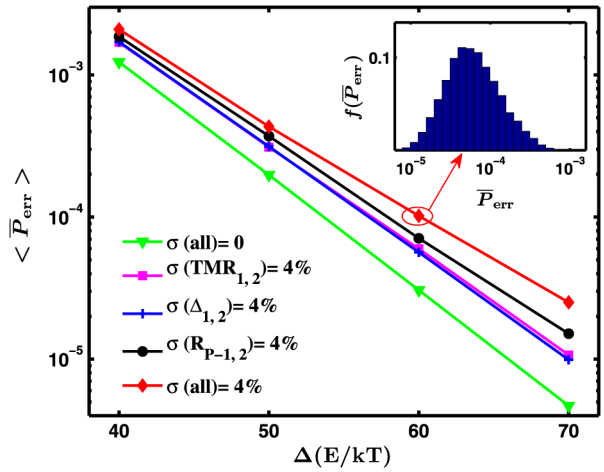

Fig. 6 The expected values of the NIMP error probability ($< \overline{P}_{\rm err} >$) as a function of Δ over 10000 samples with the Gaussian distribution for random MTJ device variations. The spread of the variations ($\sigma = \sigma/\mu$) is assumed to be 4% in Δ, TMR and $R_{\rm P}$ [26] for both target and source MTJs ($\sigma_{1,2}$). The mean values (μ) for TMR and $R_{\rm P}$ are equal to 250% and $R_{\rm P} = 1.8$ kΩ, respectively.

implemented by the reprogrammable gate (Fig. 4). The record TMR ratio of 604% [22] reported in MgO-based MTJs is close to the theoretical maximum ($\sim 1000\%$) [23], [24]. This makes the MgO-based MTJ a major candidate for STT magnetoresistive random-access memories (STT-MRAMs) and promises highly reliable MTJ-based logic architectures.

In order to preform a fair comparison, we assume the same MTJ device characteristics for both logic gates and calculate the error probabilities for implementing the same binary Boolean functions using the implication and the reprogrammable logic gates (Table II). For implication-based logic, appropriate sequential steps of NIMP and TRUE operations must be executed to perform a specific logic function [14]. With the reprogrammable gate, a network of basic logic operations including AND, OR, etc. has to be constructed. Each basic operation includes a preset (TRUE or FALSE) and a conditional switching event as explained before. We define the error probability of a specific MTJ-based logic function f as

$$E(f) = 1 - R(f) = 1 - \prod_{s=1}^{n_{\rm f}} [1 - \overline{P}_{\rm err}(s)] \qquad (11)$$

where $R(f)$ is the reliability of f and $\overline{P}_{\rm err}(s)$ is the average error probability of the sth logic step required for implementing f. Since by applying high enough voltage/current highly reliable TRUE and FALSE operations can be executed, we suppose that the error probability of a TRUE or FALSE operation is negligible compared to the error probabilities of conditional switching events in both implication and reprogrammable gates. Therefore, $n_{\rm f}$ is equal to the total number of the conditional switching events required for performing f based on either implication or reprogrammable gates.

As an example, performing an implication-based NOR operation requires three sequential steps (one TRUE and two NIMP operations) [14]. Therefore, we have $n_{\rm f} = 2$ and $E(NOR) = 1 - [1 - \overline{P}_{\rm err}(NIMP)]^2 \simeq 2 \times \overline{P}_{\rm err}(NIMP) \simeq 5.6 \times 10^{-4}$ for TMR $= 250\%$ (Fig. 4). With the reprogrammable gate, one can directly perform NOR in two steps (a FALSE and a conditional switching as shown in Table I), for which $n_{\rm f} = 1$ and $E(NOR) = \overline{P}_{\rm err}(NOR) \simeq 2.4 \times 10^{-2}$. A more efficient way to reduce the error probability with the reprogrammable gate is designing and performing the logic function f only based on the more reliable AND and NAND operations (Fig. 3 and Fig. 4). Therefore, a reprogrammable-based NOR operation can be indirectly executed as a network of two NAND and one AND operations for which $n_{\rm f} = 3$ and $E(NOR) = 1 - [1 - \overline{P}_{\rm err}(AND)][1 - \overline{P}_{\rm err}(NAND)]^2 \simeq 8.8 \times 10^{-3}$. This kind of design (shown as reprogrammable * in Table II) exhibits a more reliable behavior as compared to the direct realization of the reprogrammable-based NOR operation. However, its error is still about one order of magnitude higher than the implication-based implementation. This shows that the implication logic has a great potential to form a highly reliable MTJ-based logic framework.

As mentioned before, the TMR ratio is the main device parameter affecting the reliability MTJ-based logic gates. However, it is not the only MTJ device parameter which has to be studied for the reliability analysis. It can be shown that the computations can be generalized by normalizing all currents and resistances to $I_{\rm C0}$ and $R_{\rm P}$. Therefore, the error values are independent of the exact values of $I_{\rm C0}$ and $R_{\rm P}$. Furthermore, in the thermally-activated switching regime, the effect of the switching time value (t) is negligible as compared to the internal exponential term in (9). According to (9), the dominant term for the error calculation is $[-\Delta(1 - I/I_{\rm C0})]$. Since the modulation of $I/I_{\rm C0}$ depends on the TMR ratio value, a higher TMR decreases the errors as shown before. A higher Δ enlarges the effect of this modulation. Therefore, for a given TMR ratio (a constant the modulation in $I/I_{\rm C0}$), higher Δ decreases the error probabilities as shown in Fig. 6.

In order to investigate the effect of the MTJ device-to-device variations, Fig. 6 shows the expected NIMP error probabilities ($< \overline{P}_{\rm err} >$) as a function of Δ for MTJ device variations with Gaussian distributions [26]. For each point, circuit

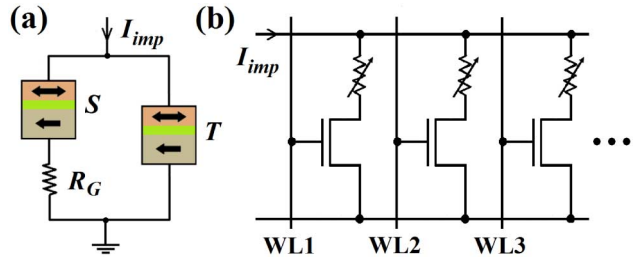

Fig. 7 Structural diagram (a) and a possible STT-MRAM-based implementation (b) of the current-controlled implication logic gate. The structural asymmetry provided by $R_{\rm G}$ in (a) is obtained in (b) by applying two different voltage levels to the word lines (WLs) simultaneously. As the optimal $R_{\rm G}$ is less than 1 kΩ ($\simeq R_{\rm P}/2$), the channel resistance can act as $R_{\rm G}$ when the access transistor is pre-selected.

parameters are fixed to the values which minimize the error For 10000 random variations, the average error probability for all combinations of the input states ($\overline{P}_{\rm err}$) is calculated. Then the expected error values are obtained by $\sum f(\overline{P}_{\rm err})\overline{P}_{\rm err}$ where $f(\overline{P}_{\rm err})$ is the distribution function of the errors (shown inset in Fig. 6). As it is expected, MTJ device variations increase the error probabilities as shown in Fig. 6. However, variations in Δ and TMR show smaller effects compared to $R_{\rm P}$, since their positive random variation values tend to decrease the error according to Fig. 6 and Fig. 4, respectively.

For the sake of generalizing the MTJ-based logic gates to large-scale logic circuits and performing more complex logic functions, it is necessary to use the output (target) MTJ of one reprogrammable (implication) gate as the input for the next stage of logic. Therefore, in our simulations the same device characteristics are assumed for all MTJs in each gate. Due to the MTJ's non-volatility and easy integration with CMOS, Hybrid CMOS/MTJ technology is promising for the development of innovative non-volatile logic architectures. As an example, Fig. 7b shows a possible implementation of the implication logic based on an STT-MRAM array [19]. In a memory (read/write) mode, a selecting voltage ($V_{\rm s}$) is applied to an arbitrary word line (WL) to allow current to flow through the correct MTJ. In a logic (implication) mode, a selecting ($V_{\rm s}$) and a pre-selecting ($V_{\rm ps}$) are applied to two arbitrary WLs where $V_{\rm s} > V_{\rm ps}$. As the applied voltage to the gate of the pre-selected access transistor is lower it exhibits a higher channel resistance and acts as a voltage-controlled resistor. This provides the structural asymmetry required for the implication gate shown in Fig. 7. It should be noted that the nonzero ON resistance of the access transistors decreases the effective TMR of the one transistor/one MTJ (1T/1MTJ) cells by about 10% [26]. However, pure STT-based read/write and logic implementation brings significant advantages of scalability and lower energy consumption [5]. Therefore, 1T/1MTJ-based implementation of the reprogrammable gates (Fig. 1c and Fig. 1d) can provide independent access to the input MTJs for STT writing instead of magnetic-field-based switching used in [13]. This can extend the functionality of the STT-MRAM architecture to include performing logic operations and eliminates the need for data transfer between separate memory and logic units.

In the magnetoresistive (MR) non-volatile logic the resistance states of the MR devices are the physical state variables. This is different compared to CMOS logic where information is represented by charge or voltage. Most of the previous proposals for MR-based logic circuits [27], [28], [29], [30], [31], [31], [32], [33] require intermediate circuitry for sensing the data stored in each non-volatile magnetic element and implementing fan-out functions. This increases the power consumption, time delay, area, and integration complexity. A possible remedy is to switch to direct communication between the MR devices thus removing intermediate circuitry [13], [14], [34], [35], [36], [37], [38]. However, this makes the computations localized by confining them to the MR devices which are directly coupled. Only recently, a groundbreaking step was presented in [12] to remove the aforementioned obstacles in the MTJ-based reprogrammable logic architecture by using current mirrors for fan-out to multiple outputs.

In the MRAM-based implication logic architecture (Fig. 7b), the issue of the non-volatile logic fan-out function is addressed as follows. The output information of a logic operation (IMP/NIMP) can be used to perform the next operation with an arbitrary MTJ in the array as a source (or a target) input. This provides high flexibility with regard to the non-volatile logic fan-out function. Indeed, when multiple fan-out is required, a set of FALSE (TRUE) and IMP (NIMP) operations (performing NOT and COPY operations) allows to copy information from the source MTJ to an arbitrary target MTJ in the array without the need for intermediate sensing. In fact, until the output of an operation is needed to be used only as the source data for the next operations, NOT/COPY operations are not required as the data is left unchanged. However, when the output is needed to be used as target data several times, implication-based NOT/COPY operations are used to keep the data available. In this logic framework, as only one operation at a time can be performed in each array, complex logic functions are implemented by using subsequent FALSE (TRUE) and IMP (NIMP) operations which form a computationally complete basis. Regardless of the number of inputs, only two extra (work) memory cells (MTJs) are needed to compute all Boolean functions [39]. An example of sequential steps required for implementing a full adder function in this computation framework is presented in [25].

As both reprogrammable-based NAND and implication-based IMP/NIMP (combined with writing '0'/'1') form complete logic bases, any Boolean logic function can be computed in a series of subsequent steps using these gates. Parallelization of several MRAM arrays can be used to perform parallel operations on the same word lines to decrease the number of required serial steps. Furthermore, combining implication-based IMP/NIMP and reprogrammable-based AND/NAND operations in the MRAM arrays can be a possible direction in designing MTJ-based logic circuits with a minimized number of logic steps and optimized error, delay, and power consumption. Finally, one has to mention that even though reliability is a very important performance parameter, it is only a part of the picture. Recently, Nikonov and *et al.* [40] have tried to compare different performance parameters, e.g., energy, speed, area, etc. between a wide range of logic types but still further studies are required.

V. Conclusion

Reliability analyses and comparisons of MTJ-based implication and reprogrammable logic gates are presented. It has been shown for given MTJ device characteristics, the implication logic gate enables a more reliable logic behavior as compared to the reprogrammable logic gates. In the MTJ thermally-activated switching regime, the error probabilities decrease exponentially with increasing TMR ratio as well as with the thermal stability factor (Δ). Since the MTJs serve simultaneously as non-volatile memory and the main computing elements and element, there is no need for intermediate circuitry. MTJ-based logic enables intrinsic non-volatile logic-in-memory circuits which decrease the device count and exhibit low power consumption, high logic density, and high speed operation simultaneously.

Acknowledgment

The work was supported by the European Research Council through the grant #247056 MOSILSPIN.

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